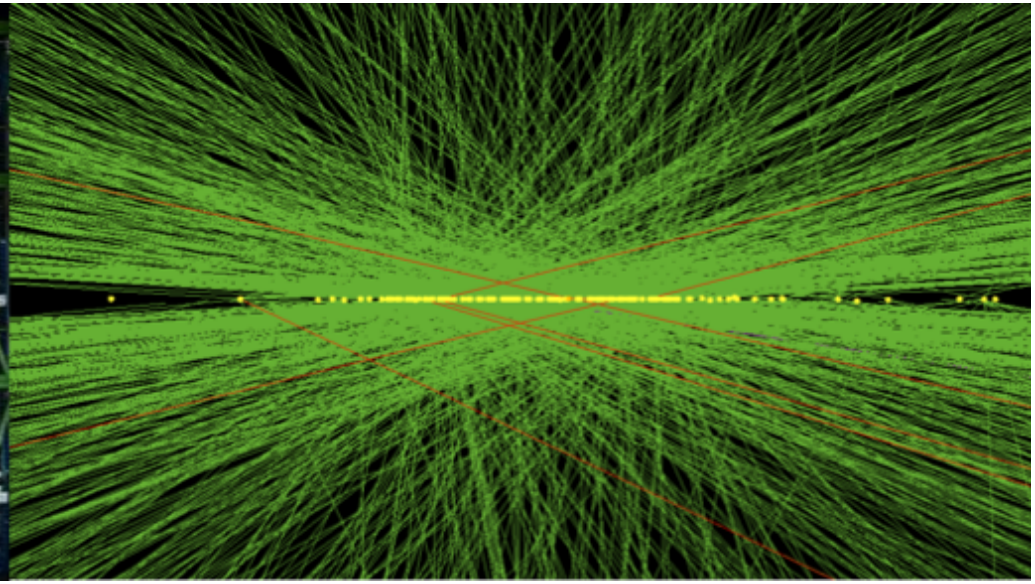
402.4.6 CE – Scintillator Calorimetry

Ted Kolberg (FSU) L3 Manager

HL LHC CMS CD-1 Review

October 23, 2019



Outline

- Technical Aspects of Scintillator Calorimetry
  - Conceptual Design
  - Scope and U.S Deliverables
  - QA/QC
- Managerial aspects of Scintillator Calorimetry
  - Cost, Schedule, and Risks
  - Contributing Institutions
  - ES&H
- Summary

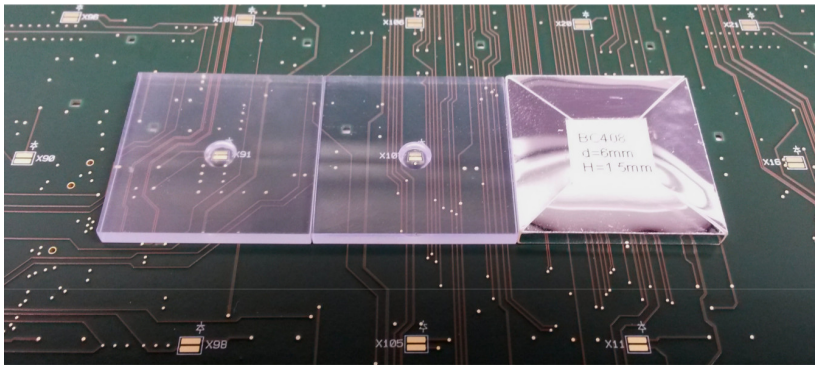
Our team

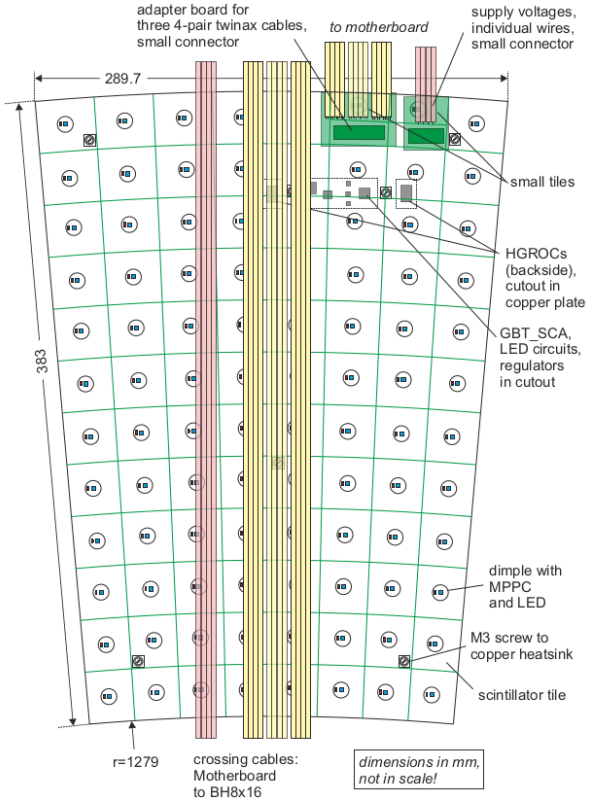
- L3 manager for CE – Scintillator Calorimetry
  - Assistant Professor at Florida State University
  - More than a decade of experience with CMS calorimeter systems:
    - Commissioning and installation of CMS ECAL
    - ECAL back end electronics
    - HCAL Phase 1 upgrade to SiPMs
  - Exotic decays of the Higgs boson to long-lived particles
    - Study use of CE for its innovative trigger and reconstruction capabilities
  - Also L4 for scintillator motherboards
- Key management team members
  - Vishnu Zutshi, NIU (L4 for scintillator tiles)
    - Extensive experience with CALICE SiPM-on-tile R&D
  - Harry Cheung, FNAL (L4 for module assembly)
    - Experience includes Phase 1 Pixels, also CE deputy L2
  - Mitch Wayne, ND (L4 for SiPMs)
    - Also closely involved with SiPM development for HCAL Phase 1, MTD projects

Conceptual Design

Conceptual design: tile-module

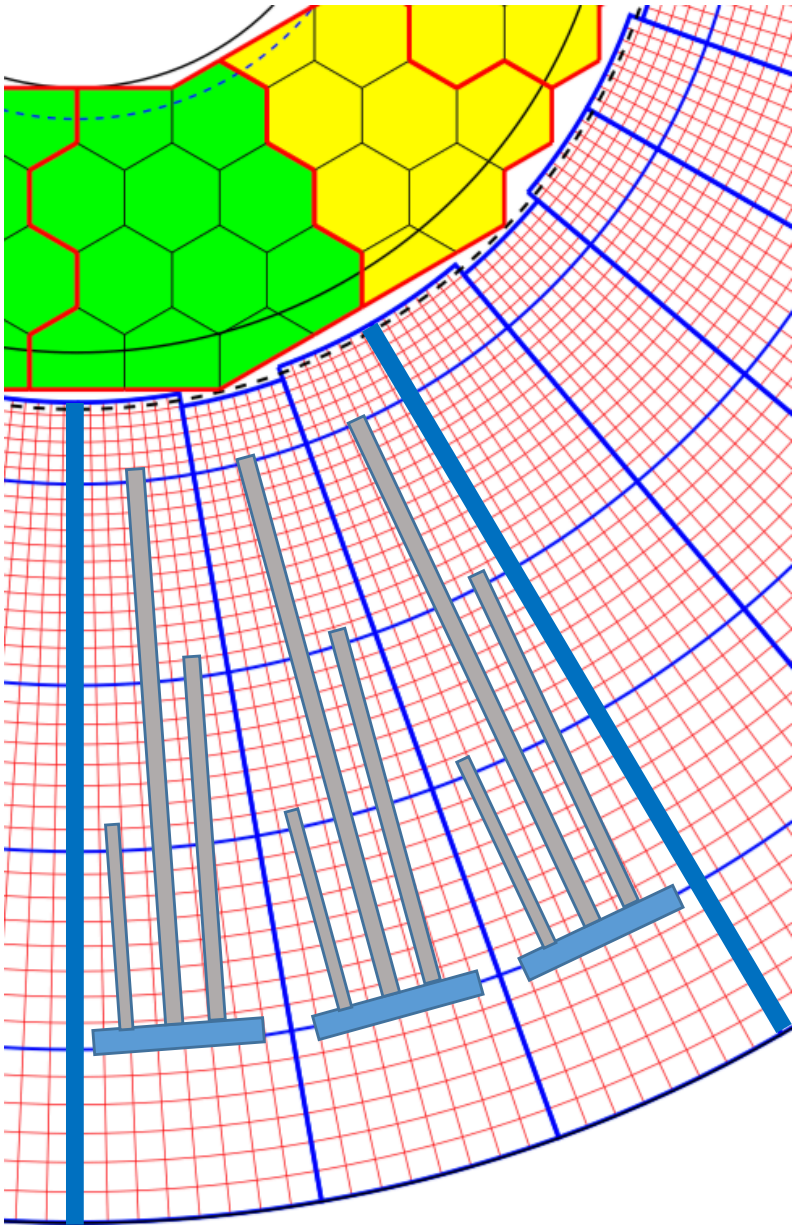
Charge #1

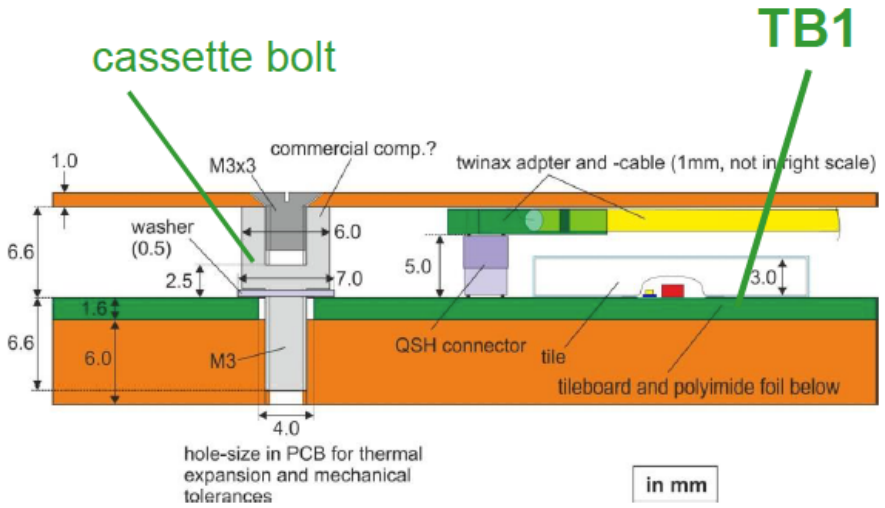




- Key technology: SiPM-on-tile.
  - Scintillation light from tiles directly illuminates SiPM photodetector underneath tiles.
  - Reflective wrapping on tiles (ESR) maximizes light reaching SiPM.
  - 'Dimple' in tile equalizes response across tile and provides space for SiPM and monitoring LED.
  - Detector in cold volume limits SiPM noise to acceptable levels even after irradiation.
  - Tile size is determined by the calibration strategy using MIPs, and depends on radiation hardness of scintillator and SiPMs.
- Active area is covered by fan-shaped tile modules.
  - Module PCB hosts the SiPM photodetectors and the HGCROC readout chips plus associated controls.
  - LED system for commissioning and monitoring.
  - Use a standardized list of module types to cover all layers.

Conceptual design — cassette





- Outer portion of mixed cassettes are tiled with scintillator (where radiation allows)
- Services and signal cables are routed over the tops of the installed tile-modules.
- Data and trigger streams from HGCROCs is brought to motherboards in the outer portion of the cassette
  - One per 10-degree sector.
  - ECON ASICs merge DAQ/trigger output of all tileboards in sector
  - Electrical-optical conversion of outgoing signals
  - Provide voltages and slow controls to tile modules inside of cassette
  - Motherboard assembly includes passive components (cables and adapter PCBs) to bring signals to motherboard.

Deliverables for 402.4.6

- Scintillator development and prototyping
  - Scintillator tile R&D: produce samples of scintillator materials under consideration, injection molding development, cold slow irradiation campaign, test beam measurements.
  - ESR wrapping procedure, tools, QC.
  - Tile module assembly procedures, tools, QC.
  - Production and assembly of tile boards for prototyping campaigns.
- Scintillator production
  - Bare scintillator tiles are produced internationally (Russia). 50% of total needed (plus spares and test beam wedge) will be shipped to US. Reception and QC of bare tiles — 150k tiles.
  - Wrapping with ESR, QC of wrapped tiles, and sorting for assembly into tile modules.

Deliverables (cont.)

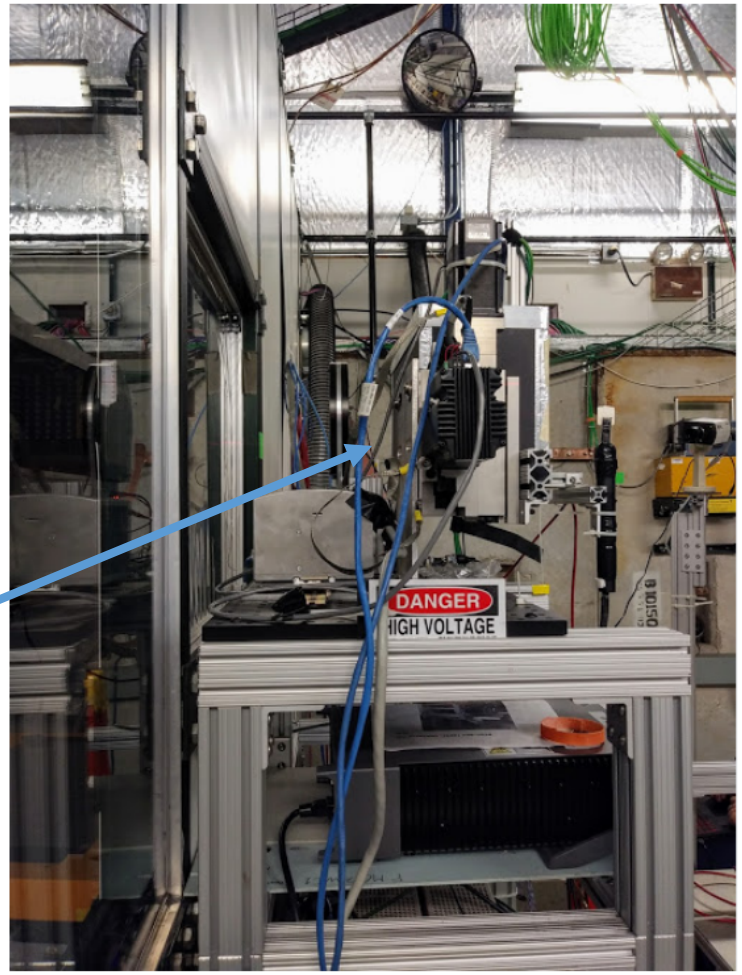
- SiPM photodetectors
  - Development of SiPM structure and packaging in collaboration with vendor.
  - Testing of prototype SiPMs, in particular after irradiation.
  - Purchase of SiPM production run, 50% of total (plus spares and test beam wedge), QC of production SiPMs — 142k SiPMs.
- Scintillator tile modules
  - US is responsible for one-third of total tile module production (plus spares and test beam wedge) — 1404 tile modules.
  - Procure tile module PCBs and electronics, QC of PCBs.
  - Assembly of tiles onto PCBs, QC of assembled modules.
- Scintillator motherboards
  - Design and construction of 1050 scintillator motherboard assemblies for all CE-H plus associated passive components (cable assemblies and adapters), including spares and test beam wedge.
  - Motherboard assemblies for prototype campaigns.

R&D Achieved

- We are pursuing a vigorous R&D program in order to converge on a baseline design for all aspects of the system:
  - Characterization of scintillator tiles and wrapping methods.
  - Developing an automated tile wrapping system.
  - Understanding performance of candidate SiPMs under CE-H conditions.
  - Development of tile module prototypes.
  - Tile module assembly techniques.
  - QC procedures & teststands.

R&D — Scintillator tiles

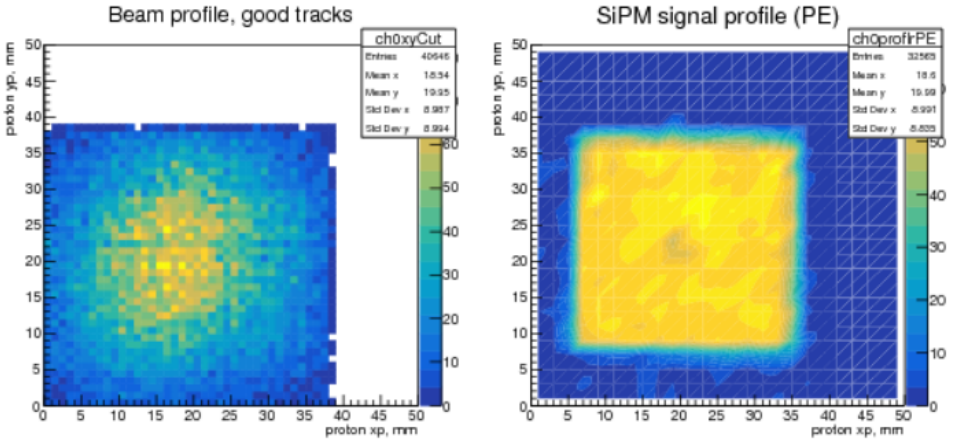
- We are well advanced in our R&D plan to understand the performance of the tiles. FNAL FTBF playing a main role.



Si X, Y planes

Dark box on moving table

FNAL FTBF results



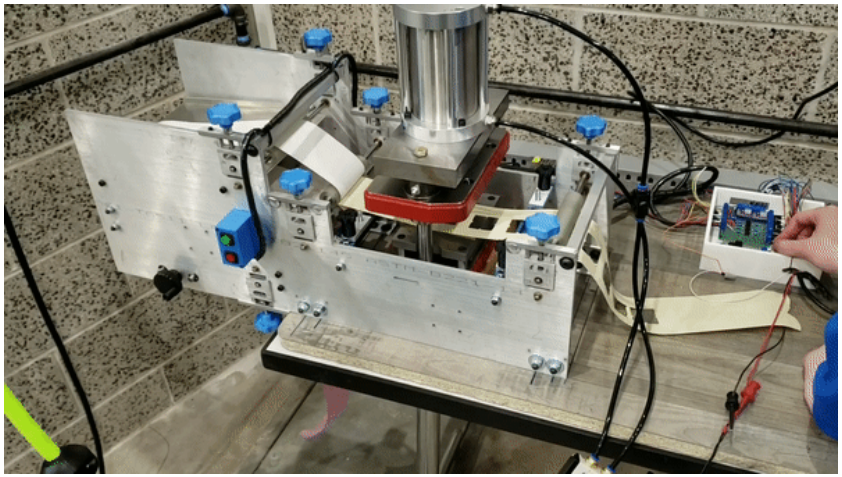
Beam Tests:: 120 GeV protons, FTBF, May 10 – Jul 05, 2019
1.3x1.3mm2 SiPM, S13360-1350, Vop=54.5V, small hole

Tile	MPV, L+G fit (PE)	FWHM	Mean (L+G fit)**	Mean (hist)
EJ208esr	51.2	21.8	50.6 +/- 0.1	59.2
EJ200esr	41.9	19.7	41.7 +/- 0.1	50.0
SC301esr*	35.7	17.8	35.5 +/- 0.1	42.3
SC307esr*	29.6	16.7	30.0 +/- 0.1	36.5
Calice Tile	21.8	13.5	22.8 +/- 0.4	28.1

J. Freeman (FNAL), S. Uzunyan (NIU)

R&D – Tile wrapping

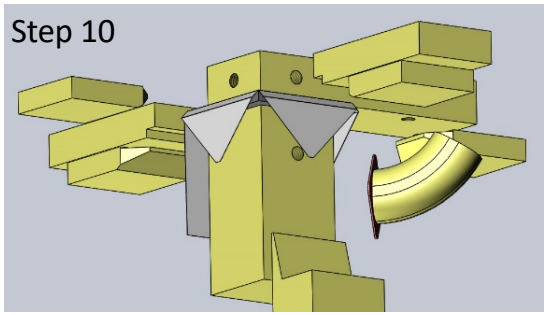
Gerald Smith, Ramanpreet Singh, Alexandre Dychkant, Iman Salehinia, Nicholas Pohlman, Vishnu Zutshi (NIU)

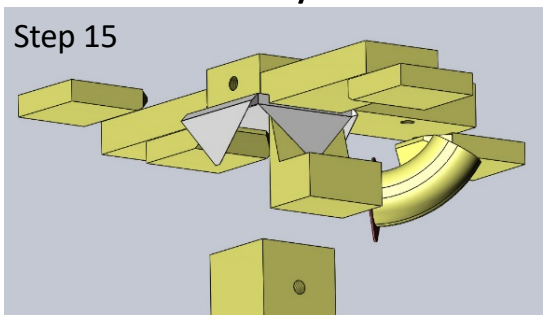


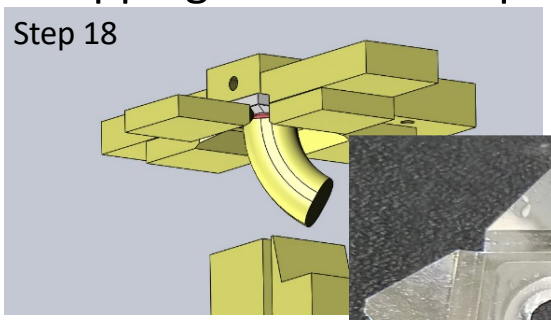
Die punch for cutting wrappers ($250/size)

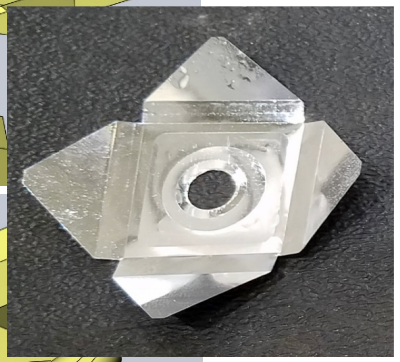
N = 40	Horizontal [mm]	Vertical [mm]
Min	31.53	31.62
Max	32.38	32.32
Stats	32.03 ± 0.235	32.05 ± 0.196

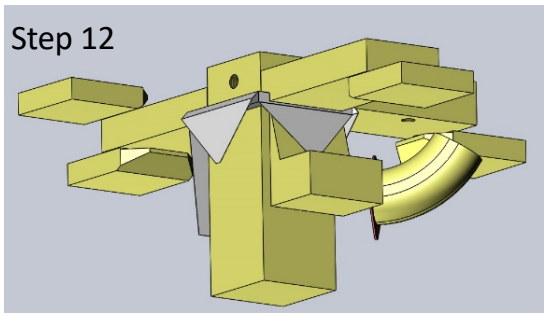
Fully automated wrapping station concept

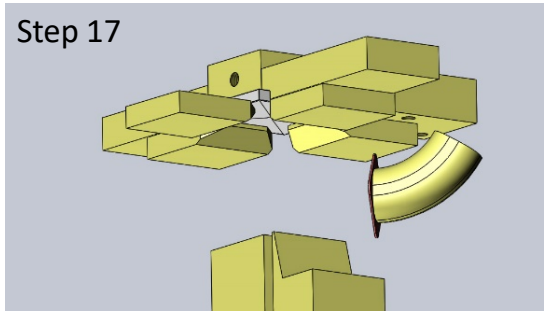


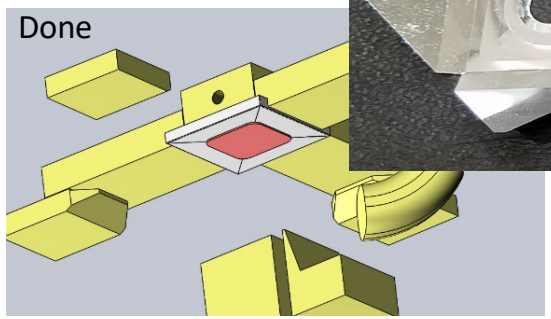






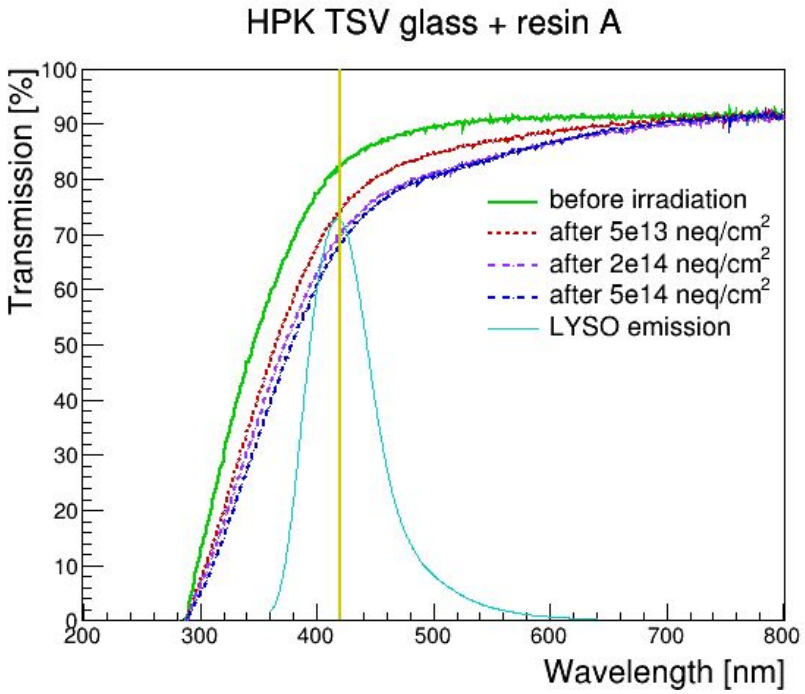


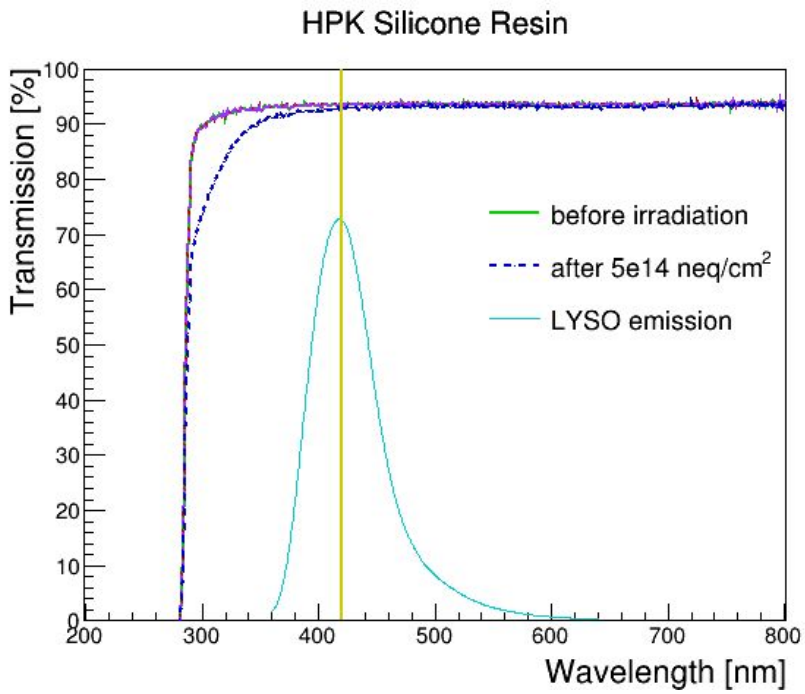




R&D – SiPM window

- Standard TSV package with glass window down to 75% transmission after 5e13 neq/cm^2.
- Transmission remains above 90% after irradiation with silicone resin window.

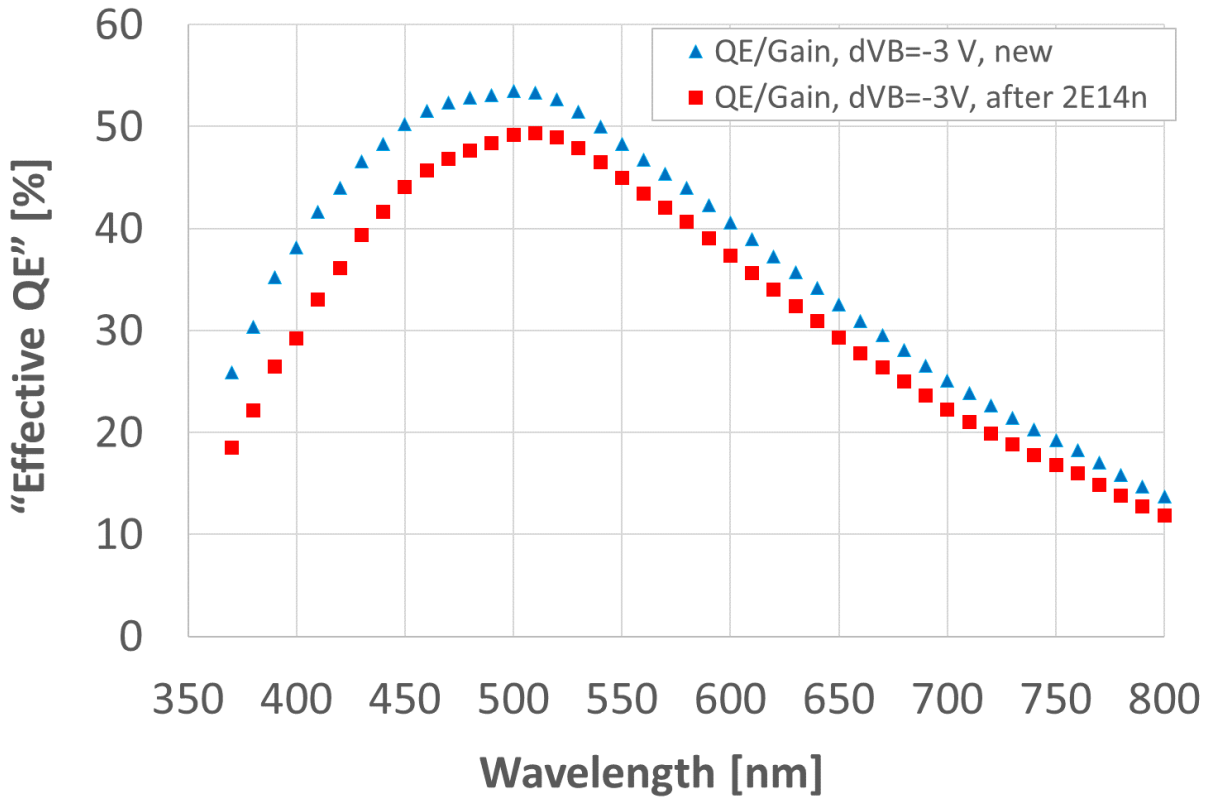




M. Wayne, A. Heering, Y. Musienko (ND)

R&D — SiPM QE after irradiation

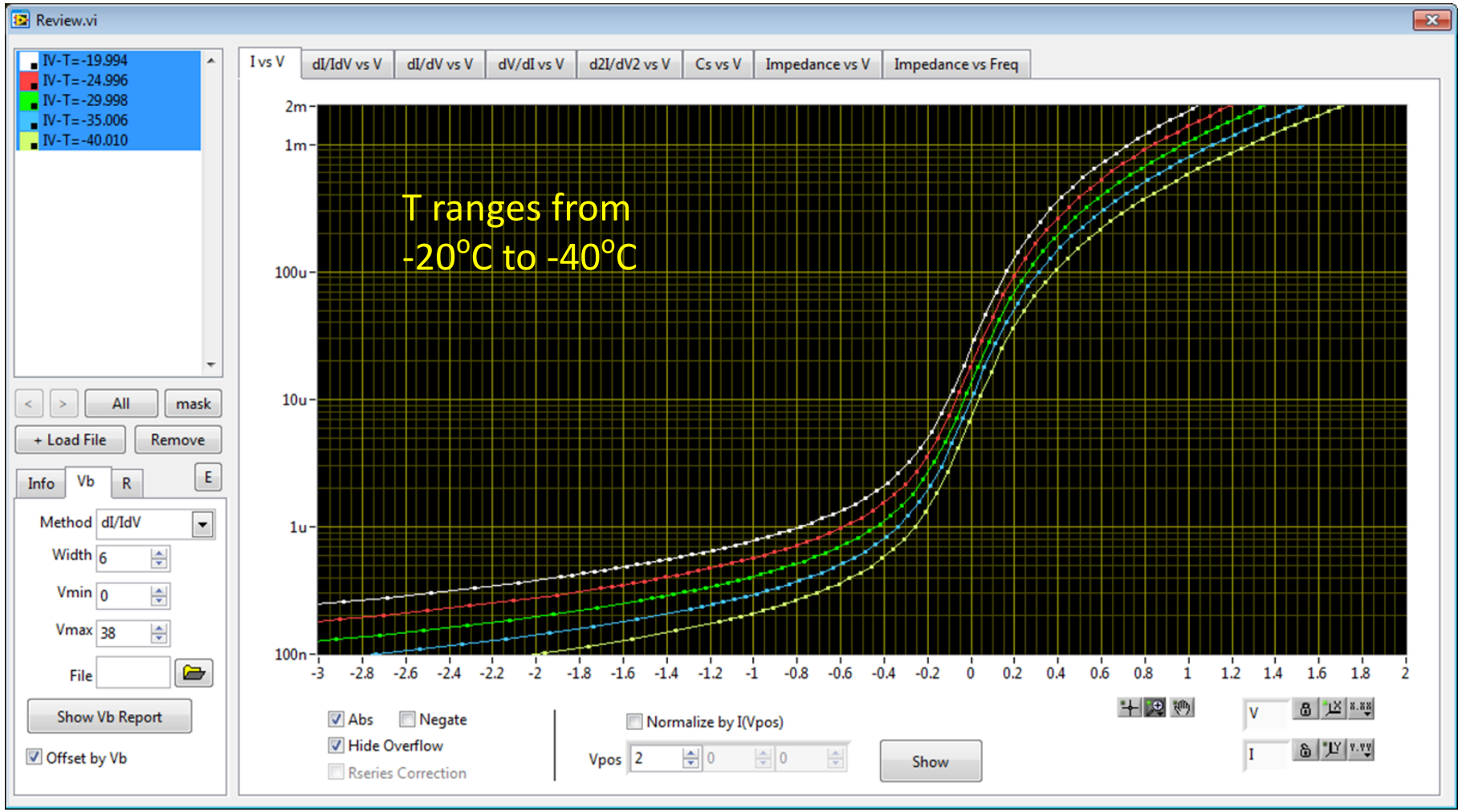
- Device under consideration is Hamamatsu HDR2-15µm.
- Observe 20% loss of QE after 2e14 neq/cm^2 including effect of glass window.
- Extrapolate less than 5% loss of QE for this device in CE-H conditions.



M. Wayne, A. Heering, Y. Musienko (ND)

R&D – SiPM noise

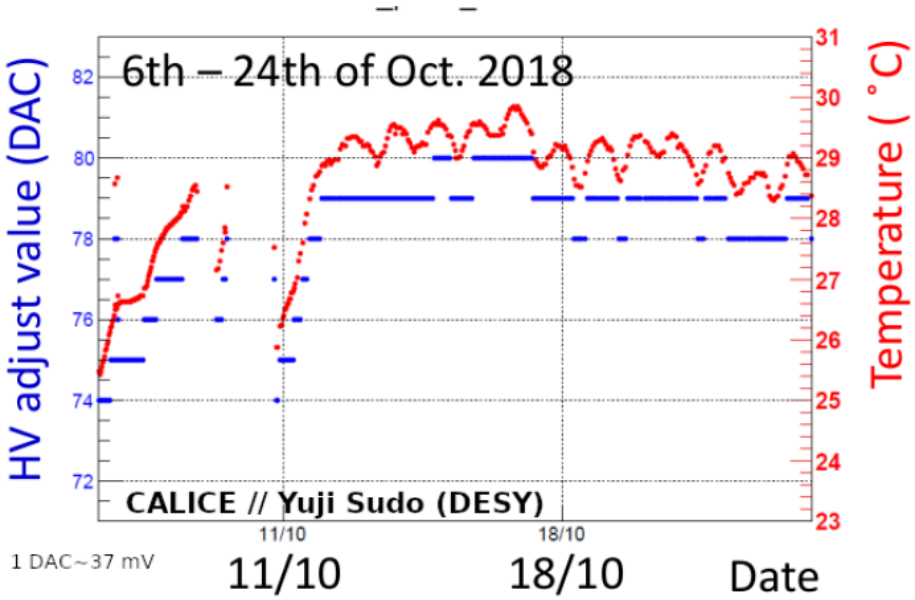
- DCR for HDR2-15µm after 5e13 neq/cm^2 is 5.4 GHz/mm^2 at -30 C — consistent with good MIP S/N at end-of-life



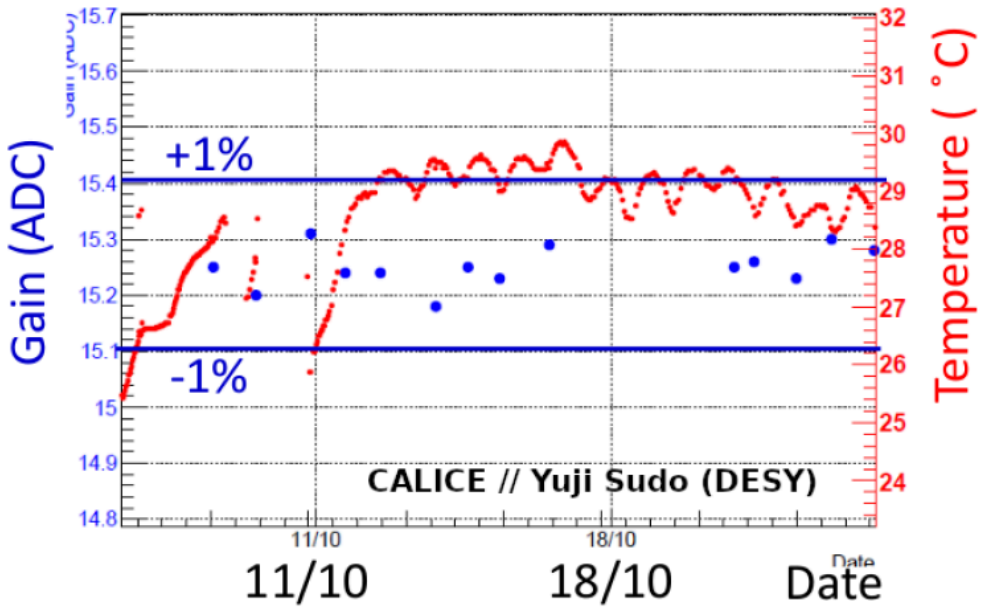
M. Wayne, A. Heering, Y. Musienko (ND)

R&D — SiPM gain stabilization vs. T

- SiPM gain stabilization via slow-control/software loop demonstrated by CALICE in testbeam.
  - Gain stability within 1% of nominal achieved despite 6 °C temperature swing in TB via adjustment of SiPM bias voltage.
- Propose to adopt a similar scheme in CE-H where typical temperature gradients are expected to be 2 °C.
  - PT1000 resistors on tileboard provide 0.1 °C temperature precision.
  - 1% stability can be achieved with a 10 mV precision (= 0.35 °C) in HGCROC bias circuit.



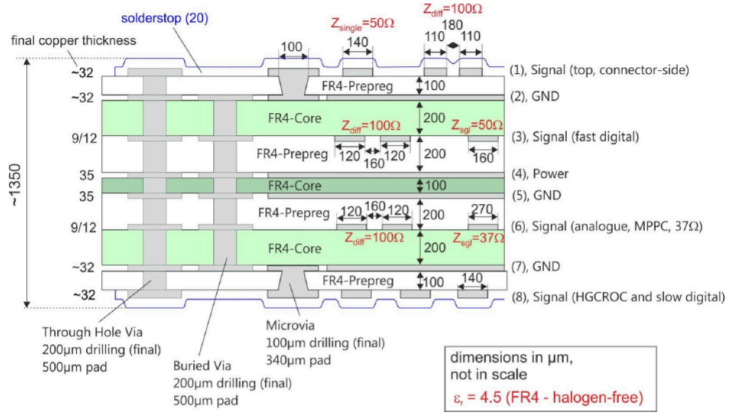
(a)

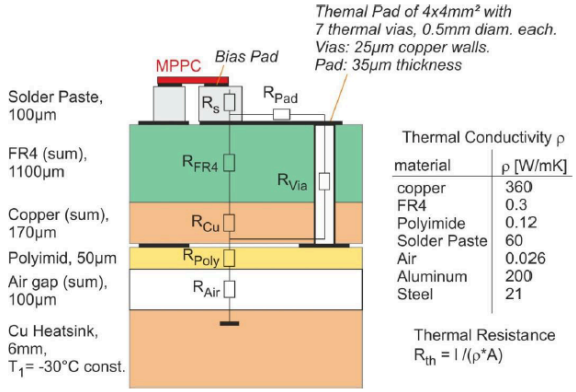


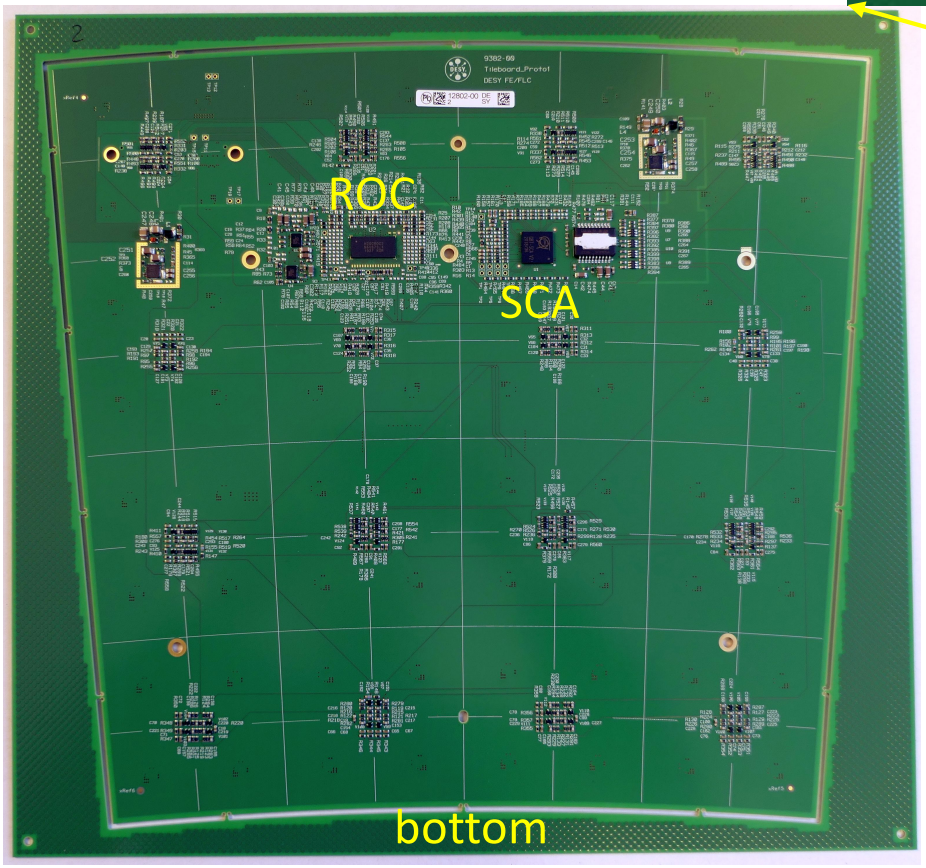
(b)

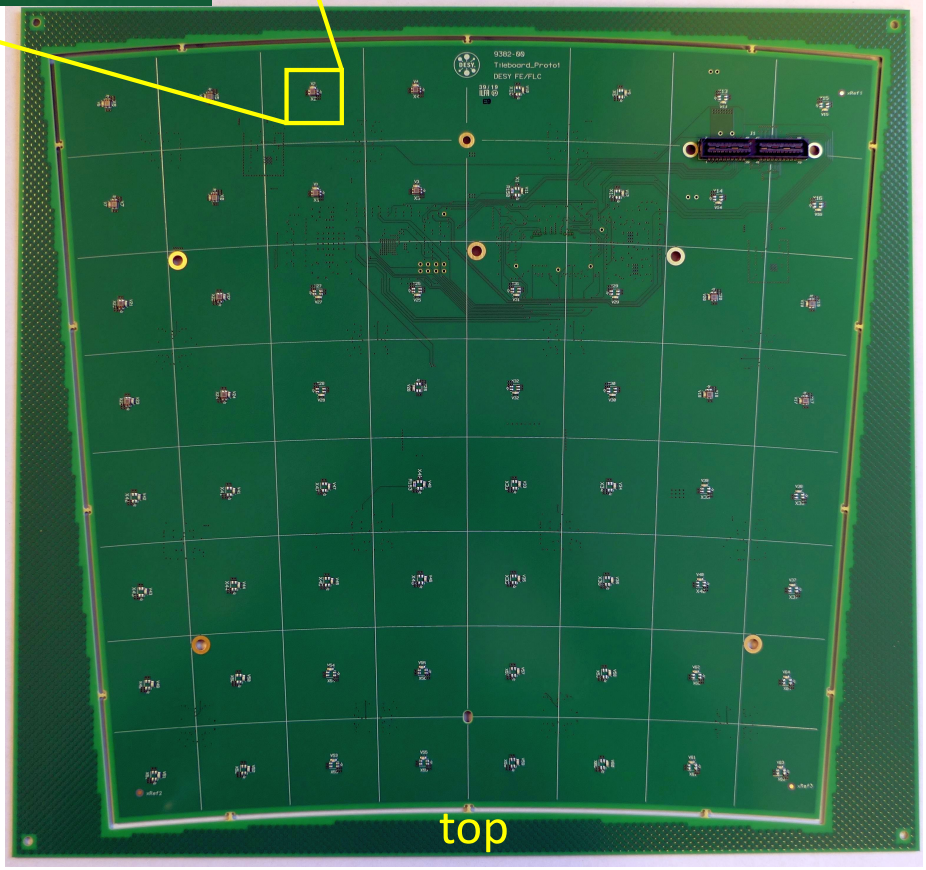
R&D — TB1 prototype tile module

M. Reinecke [DESY]



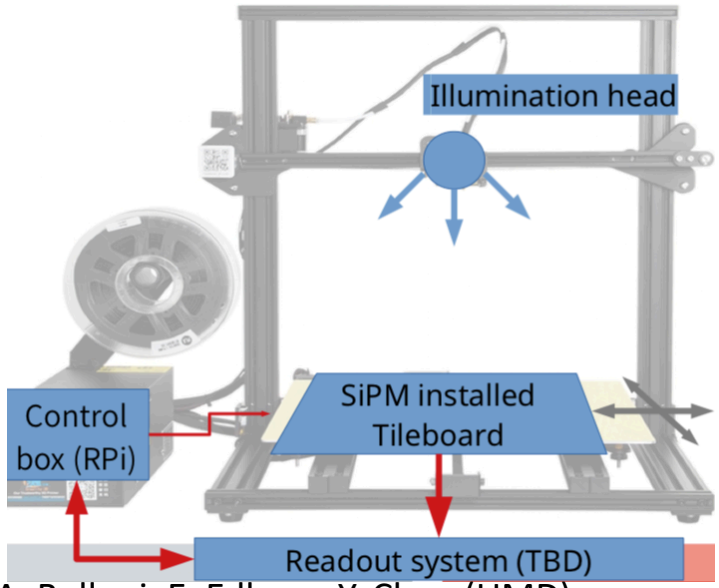


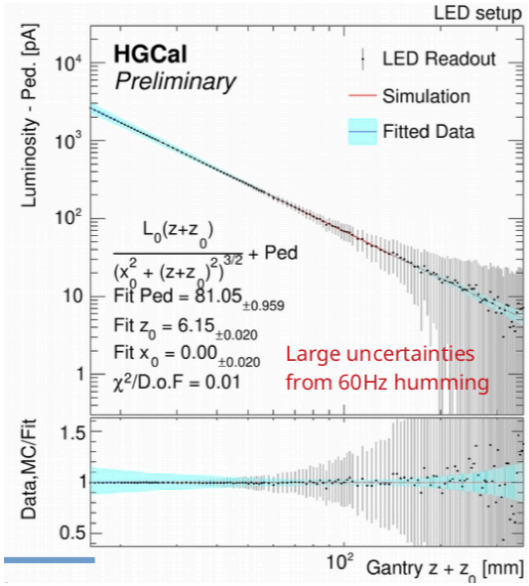


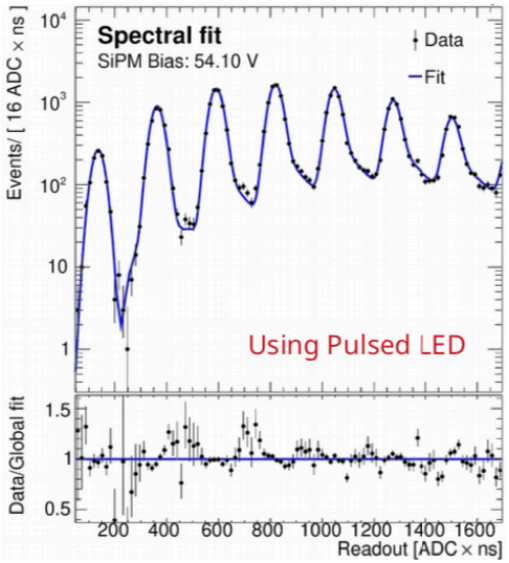


R&D — Tile module PCB QC

- Tile module PCBs will undergo QC before gluing of tiles to board.
  - Movable nano-second pulsed LED allows to illuminate SiPMs over the relevant dynamic range of more than 10^3.
  - Many parameters per SiPM can be extracted from a single spectrum measurement, including gain, common noise, cross-talk, after-pulsing, and dark current.





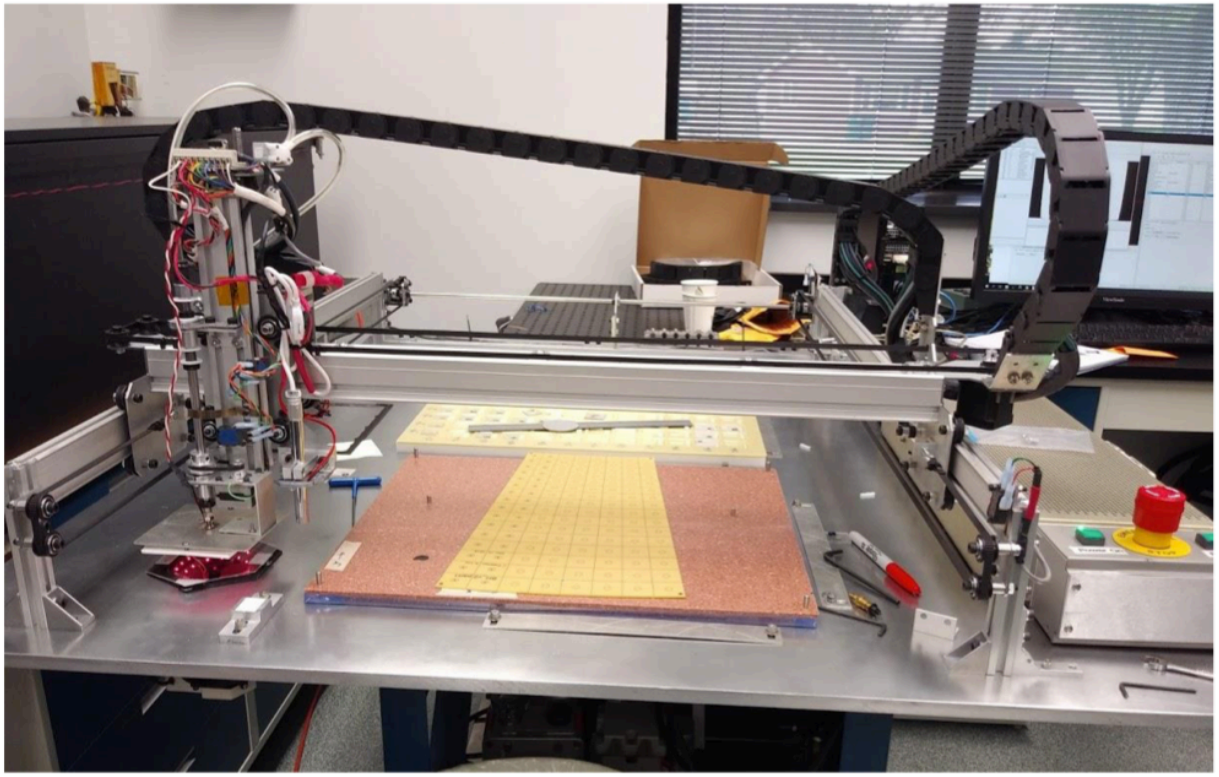


A. Belloni, E. Edberg, Y. Chen (UMD)

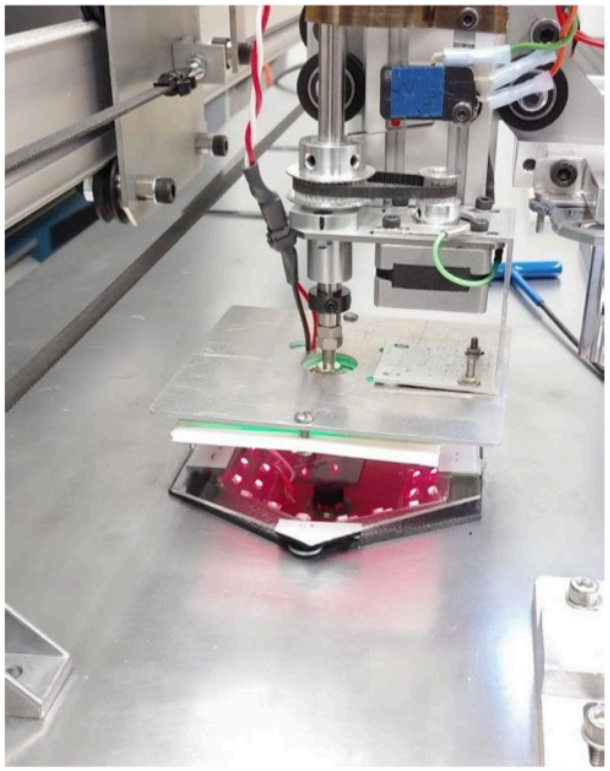
R&D — Tile module assembly

- Focus is on development of automated, highly repeatable procedures for module assembly.

PnP Machine → ready to use

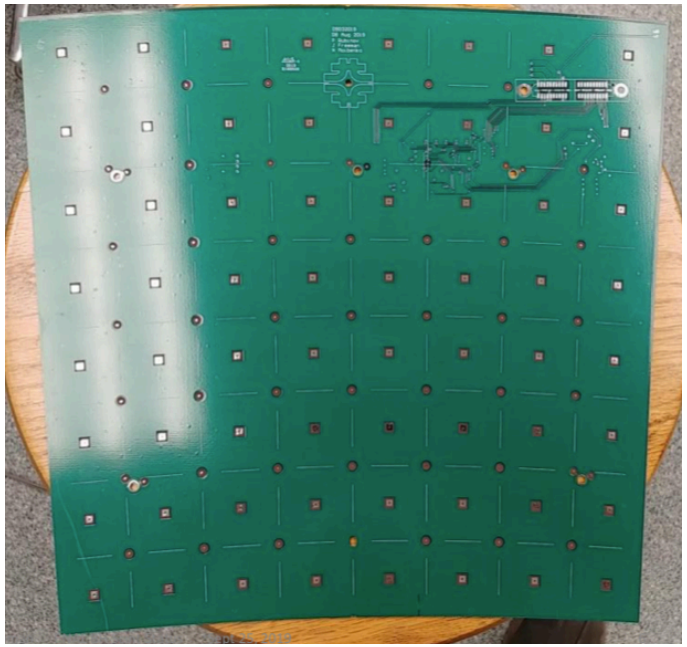


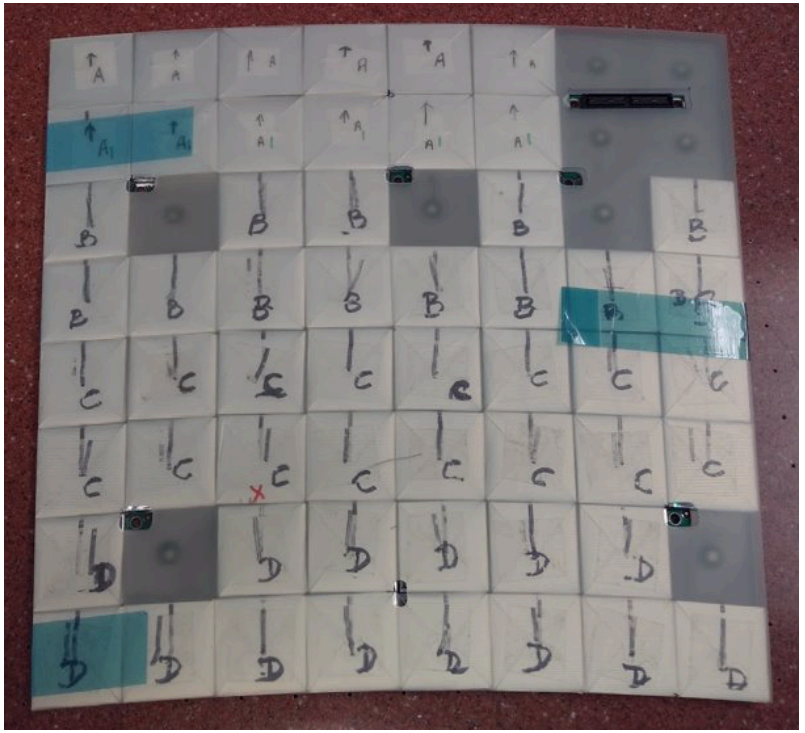
J. Freeman - FNAL

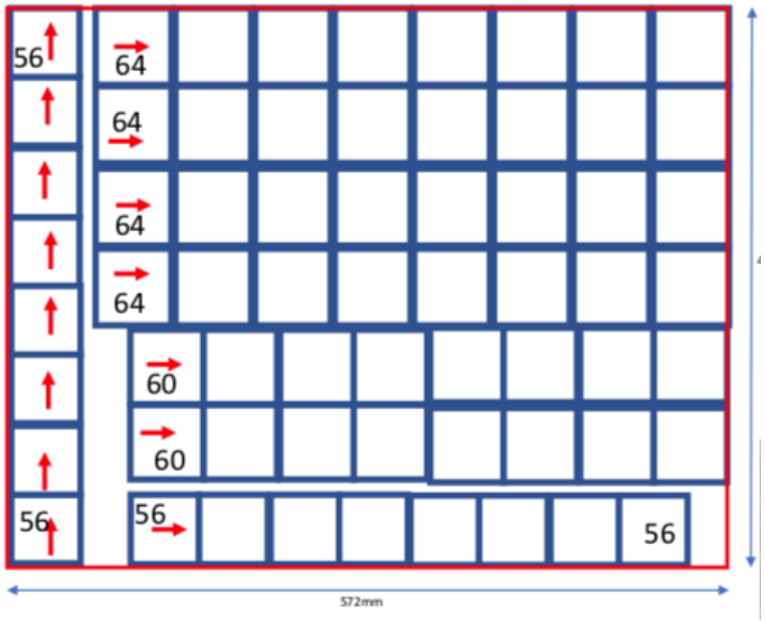


Bottom vision camera

R&D — Tile module assembly







1. Place cut Laird film on PCB
2. Align PCB to pick-and-place via alignment pins
3. Prepare tray with tiles for mounting
4. Remove Laird protective layer, machine places tiles on tacky Laird film
5. Transfer assembly to oven for 30 mins at 55C

Readiness for CD-2

- We are converging quickly on a baseline design. Preliminary design is nearly complete.
- Moving into final design phase.
  - Documenting interfaces & risks.
  - Producing detailed designs for all major components.
- We consider the design maturity for this WBS area to be appropriate for CD1 and advancing rapidly.
- To be done before CD-2: Firm up labor estimates which scale per tile/per channel.
  - Wrapping station: reduce uncertainty on labor requirements
  - Tile module assembly: reduce uncertainty on labor requirements
  - QC effort: what fraction of channels are subject to which QC tests? At what labor cost per channel?

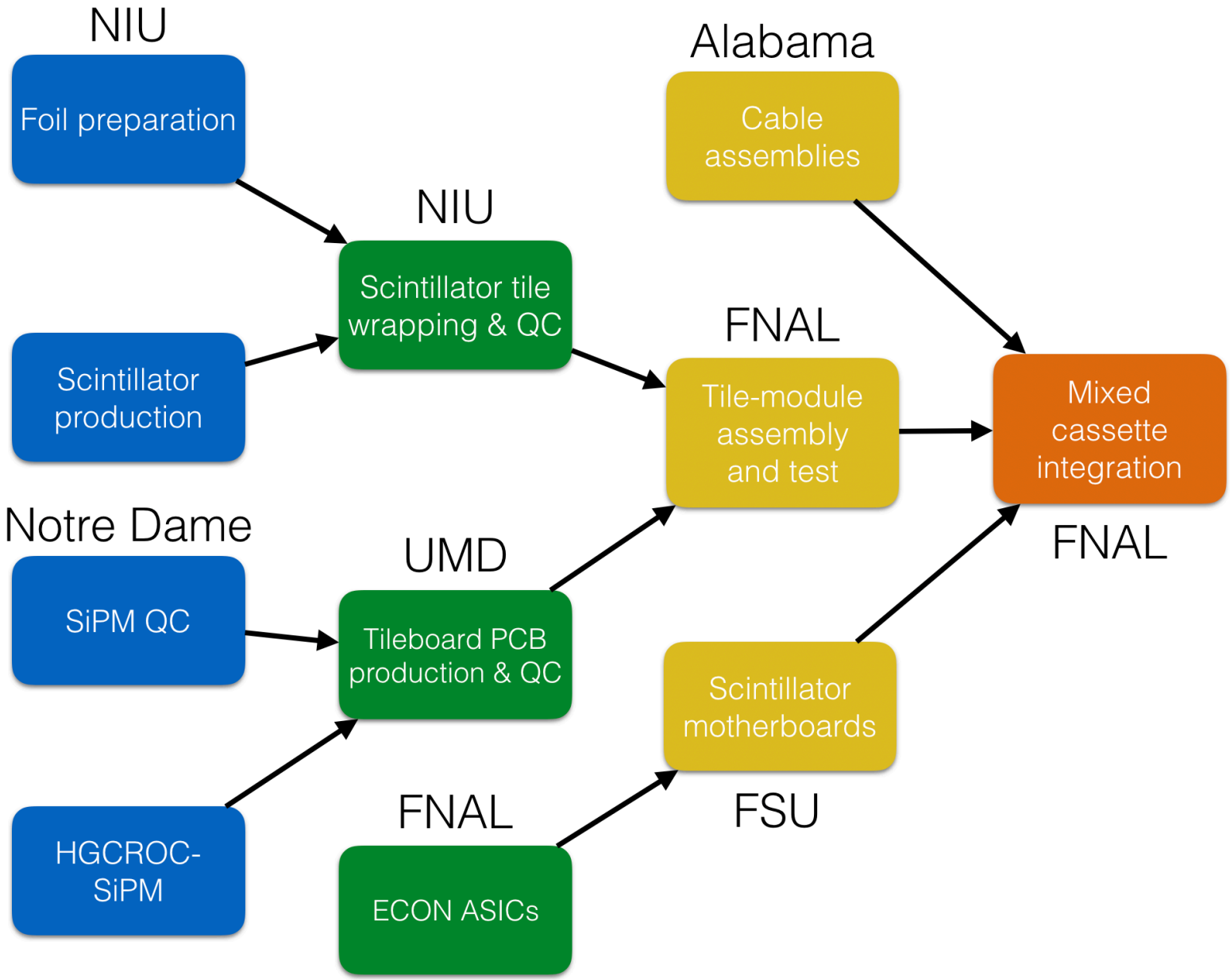
Quality Assurance and Quality Control

Charge #2

- QA/QC is a major focus of our effort:
  - NIU QC teststands for bare and wrapped tiles, building on source measurements devised for CALICE.
  - ND lab at CERN carries out a sophisticated suite of measurements on SiPMs, including after irradiation, which will be followed throughout the prototyping and production process.
  - UMD teststand for bare tile module PCBs, including detailed characterization of SiPM parameters.
  - FNAL group working on high accuracy automated assembly procedures along with QC steps e.g. verification of wrapped tile tolerances.
- QA/QC plans are sufficiently advanced for CD1 and advancing rapidly.

Cost and Schedule

Scintillator workflow

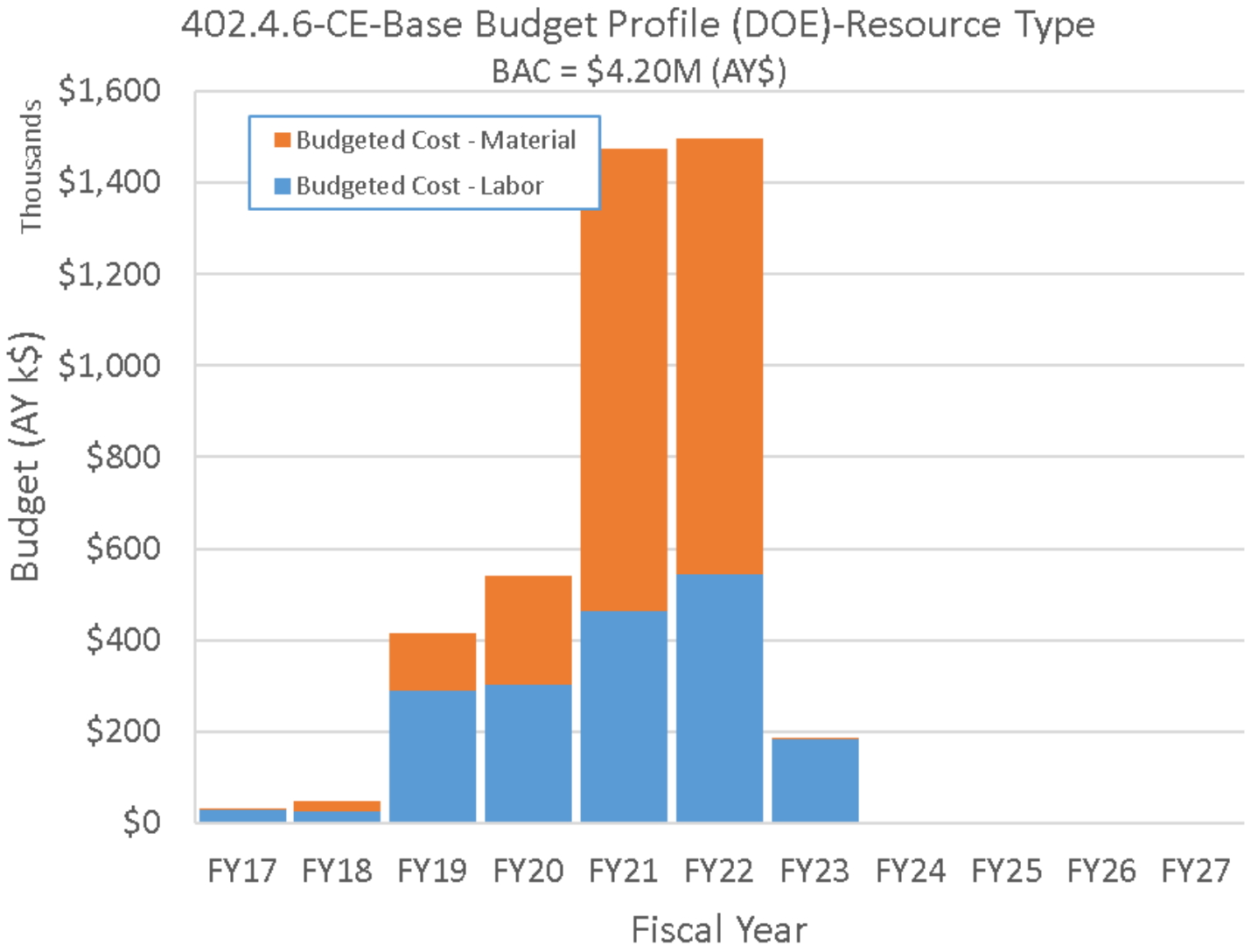


Costs: Scintillator Calorimetry

WBS	Direct M&S ($)	Labor (Hours)	FTE	Direct + Indirect + Esc. ($)	Estimate Uncertainty ($)	Total Cost ($)
DOE-CD1-402.4 402.4 CE - Calorimeter Endcap (at DOE CD1)	21,051,786	332579	188.11	40,672,474	10,143,585	50,816,059
DOE-CD1-402.4.6 CE - Scintillator Calorimetry	2,084,047	60875	34.43	4,196,710	1,244,785	5,441,494
DOE-CD1-402.4.6.1 CE - Scintillator Development and Prototyping	196,600	35180	19.90	620,811	104,856	725,667
DOE-CD1-402.4.6.2 CE - Scintillator Production	151,739	6550	3.70	411,442	120,802	532,244
DOE-CD1-402.4.6.3 CE - SiPM Photodetectors	896,000	4854	2.75	1,564,589	398,521	1,963,110
DOE-CD1-402.4.6.4 CE - Scintillator Tilemodules	369,323	10123	5.73	688,300	206,490	894,790
DOE-CD1-402.4.6.5 CE - Scintillator Motherboards	470,385	4168	2.36	911,568	414,116	1,325,684

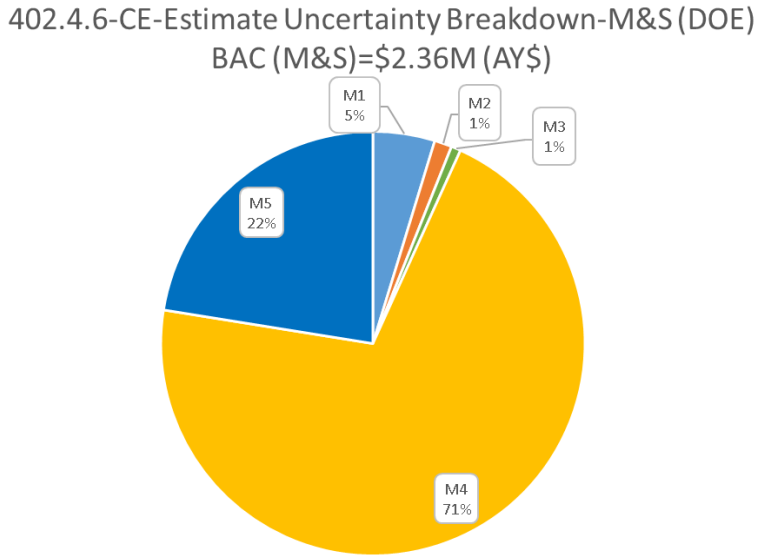
- Production SiPM purchase (~0.9 M$) is the largest single line item.
- Scintillator tile module production involves significant amounts of labor and M&S.
- Scintillator motherboards production involves large M&S costs for purchase of electronic components for motherboards.

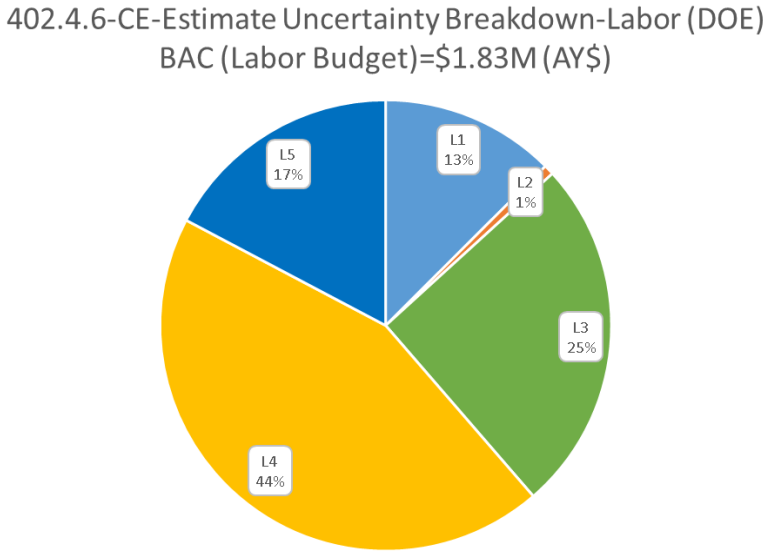
Fiscal Year Cost Profile



M&S — main production procurements in FY21-22
Labor less sharply peaked (staffing of tile QC, module assembly)

Contingency Breakdown





- Contingency breakdown is reasonable for this stage of the project.
- As baseline plans firm up for CD2, anticipate reductions of category 4 & 5 uncertainties.
  - E.g. better quality labor estimates for tile wrapping and board assembly.

Risks

Charge #3,5

RI-ID	Title	Probability	Cost Impact	Schedule Impact	P * Impact (k$)	P * Impact (months)
WBS / Ops Lab Activity : 402.4 CE - Calorimeter Endcap (16)						
Risk Rank : 3 (High) (2)						
RT-402-4-18-D	CE - Additional concentrator ASIC engineering (MPW) run is required	50 %	164 -- 241 -- 385 k$	6 -- 7.5 -- 9 months	132	3.8
RT-402-4-01-D	CE - Additional FE ASIC engineering run required	25 %	336 k$	8 months	84	2.0
Risk Rank : 2 (Medium) (6)						
RT-402-4-22-D	CE - Additional production acceleration required	20 %	564 -- 564 -- 777 k$	1 months	127	0.2
RT-402-4-91-D	CE - Shortfall in Calorimeter Endcap scientific labor	30 %	0 -- 0 -- 982 k$	0 months	98	0.0
RT-402-4-04-D	CE - Concentrator does not meet specifications	10 %	907 -- 971 -- 1035 k$	6 -- 7.5 -- 9 months	97	0.8
RT-402-4-90-D	CE - Key Calorimeter Endcap personnel need to be replaced	25 %	75 -- 225 -- 555 k$	0 -- 0 -- 3 months	71	0.3
RT-402-4-02-D	CE - Infrastructure failure at module assembly facility	30 %	100 -- 336 k$	1 -- 4 months	65	0.8
RT-402-4-13-D	CE - HGCROC front end chip is delayed	20 %	21 -- 126 -- 252 k$	1 -- 6 -- 12 months	27	1.3
Risk Rank : 1 (Low) (8)						
RT-402-4-23-D	CE - Si Motherboard complexity is much higher than expected	5 %	383 -- 575 -- 767 k$	0 months	29	0.0
RT-402-4-16-D	CE - Cassettes damaged or lost in assembly, testing or shipping	5 %	100 -- 1000 k$	3 months	28	0.2
RT-402-4-15-D	CE - Motherboard and interface board fabrication failure	10 %	73 -- 193 k$	3 months	13	0.3
RT-402-4-20-D	CE - Boundary between Si and scintillator sections is moved	5 %	252 k$	0 months	13	0.0
RT-402-4-17-D	CE - Cassette assembly site failure	10 %	73 -- 163 k$	3 months	12	0.3
RT-402-4-09-D	CE - Module PCB batch failure	5 %	144 -- 186 k$	2 -- 4 months	8	0.2
RT-402-4-14-D	CE - Cassette cooling plate fabrication failure	10 %	73 -- 83 k$	3 months	8	0.3
RT-402-4-10-D	CE - Silicon sensor has low yield	1 %	542 -- 784 k$	2 -- 4 months	7	0.0

Schedule Overview

Schedule is organized into three major phases:

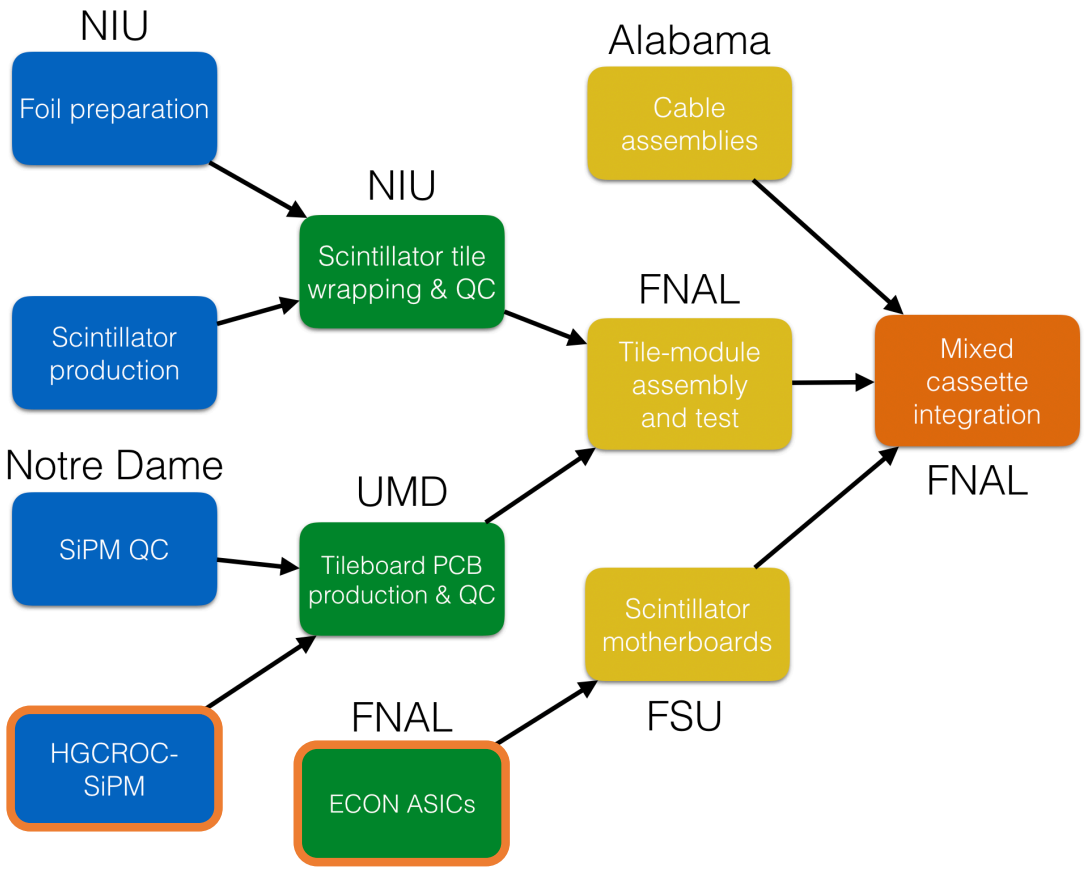
- Mockups/R&D phase — concluding:
  - Few input dependencies (no use of common components).
  - Focused on answering outstanding questions to validate the design and choose amongst remaining options.
  - Successful mockup and R&D positions us to produce scintillator prototypes during next phase.
- Prototyping phase — FY19-21:
  - Validate design by constructing two prototype cycles with as close to final components as available.
  - Requires results of mockup/R&D program.
  - Some external inputs (HGCROC and ECON prototypes).
  - Successful completion of prototypes campaign positions us to begin production of final components.
- Production phase — FY21-23:
  - Produce final production components based on outcome of prototype program.
  - Requires final versions of HGCROC and ECON.

Milestones for 402.4.6

- Milestones exist to track the progress of tile-modules and motherboards through the prototype and production process.
- SiPM activities are tied to milestones through the tile—module activities.
- Major milestones to watch:
  - Set of milestones for completion of R&D activities needed for CD-2 readiness.
  - Successful completion of the prototype campaign in each WBS area is required to start production activities, will monitor prototype schedule closely.

ASICs schedule risks

- Tile module PCBs require the final HGCROC in order to go ahead with production.
  - Tile preparation/wrapping are in parallel with module PCB production and should not be affected.
  - Current SiPM QC plans involve measuring them in-situ on the tile module PCB — so delays in HGCROC can eventually affect SiPM production flow.
  - Tile module assembly could potentially be accelerated by doubling the machinery and tooling at the assembly site.
- Motherboards require concentrator ASIC.
  - Delays to concentrator ASIC availability will impact scintillator section similarly to the silicon section.
- HGCROC enters earlier in the chain and has more potential for knock-on effects.



Critical Path items for 402.4.6

Charge #5

- Some scintillator activities are close to the critical path.
- Take precautions to avoid slippage in the tile module production schedule as this depends on availability of HGCROC, and would begin to affect cassette assembly if substantially delayed.
- Cassette assembly also requires production motherboards, which depend on ECON ASICs.
  - Motherboard assembly is likely easier to accelerate than tile modules, due to fewer external dependencies.

Contributing Institutions and Resource Optimization

Contributing Institutions

Charge #3

- Alabama: cable assemblies and adapters (Henderson)
- FNAL: testbeam program (Freeman, Lincoln), mockup and prototype mixed cassettes, cassette assembly site
- FSU: motherboard design, LED system, L3/L4 manager scintillator/motherboards (Kolberg)
- UMD: scintillator studies, irradiation campaign, tile PCB QC (Belloni, Eno)
- UMN: readout system design, int'l scintillator mgmt (Mans), EE (Frahm)
- NIU: individual tile production (Dyshkant), tile board assembly and wrapping, L4 manager tiles (Zutshi)
- ND: SiPMs (Heering, Musienko), L4 manager (Wayne)

Resource Optimization

Charge #3

- Tile-modules
  - Re-use existing test infrastructure at NIU (NICADD) for tile boards.
  - Use injection molded tiles where possible in order to cut costs of labor-intensive machining of cast scintillator. Use affordable commercial injection molding.
  - Import automated assembly techniques from CALICE in order to use cost-effective commercial pick and place systems in place of technician labor.
- SiPMs
  - Re-use test infrastructure and expertise of ND group at CERN in order to minimize SiPM engineering cost.
- Motherboards
  - Re-use of common components (ECON, lpGBT/GBT-SCA, VTRX+, …).

ES&H

Charge #4

- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394)
- In General Safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW
- No unique hazards in this WBS area.

Summary

- We have identified a cost effective and robust technology (SiPM-on-tile) for hadronic calorimetry using plastic scintillator and silicon photomultipliers for the endcap region at HL-LHC.
- R&D program is in place, largely completed, and paced to answer remaining questions before prototypes are built.
  - CD-2 readiness is our target as we wrap up R&D phase.
- Prototype program is in place to test production methods and performance of assembled detector.
- Cost and schedule are understood and under control for a project at CD-1 phase.
  - Risks are identified and appear manageable.
  - Paying close attention to parts of the workflow which are near the critical path.
- Strong team in place that is excited to apply this technology at HL-LHC.

Backup

Design Considerations for 402.4.6

Scintillator calorimetry in endcap is needed to meet scientific requirements for the endcap:

- Choice of scintillator and photodetector driven by calibration requirements (EC-sci-engr-001).
- SiPM-on-tile technology allows us to instrument full detector depth of ~10 hadronic interaction lengths in a cost effective way (EC-sci-engr-005). Results in longitudinal granularity (EC-sci-engr-002).
- Tile size is chosen to limit the negative effects of HL-LHC radiation dose, allowing good resolution jet and MET measurements even at end of life (EC-sci-engr-006). Results in transverse granularity (EC-sci-engr-002).
- Resulting design has positive effects for pileup mitigation (EC-sci-engr-007).

Charge #2

Conceptual design – tile modules

Layer Overview: No. Channels and ROCs, Dimensions.

This is for "second optimization". The outer rings in FH are not included in ASCII table on tab "Layer_Data" (BV currents!). Some inner rings deleted.

CE-H: layers FH 9-12 (36 to 39)

r [mm], inner	ring	9	10	11	12
		36	37	38	39
2179.20	34				
2132.67	33				
2086.15	32			56chns 1HGCROC 302x372mm²	64chns 1 HGCROC 349x380mm²
2041.61	31		48chns 1HGCROC 256x364mm²		
1997.08	30				
1954.44	29	32chns 1HGCROC 167x348mm²			
1911.80	28		F6	F7	F8
1870.99	27				
1830.17	26	F4			
1791.10	25				
1752.03	24	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²
1714.62	23				
1677.22	22				
1641.41	21				
1605.60	20	D8'	D8'	D8'	D8'
1571.33	19				
1537.05	18				

10 degree Tileboard, 1.25° tiles

not assembled

Connector/HGCROC Pos.

A6 - Board Type

4mm² SiPM

2mm² SiPM

CE-H: layers BH 13-22 (40 to 49)

r [mm], inner	ring	13	14	15	16 -18	19 -21	22
		40	41	42	43, 44, 45	46, 47, 48	49
2594.79	42						
2539.39	41						
2483.99	40						
2430.96	39			56chns 1HGCROC 360x443mm²	64chns 1 HGCROC 416x452mm²	64chns 1 HGCROC 416x452mm²	48chns 1HGCROC 305x433mm²
2377.93	38						
2327.16	37		40chns 1HGCROC 251x424mm²				
2276.40	36	24chns 147x406mm²					
2227.80	35		G5	G7	G8	G8	G6
2179.20	34	G3					
2132.67	33						
2086.15	32	64chns 1 HGCROC 349x380mm²	64chns 1 HGCROC 349x380mm²	64chns 1 HGCROC 349x380mm²	64chns 1 HGCROC 349x380mm²	64chns 1 HGCROC 349x380mm²	64chns 1 HGCROC 349x380mm²
2041.61	31						
1997.08	30						
1954.44	29						
1911.80	28	E8	E8	E8	E8	E8	E8
1870.99	27						
1830.17	26						
1791.10	25						
1752.03	24	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²	64chns 1 HGCROC 293x319mm²
1714.62	23						
1677.22	22						
1641.41	21						
1605.60	20	D8	D8	D8	D8	D8	D8
1571.33	19						
1537.05	18						
1504.23	17						
1471.42	16	40chns 1HGCROC 159x268mm²	40chns 1HGCROC 159x268mm²	96chns 2 HGCROCs 354x268mm²	96chns 2 HGCROCs 354x268mm²	96chns 2 HGCROCs 354x268mm²	96chns 2 HGCROCs 354x268mm²
1440.00	15						
1408.59	14						
1378.52	13	C5	C5				
1348.45	12						
1319.66	11						
1290.87	10						
1263.31	9			B11 / B12	B11 / B12	B12	B12
1235.75	8						
1209.37	7						
1182.99	6						
1157.73	5						
1132.48	4					48chns 1HGCROC 145x206mm²	48chns 1HGCROC 145x206mm²
1108.30	3						
1084.12	2						
1060.98	1					A5 / A6	A5 / A6
1037.83	0						

SiPM area subject to change—
One possible scenario pictured

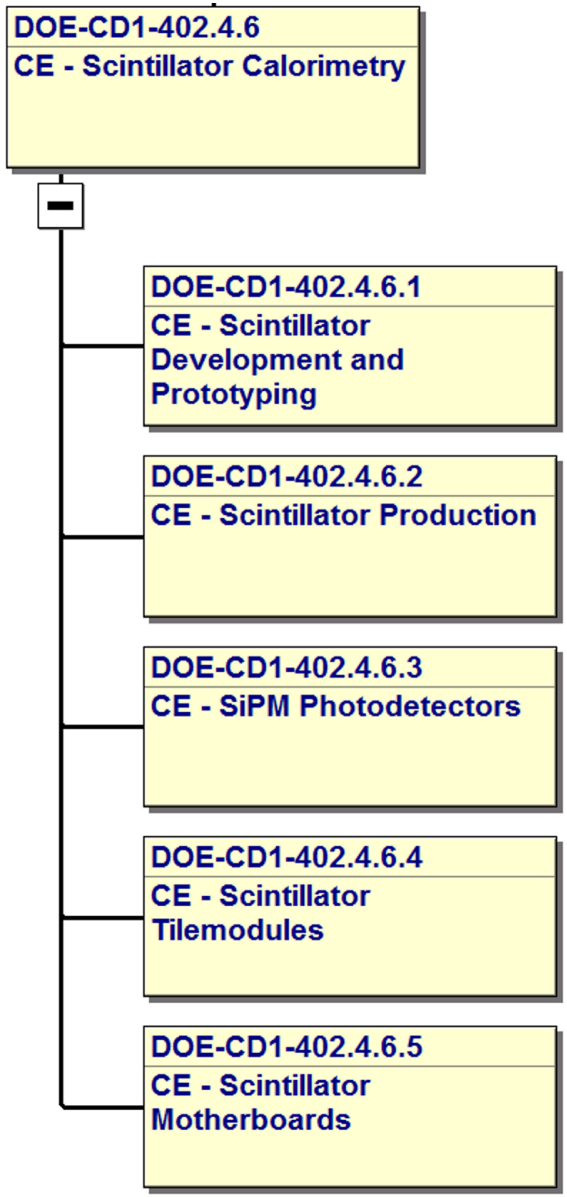
SiPM R&D - Summary of results

Overvoltage	1.0 volts	1.5 volts
Operating Voltage	37.5 volts	38 volts
Dark Current	117 μA/mm^2 before annealing	~240 μA/mm^2 before annealing
Power consumption	4.5 mW/mm^2 before annealing	~9.1 mW/mm^2 before annealing
Operating Temperature	-30°C	-30°C
Peak excitation wavelength	410 nm	410 nm
PDE before irradiation	21%	25%
Gain	1.34 x 10^5	1.83 x 10^5
% loss at entrance window	≤ 4%	≤ 4%
% loss of intrinsic QE	≤ 5%	≤ 5%
Dark count rate	5.4 x 10^9/mm^2 before annealing 2.7 x 10^9/mm^2 after annealing	~8.2 x 10^9/mm^2 before annealing ~4.1 x 10^9/mm^2 after annealing
Loss of PDE due to occupancy	≤ .25% before annealing	≤ .4% before annealing
Loss in PDE from self-heating	.07% before annealing for 2x2 mm^2	~.14% before annealing for 2x2 mm^2
Shift in breakdown voltage	≤ 0.5 volts	≤ 0.5 volts
S/N for ~3100 photon input	28.5	25.5

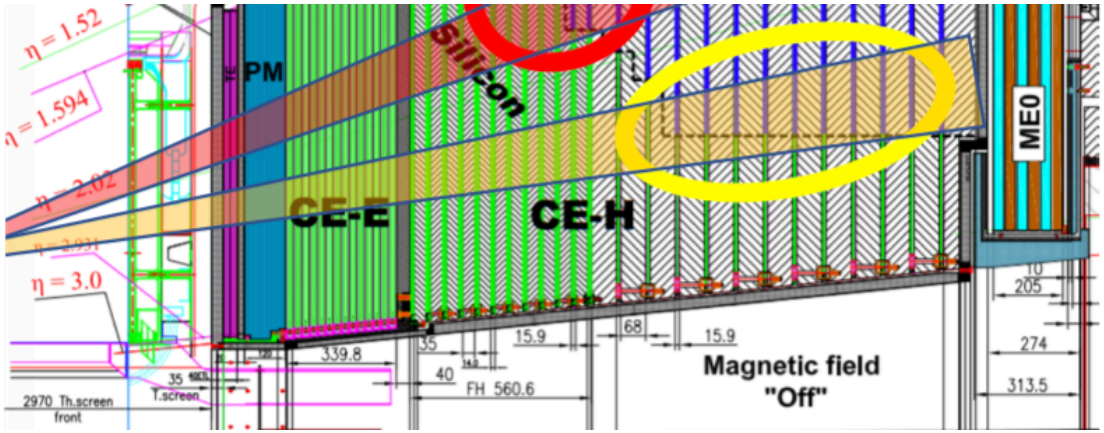
M. Wayne, A. Heering, Y. Musienko (ND)

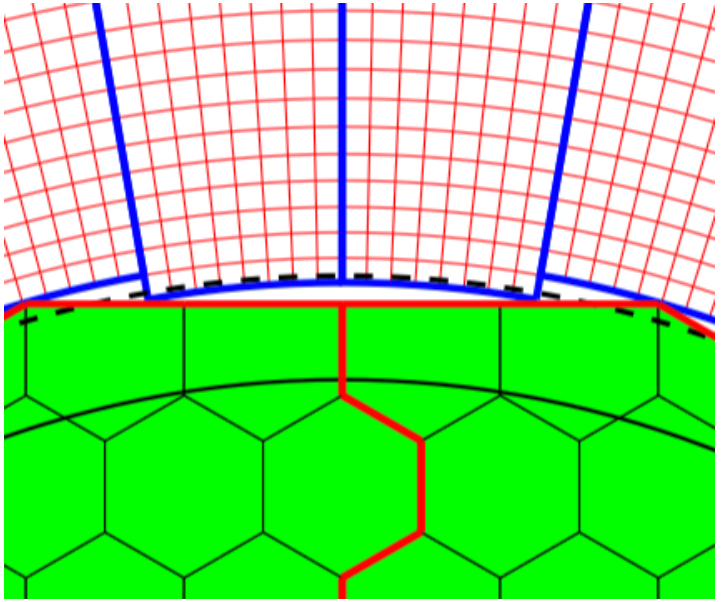
402.4.6 WBS Structure

- See slides 10-12 for deliverables coming from each WBS area.



Quantifying impact of Si-scint 'gap'





Single pions in eta range marked in yellow show a negligible increase in energy resolution upon turning off an additional ring of tiles in every layer.

[B. Caraway (Baylor)]