University of Pennsylvania

David Rivera

ICEBERG WIB Firmware

WIB

Currently:

- receives system clock timing and control signals from the timing system and provided processing and fan-out to the four FEMBs.
- Receives high-speed data from up to four FEMBs (1.28Gbps/FEMB)
- Bandwidth requirement:
- $8\frac{ADC}{FEMB}\times16\frac{ch}{ADC}\times2\frac{Bytes}{sample}\times\frac{10b}{8b}\times2M\frac{sample}{s}\times4\frac{links}{FEMB}=1280Mbps$ = 1.28Gbps

Data Processing

- 8b10b encoded data from FEMB (1.28Gbps) data lines
- Data is decoded at the WIB, error codes are tallied and stripped
- Data is repackaged 8:32 RAM and re-encoded (custom for high speed transfers)
- Timestamp and error counter values reported in header to downstream DAQ along with the data

Changes

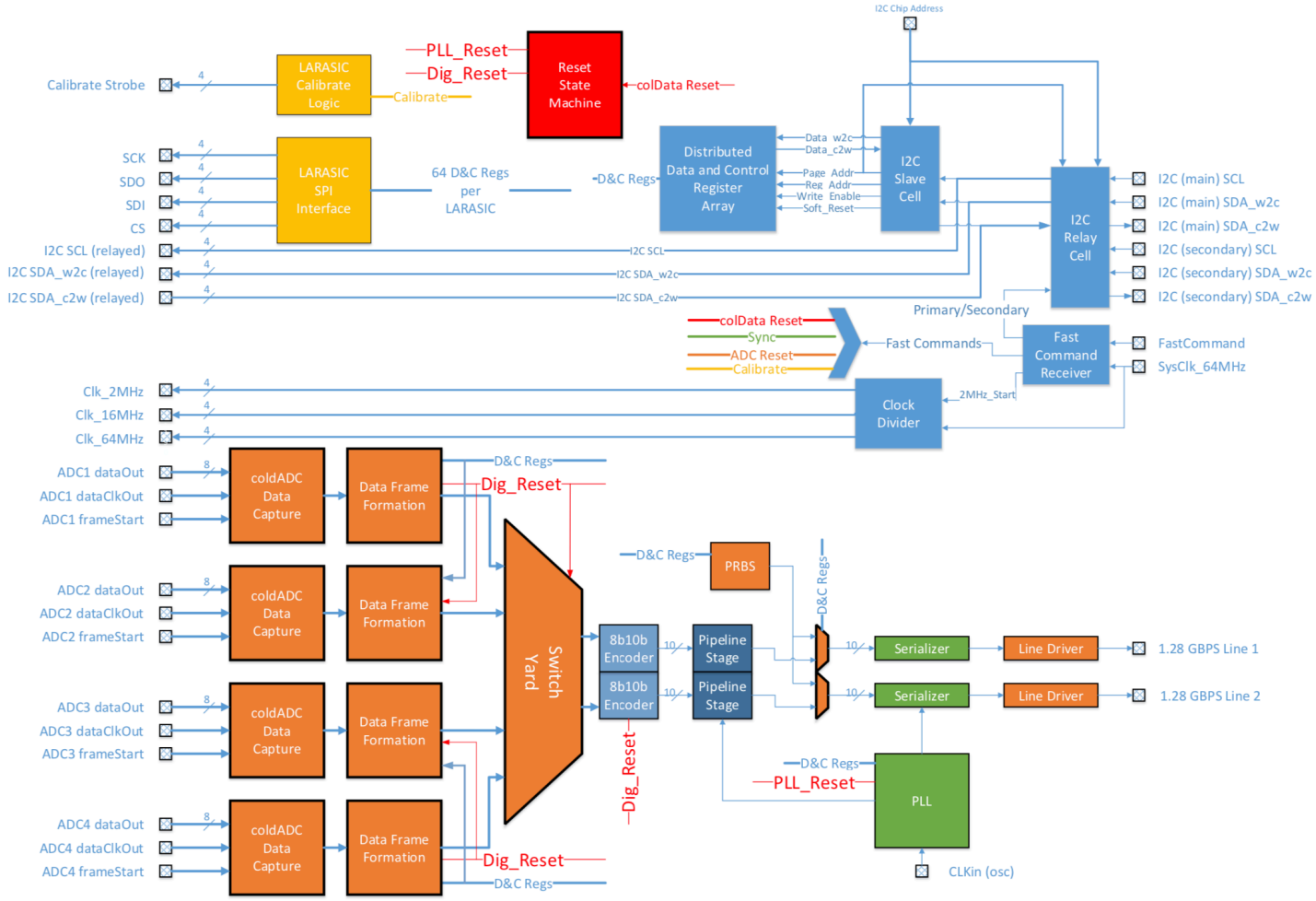
- Adapt existing WIB firmware to enable multiple readout chains for new ASICs
  - Variants include:
    - LArASIC + ColdADC (P1) + cold FPGA
    - LArASIC + ColdADC (P2) + 2 COLDATA
    - SLAC CRYO chip (All-in-one: FE, ADC, Data Serializer)
    - LArASIC + COTS ADC + cold FPGA (a la SBND)
- New timing and run control interface requirements
  - 64MHz system clock
  - FastCommand
- Substitute Altera-specific firmware (e.g. Triple Speed Ethernet, altera_xcvr, etc.) to Xilinx/ZYNQ equivalents.

Timing

- Current readout chains operate with a 50MHz system clock
- Firmware will be adapted to operate on the new system clock frequency

FastCommand Integration

- The WIB FPGA must translate the external DUNE Timing System control protocol to FastCommands for the Cold Electronics
- FastCommand is the serial command interface between WIB and COLDATA
- Designed to operate the core functionalities of the COLDATA chip (e.g. sync, reset, calibrate) in a timely manner



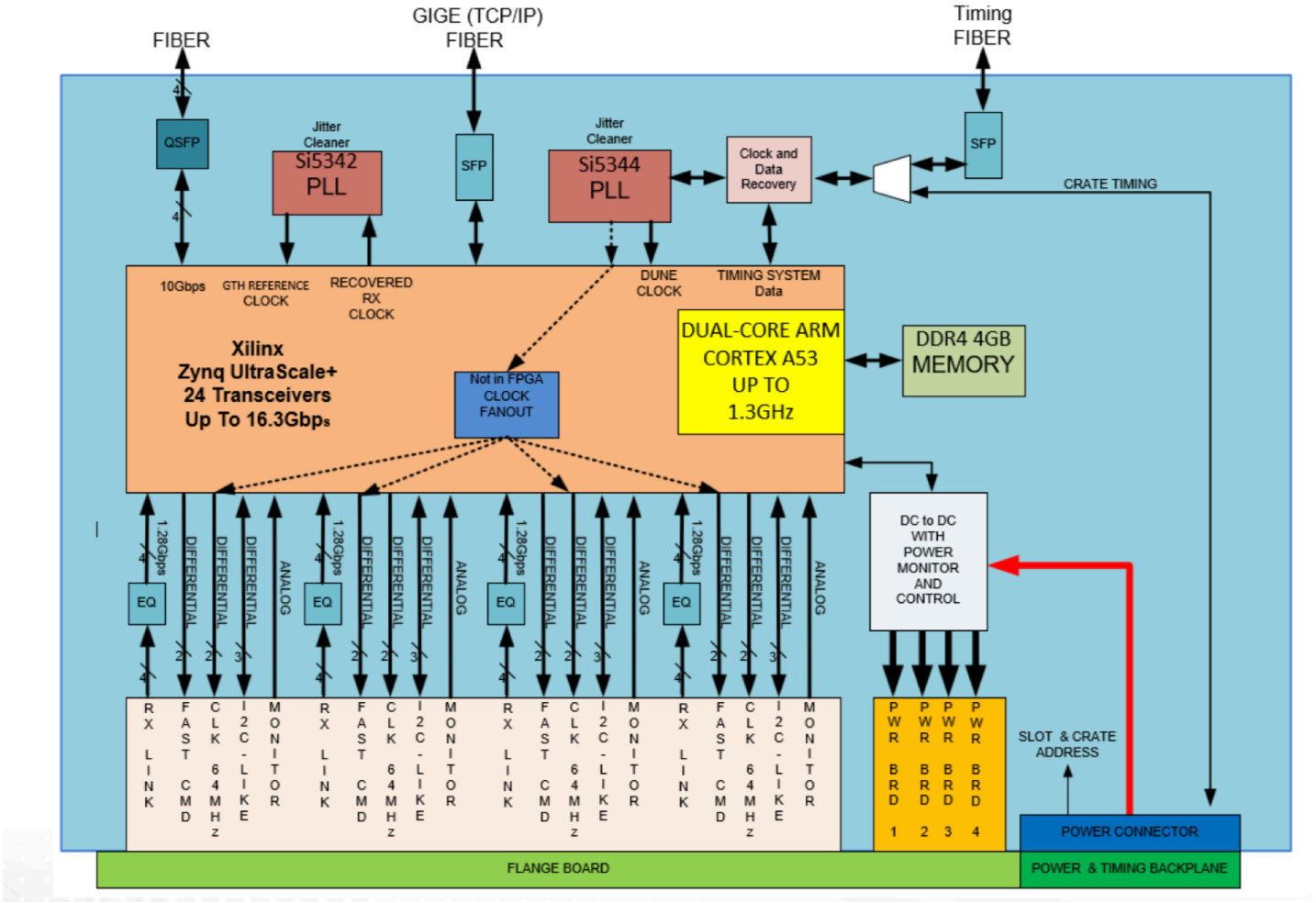
[Docdb-7232]

DUNE I2C

- Utilized with COLDATA ASIC
- 3-word variant on the canonical I2C protocol
- Chip/page address, register address, data (as opposed to just the latter two)
- Must reassign one JTAG signal pair to be used for DUNE I2C (cold to warm)
  - 4 JTAG lines will no longer be necessary for COLDATA
- May have to assign two sets of I2C for test board to account for missing wire bond to 4th address input pad on COLDADC (see Comments on I2C used by COLDATA and COLDADC)

ICEBERG WIB

- New version of WIB to be utilized in future ASIC validation tests at FNAL
- Altera Arria V -> Zynq UltraScale+

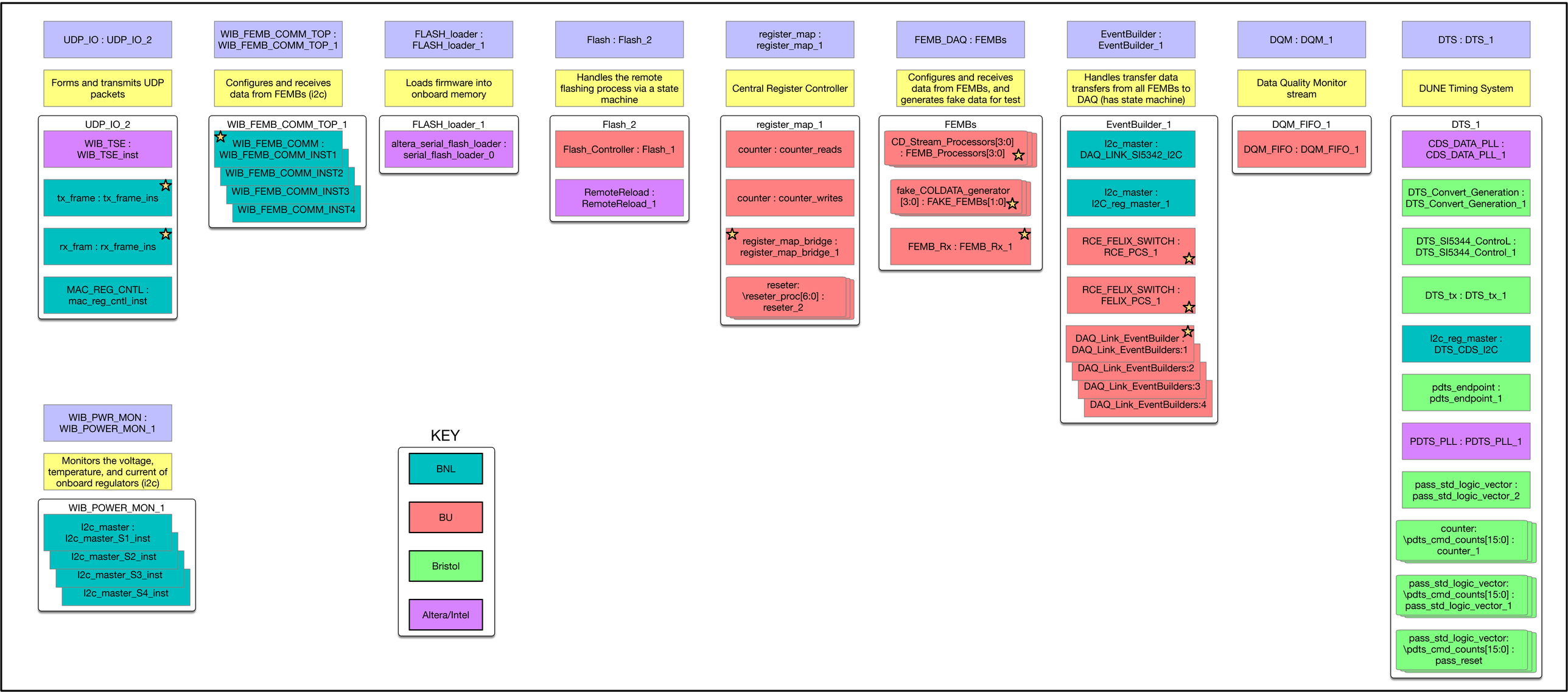


[Indico]

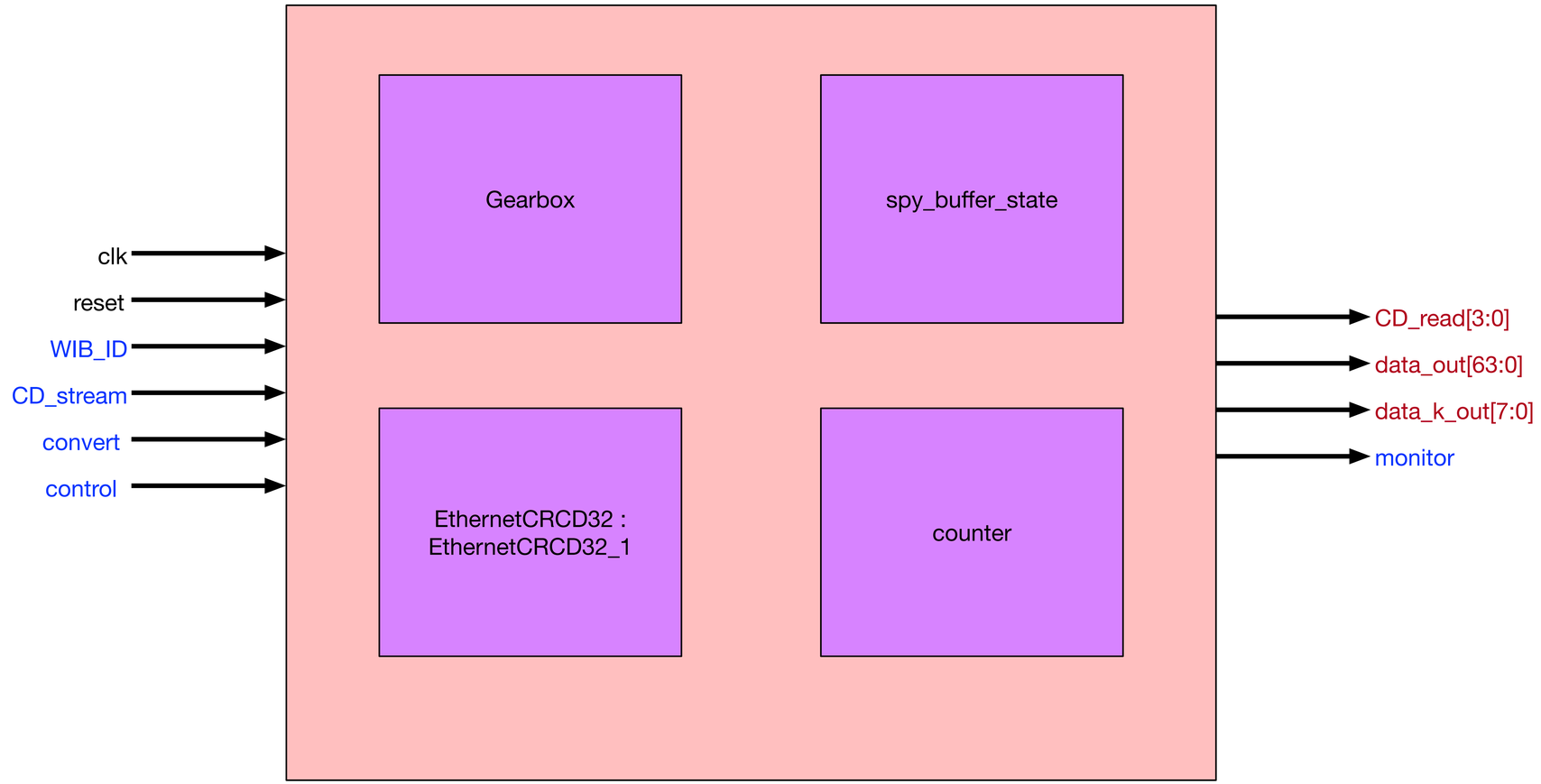
Questions

- ZU6CG variant?
- WIB Onboard memory for firmware?
  - SD slot?

WIB_TOP


UDP_IO : UDP_IO_2
Forms and transmits UDP packets
UDP_IO_2
WIB_TSE : WIB_TSE_inst
tx_frame : tx_frame_ins
rx_fram : rx_frame_ins
MAC_REG_CNTL : mac_reg_cntl_inst
WIB_FEMB_COMM_TOP : WIB_FEMB_COMM_TOP_1
Configures and receives data from FEMBs (i2c)
WIB_FEMB_COMM_TOP_1
WIB_FEMB_COMM : WIB_FEMB_COMM_INST1
WIB_FEMB_COMM_INST2
WIB_FEMB_COMM_INST3
WIB_FEMB_COMM_INST4
FLASH_loader : FLASH_loader_1
Loads firmware into onboard memory
FLASH_loader_1
altera_serial_flash_loader : serial_flash_loader_0
Flash : Flash_2
Handles the remote flashing process via a state machine
Flash_2
Flash_Controller : Flash_1
RemoteReload : RemoteReload_1
register_map : register_map_1
Central Register Controller
register_map_1
counter : counter_reads
counter : counter_writes
register_map_bridge : register_map_bridge_1
reseter: \reseter_proc[6:0] : reseter_2
FEMB_DAQ : FEMBs
Configures and receives data from FEMBs, and generates fake data for test
FEMBs
CD_Stream_Processors[3:0] : FEMB_Processors[3:0]
fake_COLDATA_generator [3:0] : FAKE_FEMBs[1:0]
FEMB_Rx : FEMB_Rx_1
EventBuilder : EventBuilder_1
Handles transfer data transfers from all FEMBs to DAQ (has state machine)
EventBuilder_1
I2c_master : DAQ_LINK_SI5342_I2C
I2c_master : I2C_reg_master_1
RCE_FELIX_SWITCH : RCE_PCS_1
RCE_FELIX_SWITCH : FELIX_PCS_1
DAQ_Link_EventBuilder : DAQ_Link_EventBuilders:1
DAQ_Link_EventBuilders:2
DAQ_Link_EventBuilders:3
DAQ_Link_EventBuilders:4
DQM : DQM_1
Data Quality Monitor stream
DQM_FIFO_1
DQM_FIFO : DQM_FIFO_1
DTS : DTS_1
DUNE Timing System
DTS_1
CDS_DATA_PLL : CDS_DATA_PLL_1
DTS_Convert_Generation : DTS_Convert_Generation_1
DTS_SI5344_ControL : DTS_SI5344_Control_1
DTS_tx : DTS_tx_1
I2c_reg_master : DTS_CDS_I2C
pdts_endpoint : pdts_endpoint_1
PDTS_PLL : PDTS_PLL_1
pass_std_logic_vector : pass_std_logic_vector_2
counter: \pdts_cmd_counts[15:0] : counter_1
pass_std_logic_vector: \pdts_cmd_counts[15:0] : pass_std_logic_vector_1
pass_std_logic_vector: \pdts_cmd_counts[15:0] : pass_reset
WIB_PWR_MON : WIB_POWER_MON_1
Monitors the voltage, temperature, and current of onboard regulators (i2c)
WIB_POWER_MON_1
I2c_master : I2c_master_S1_inst
I2c_master_S2_inst
I2c_master_S3_inst
I2c_master_S4_inst
KEY
BNL
BU
Bristol
Altera/Intel

DAQ_Link_EventBuilder



- CD_stream is of type CD_stream_array_t and has size
- (CDAS_PER_DAQ_LINK * LINKS_PER_CDA)
- array of types CD_Stream_t
- CDAS_PER_DAQ_LINK is set in WIB_Constants.vhd
  - is 2 for RCEs
  - is 4 for Felix
- LINKS_PER_CDA = 2

CD_Stream_t :
- valid
- capture_errors[7:0]
- CD_errors[15:0]
- CD_timestamp[15:0]
- data_out[31:0]

- control is of type **DAQ_Link_EB_Control_t :**
- enable
- COLDATA_en[4(8)-1:0] ([3:0] for RCE, [7:0] for Felix
- event_cout_reset
- spy_buffer_wait_for_trigger
- spy_buffer_start
- spy_buffer_read
- debug
- enable_bad_crc
- bad_crc_bits[15:0]
- gearbox, which is of type GB_Control_t

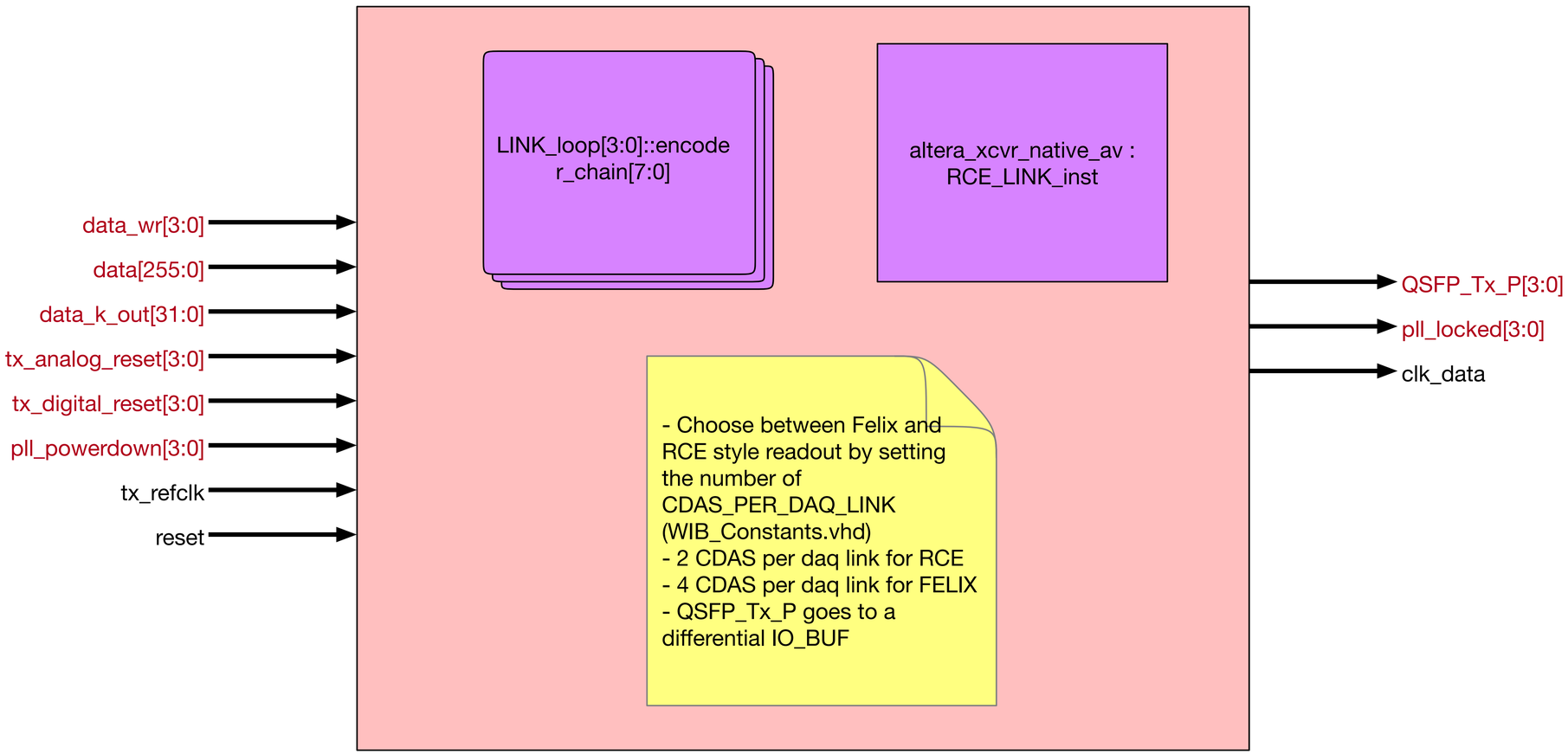
- monitor is of type **DAQ_Link_EB_Monitor_t :**
- enable
- COLDATA_en
- fiber_number
- FEMB_mask
- frate_id
- slot_id
- event_count
- spy_buffer_data
- spy_buffer_empty
- spy_buffer_running
- spy_buffer_wait_for_trigger
- debug
- enable_bad_crc
- bad_crc_bits
- gearbox

- convert is of type convert_t

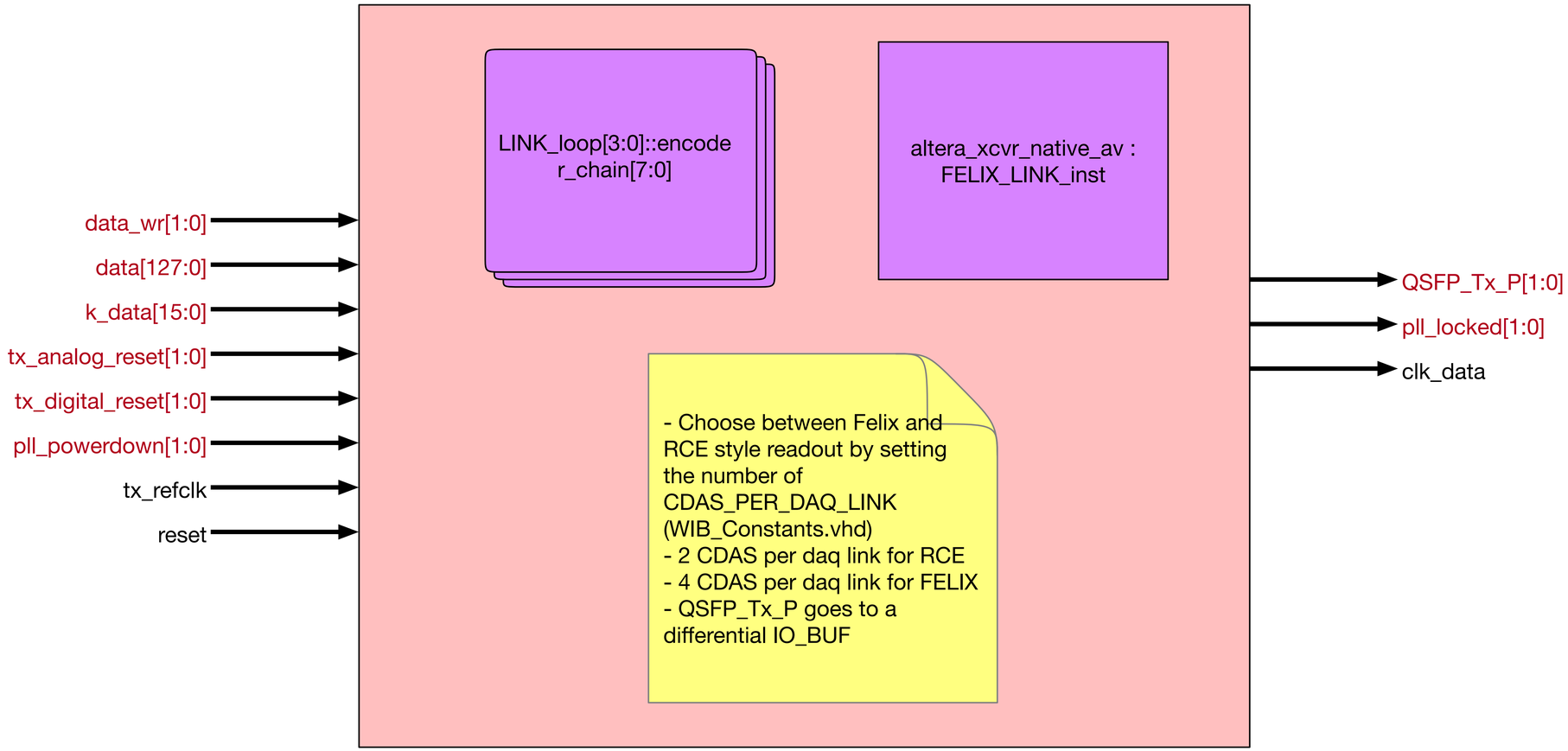
convert_t :
- trigger
- reset_count[23:0]
- convert_count[15:0]
- time_stamp[63:0]
- out_of_sync

- WIB_ID is of type WIB_ID_t
WIB_ID_t :
- slot[3:0]
- crate[3:0]

RCE_FELIX_SWITCH : RCE_PCS



RCE_FELIX_SWITCH : FELIX_PCS



COLDATA_Simulator

- generates fake data
- can inject errors
- one COLDATA_Simulator takes the place of one CDA
- each CDA has two links
- each data output stream simulates a single CDA link

clk
reset_sync
control
convert

monitor
data_out_stream1[8:0]
data_out_stream2[8:0]

- control is of type Fake_CD_Control_t
- one Fake_CD_Control_t per FEMB
- Fake_CD_Control_t is a record of analog and digital resets, one per FEMB link

- monitor is of type Fake_CD_Monitor_t
contain a record with logic vectors of size 4 (one per link per FEMB)

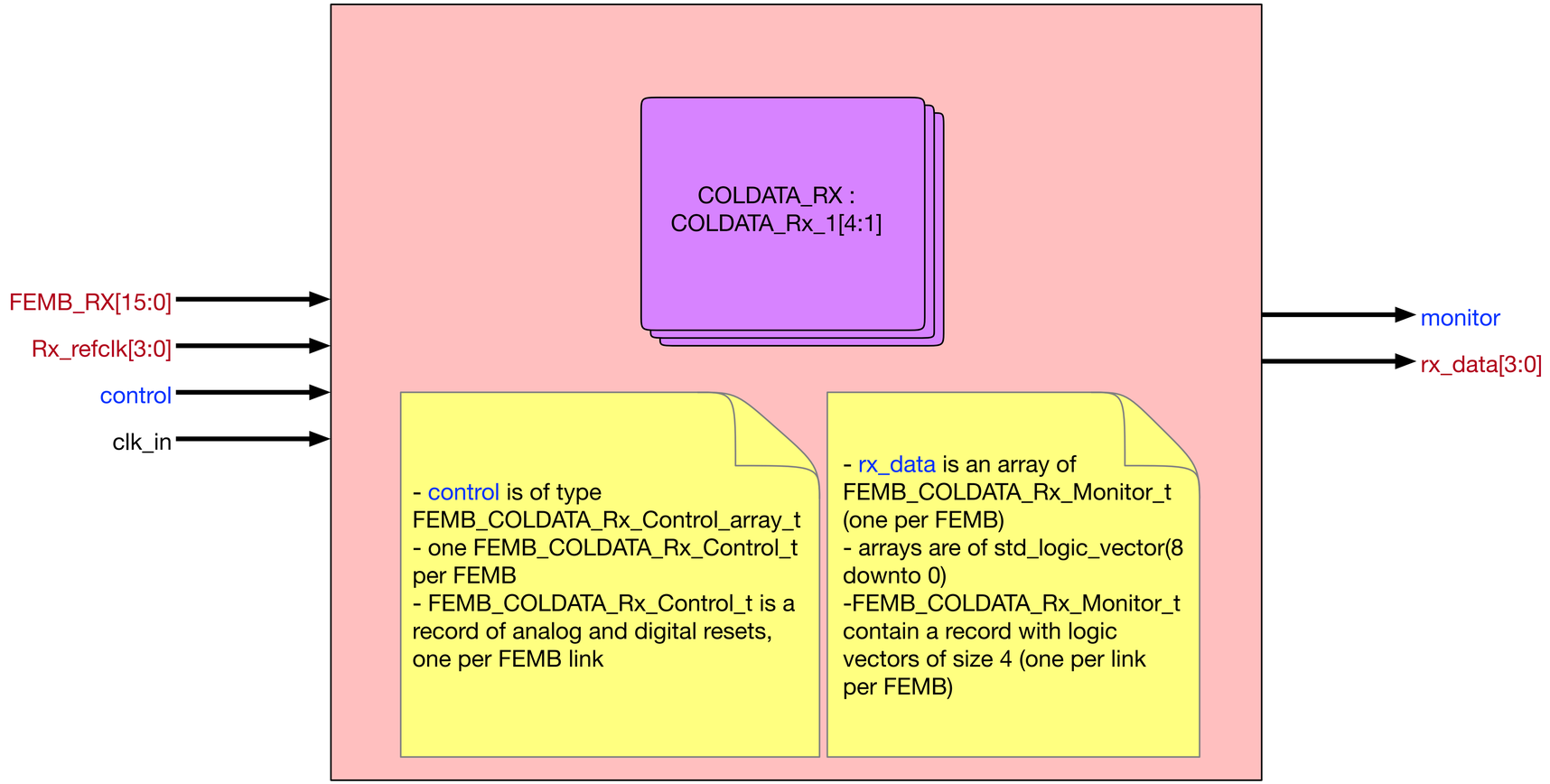
- convert is of type convert_t

convert_t :
- trigger
- reset_count[23:0]
- convert_count[15:0]
- time_stamp[63:0]
- out_of_sync

Fake_CD_Control_t :
-reset_counter_packets_1_A
-reset_counter_packets_1_B
-inject_errors
-inject_CD_errors[15:0]
-inject_BAD_checksum[1:0]
-inject_BAD_SOF[1:0]
-inject_LARGE_FRAME[1:0]
-inject_K_CHAR[1:0]
-inject_SHORT_FRAME[1:0]
-set_reserved[15:0]
-set_header[31:0]
-fake_stream_type[LINKS_PER_CDA:1]

Fake_CD_Monitor_t :
-counter_packets_A(B)
-counter_packets_B
-data_A[8:0]
-data_B[8:0]
-inject_CD_errors[15:0]
-inject_BAD_checksum[1:0]
-inject_BAD_SOF[1:0]
-inject_LARGE_FRAME[1:0]
-inject_K_CHAR[1:0]
-inject_SHORT_FRAME[1:0]
-set_reserved[15:0]
-set_header[31:0]
-fake_data_type[1:0]
-fake_stream_type[LINKS_PER_CDA:1]

FEMB_Rx

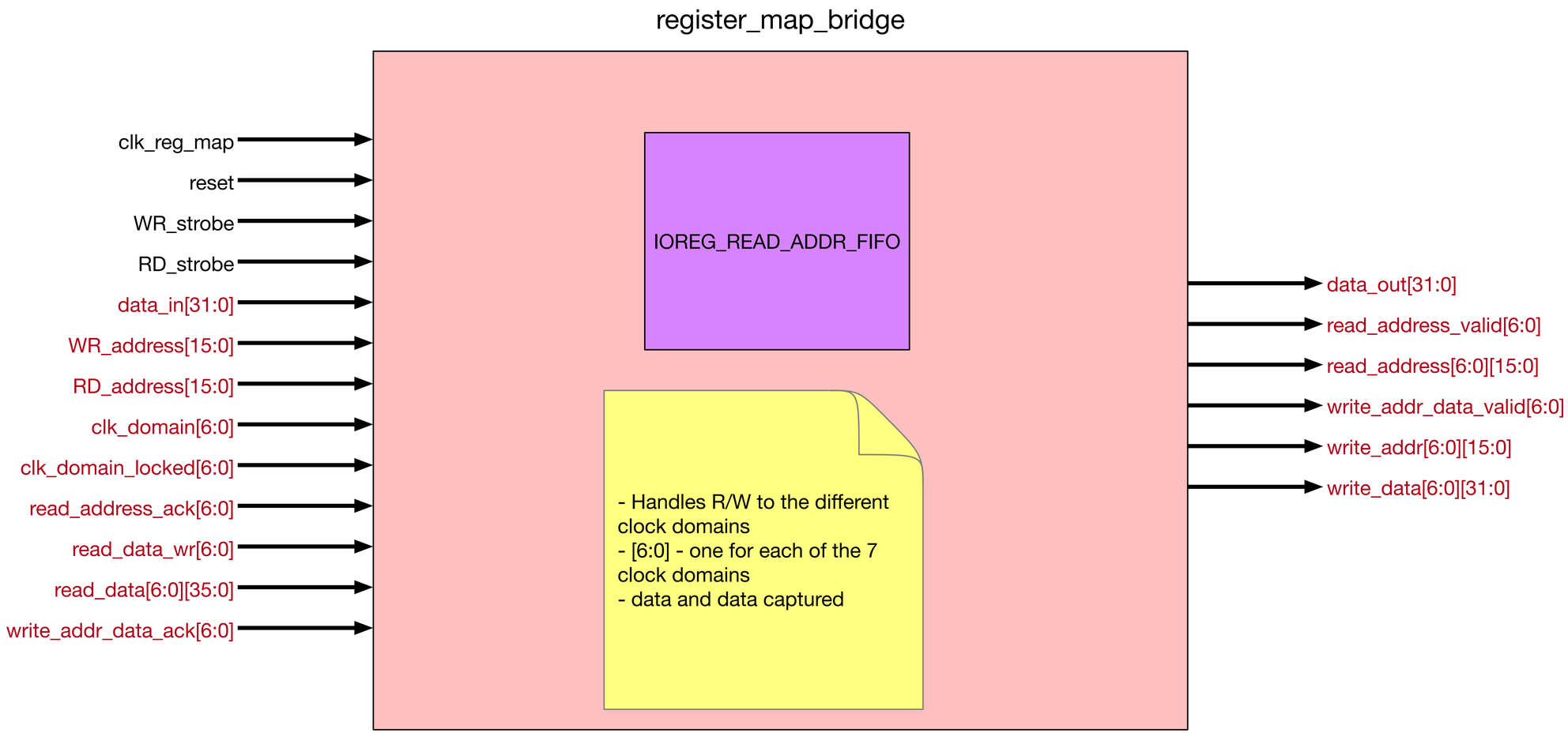


FEMB_COLDATA_Rx_Control_t :
- rx_analogreset
- rx_digitalreset

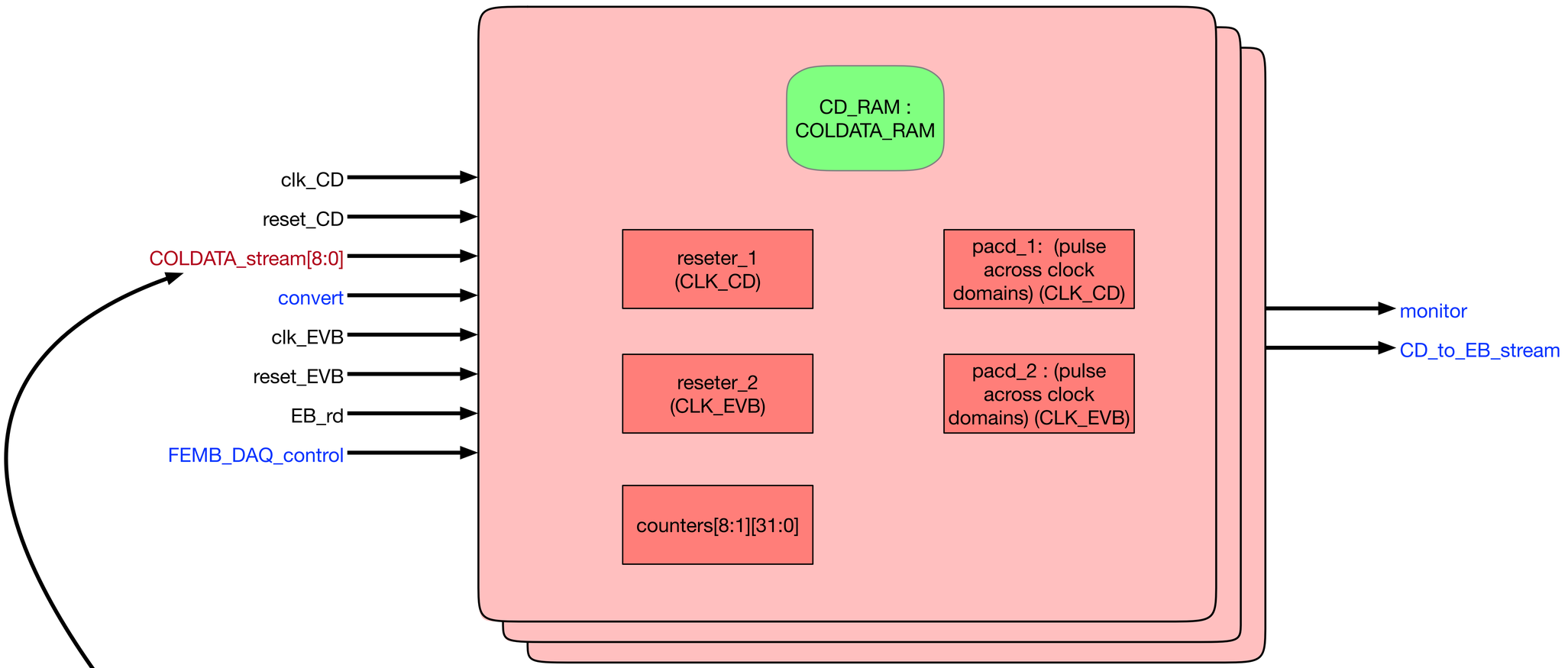
- FEMB_Rx has size LINK_COUNT, defined in WIB_Constants.vhd
- LINK_COUNT = FEMB_COUNT * LINKS_PER_FEMB
  - FEMB_COUNT = 4, per WIB
  - LINKS_PER_FEMB = CDAS_PER_FEMB * LINKS_PER_CDA
    - CDAS_PER_FEMB = 2
    - LINKS_PER_CDA = 2, the number of links per COLDATA ASIC

- Rx_refclk has size LINK_GROUPS, defined in WIB_Constants.vhd
- LINK_GROUPS = 4

FEMB_COLDATA_Rx_Monitor_t :
- rx_analogreset[4:1]
- rx_digitalreset[4:1]
- rx_cal_busy[4:1]
- rx_is_lockedtoref[4:1]
- rx_is_lockedtodata[4:1]
- rx_errdetect[4:1]
- rx_disperr[4:1]
- rx_runningdisp[4:1]
- rx_patterndetect[4:1]
- rx_syncstatus[4:1]


register_map_bridge
clk_reg_map
reset
WR_strobe
RD_strobe
data_in[31:0]
WR_address[15:0]
RD_address[15:0]
clk_domain[6:0]
clk_domain_locked[6:0]
read_address_ack[6:0]
read_data_wr[6:0]
read_data[6:0][35:0]
write_addr_data_ack[6:0]
IOREG_READ_ADDR_FIFO
- Handles R/W to the different clock domains
- [6:0] - one for each of the 7 clock domains
- data and data captured
data_out[31:0]
read_address_valid[6:0]
read_address[6:0][15:0]
write_addr_data_valid[6:0]
write_addr[6:0][15:0]
write_data[6:0][31:0]

CD_Stream_Processor



- 9th bit is used to indicate to the CD_Stream_Processor whether a word is a “command” or a “data” word
-If asserted it is not a data word

CD_RAM:
- 256B of RAM/processor
- R/W
- 8-bit input
- 32-bit output (q_b)

Relies on :
- FEMB_DAQ_package.vhd
- 4 links per FEMB
- 4 CD_Stream_processors, one for each link

Counters :
- BAD_CHSUM
- BAD_SOF
- BUFFER_FULL
- CONVERT_IN_WAIT_WINDOW
- KCHAR_IN_DATA
- MISSING_EOF
- UNEXPECTED_EOF
- packets

-monitor is of type CD_Stream_Monitor_t

CD_Stream_Monitor_t :
- convert_delay
- wait_window
- counter values from each of the counters listed (see Counters list)
- data[8:0]

-FEMB_DAQ_control is of type CD_Stream_Control_t

CD_Stream_Control_t :
- enable
- convert_delay
- reset inputs for each counter in the list of **Counters**

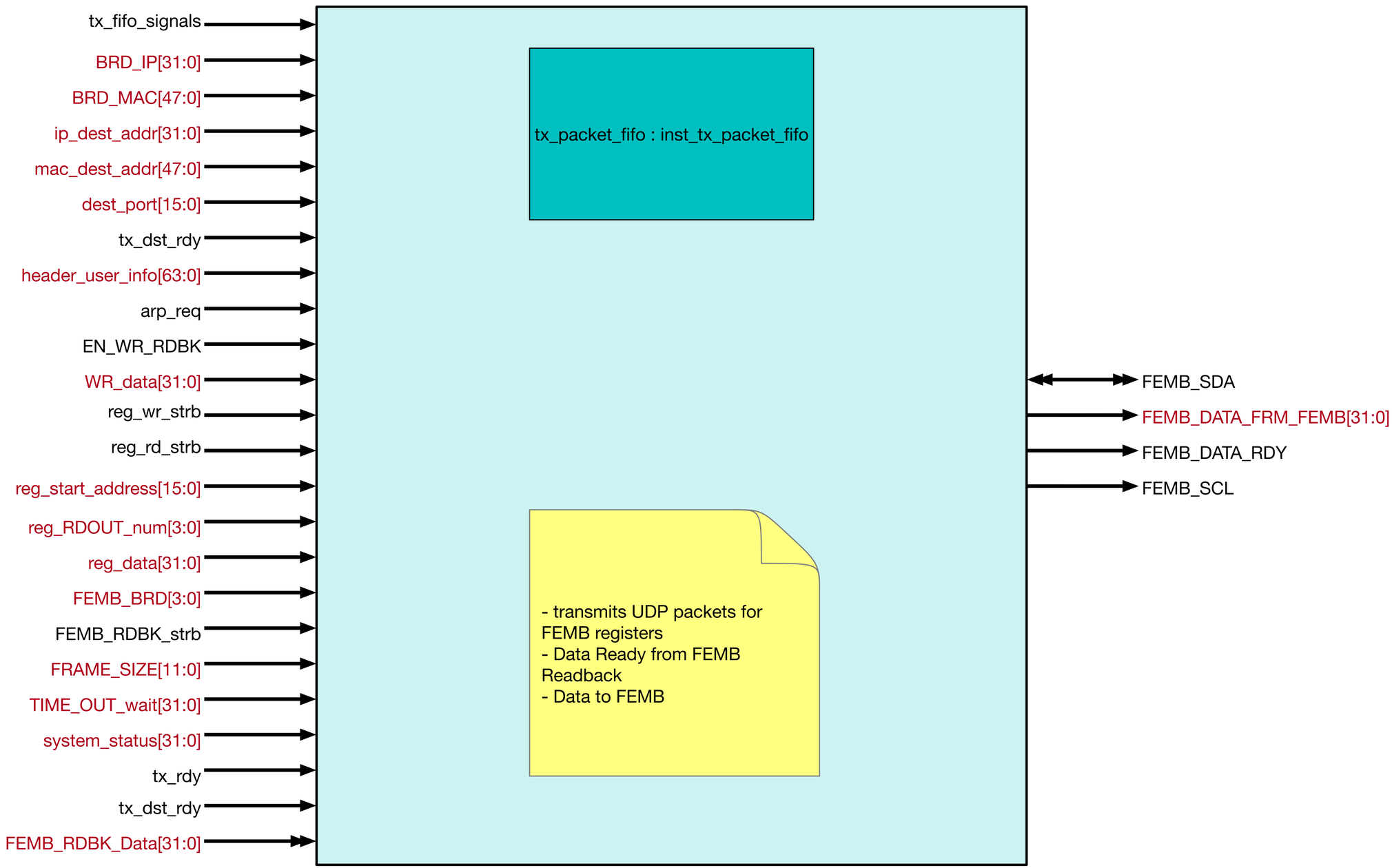
-CD_to_EB_stream is of type CD_stream_t

CD_Stream_t :
- valid
- capture_errors[7:0]
- CD_errors[15:0]
- CD_timestamp[15:0]
- data_out[31:0]

-convert is of type convert_t

convert_t :
- trigger
- reset_count[23:0]
- convert_count[15:0]
- time_stamp[63:0]
- out_of_sync

tx_frame

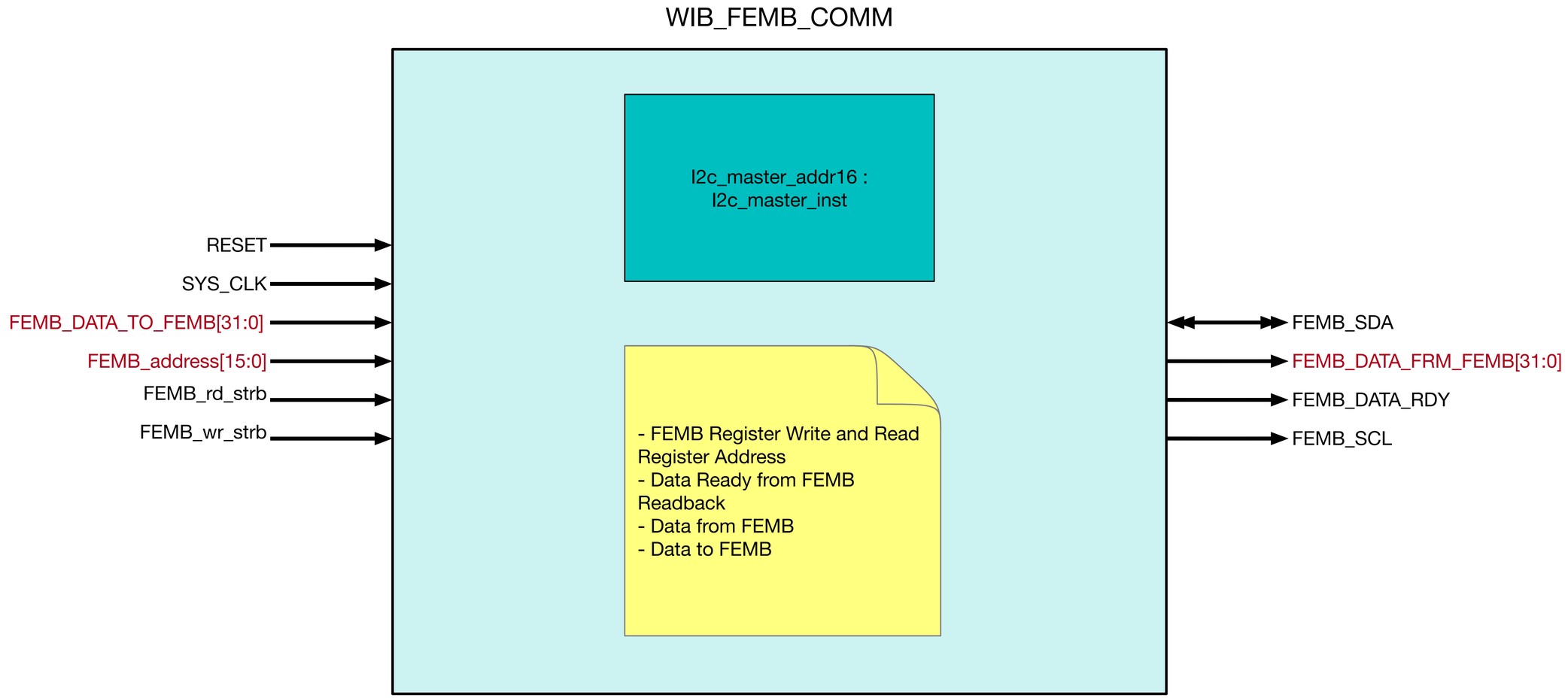

tx_fifo_signals
BRD_IP[31:0]
BRD_MAC[47:0]
ip_dest_addr[31:0]
mac_dest_addr[47:0]
dest_port[15:0]
tx_dst_rdy
header_user_info[63:0]
arp_req
EN_WR_RDBK
WR_data[31:0]
reg_wr_strb
reg_rd_strb
reg_start_address[15:0]
reg_RDOUT_num[3:0]
reg_data[31:0]
FEMB_BRD[3:0]
FEMB_RDBK_strb
FRAME_SIZE[11:0]
TIME_OUT_wait[31:0]
system_status[31:0]
tx_rdy
tx_dst_rdy
FEMB_RDBK_Data[31:0]
tx_packet_fifo : inst_tx_packet_fifo
- transmits UDP packets for FEMB registers
- Data Ready from FEMB Readback
- Data to FEMB
FEMB_SDA
FEMB_DATA_FRM_FEMB[31:0]
FEMB_DATA_RDY
FEMB_SCL

rx_frame

clk
reset
BRD_IP[31:0]
rx_data_in[7:0]
rx_dval
rx_eop
rx_sop

- FEMB frame receiver
- FEMB Register Read Register Address
- Data from FEMB

src_MAC[47:0]
src_IP[31:0]
src_port[15:0]
arp_req
ping_req
RD_WR_ADDR_SEL
IO_address[15:0]
IO_data[31:0]
WR_strb
RD_strb
WR_strb_RESP
FEMB_BRD[3:0]
FEMB_RD_strb
FEMB_WR_strb


WIB_FEMB_COMM
I2c_master_addr16 :
I2c_master_inst
RESET
SYS_CLK
FEMB_DATA_TO_FEMB[31:0]
FEMB_address[15:0]
FEMB_rd_strb
FEMB_wr_strb
- FEMB Register Write and Read Register Address
- Data Ready from FEMB Readback
- Data from FEMB
- Data to FEMB
FEMB_SDA
FEMB_DATA_FRM_FEMB[31:0]
FEMB_DATA_RDY
FEMB_SCL