DUNE FE ASIC Cold Studies: Ledge Threshold

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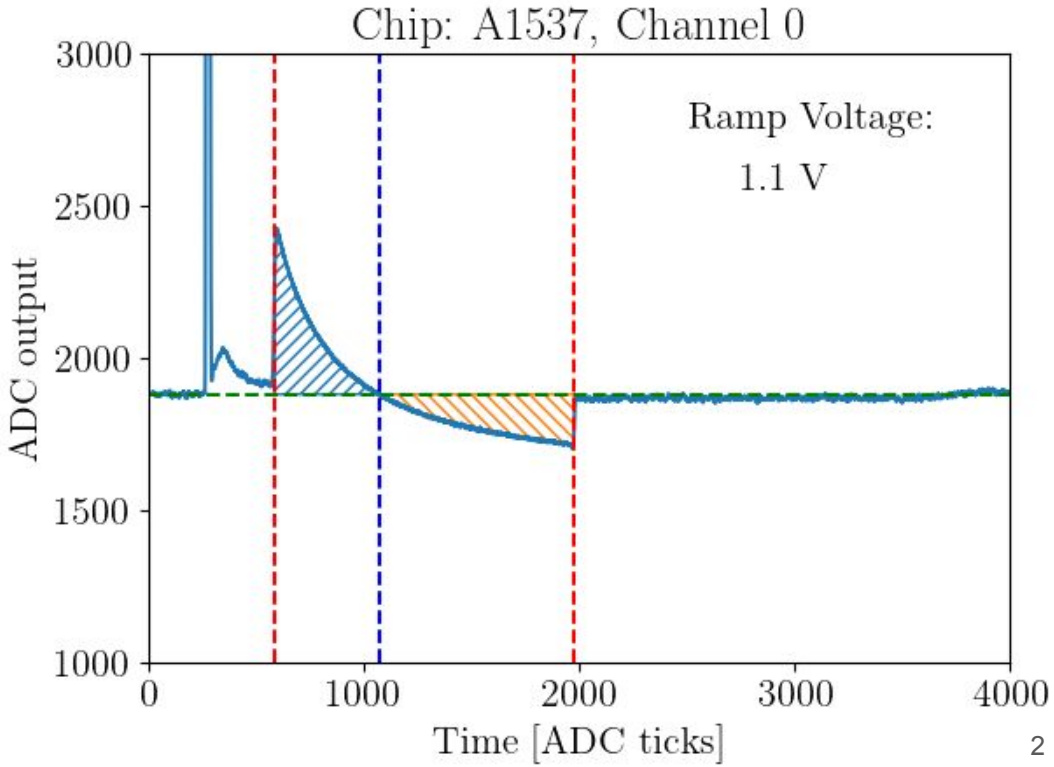
What is the ledge effect?

After receiving large pulses, the ASIC tends to “lock up”

Scales with input charge

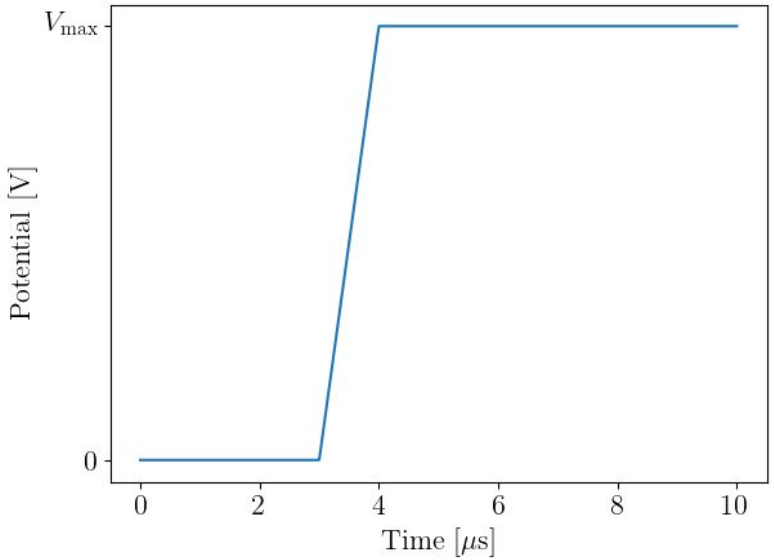
RMS noise decreases

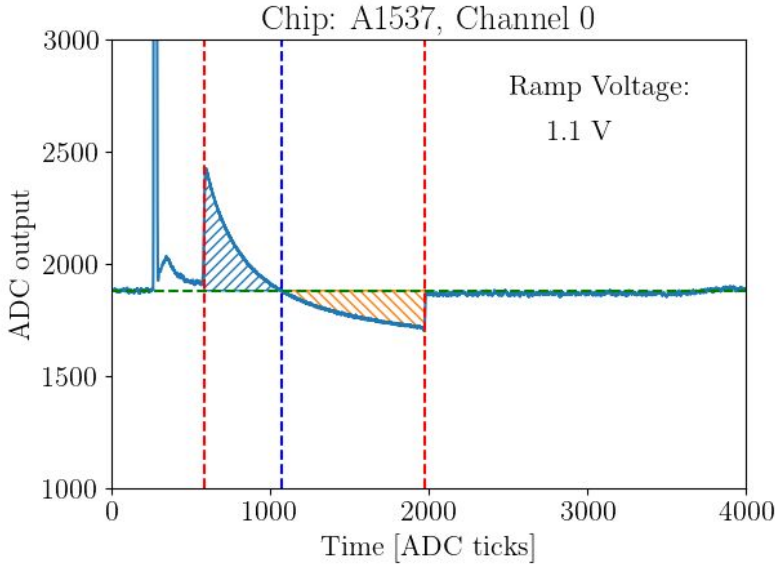


Instigating the Ledge

We use an arbitrary waveform generator to make a 1μs voltage ramp.

We scan through voltages (0.1V → 1.5V) and record the waveform.





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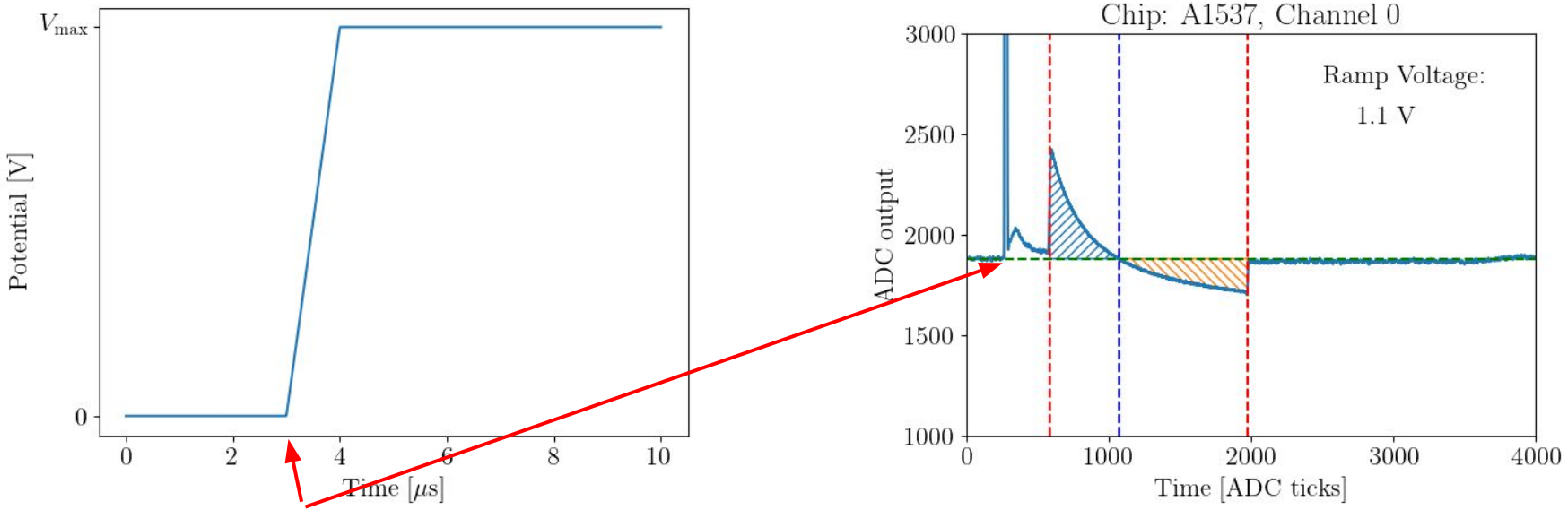
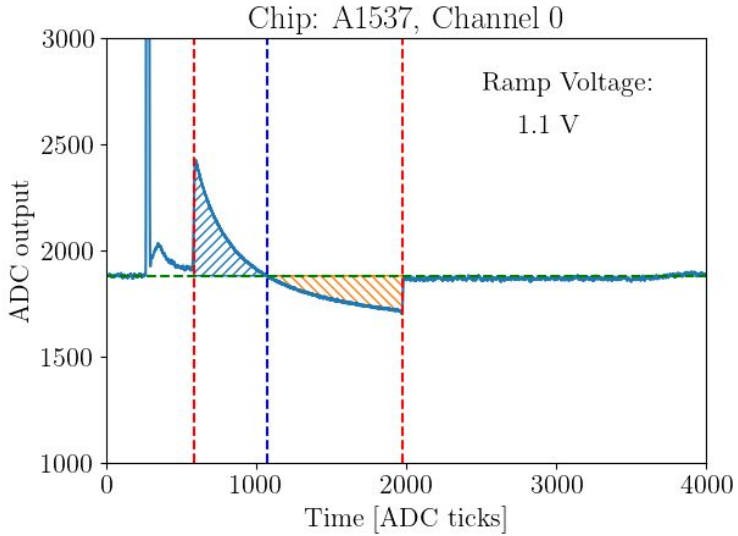
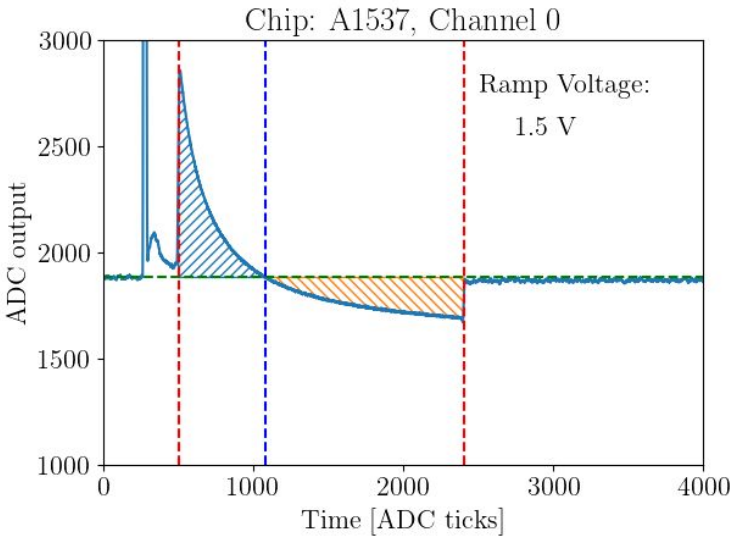


Waveform readout is synchronized with pulser.

Ledge Scaling

- Scaling in time (start, stop & duration)
- Scaling in magnitude
- Scaling in area

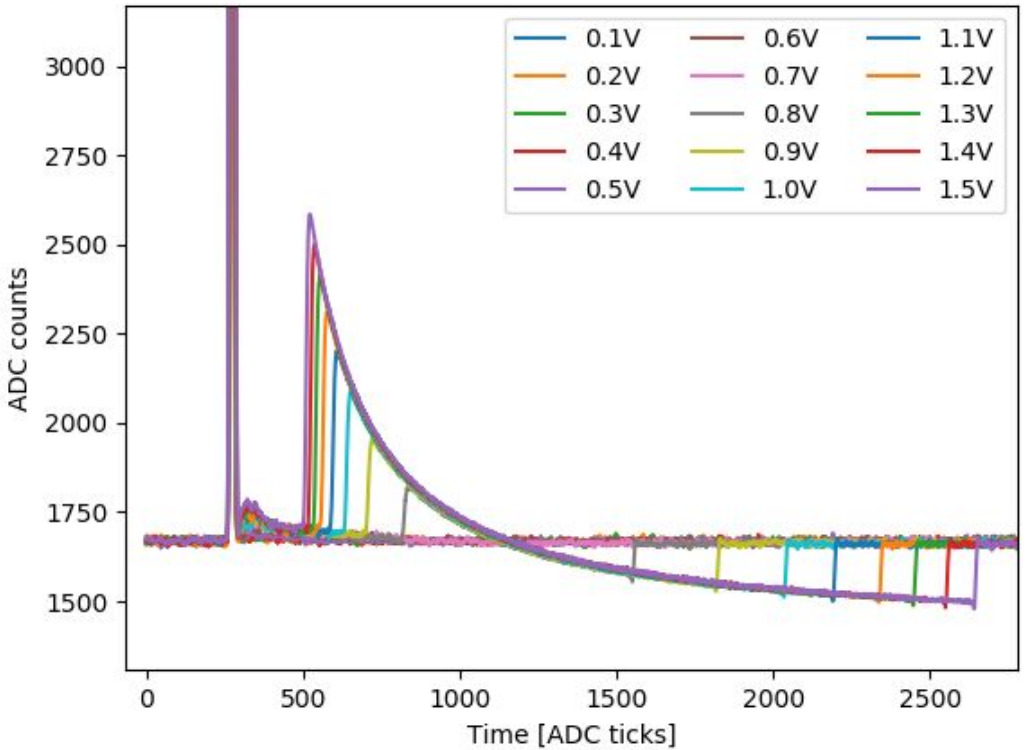




Ledge Scaling (Continued)

Ledges follow the same shape (exponential decay from peak?)

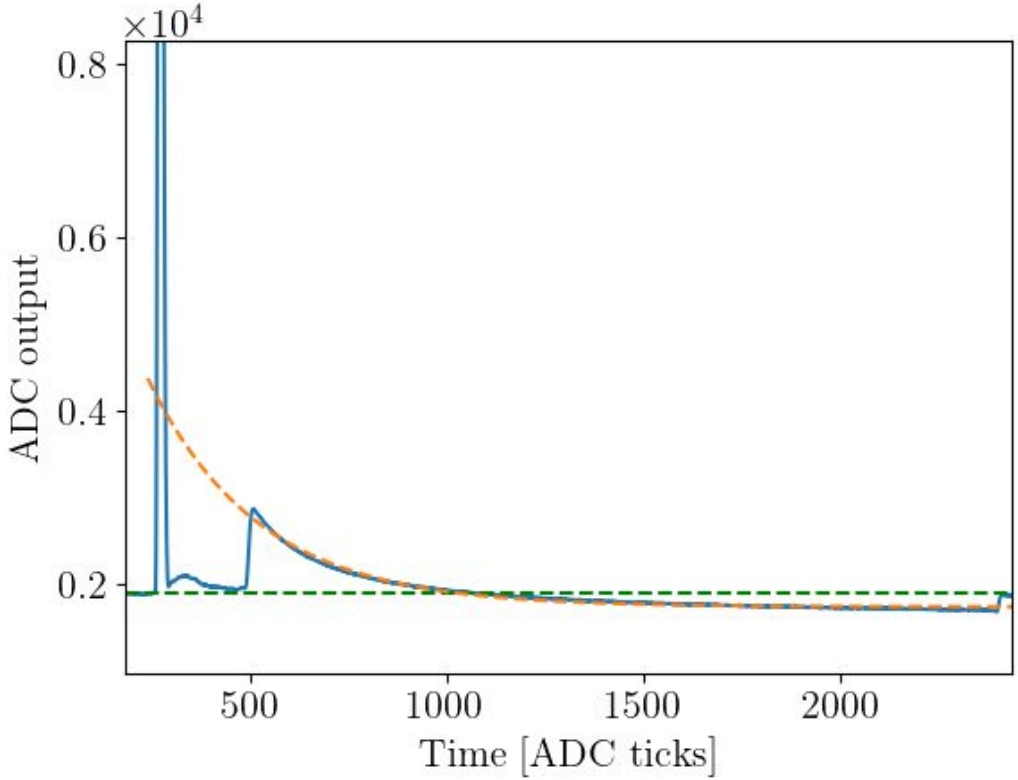
Only start/stop times change based on input charge.



Ledge Scaling (Continued)

Fitting an exponential yields a poor match.

Some other kind of decay from the peak?

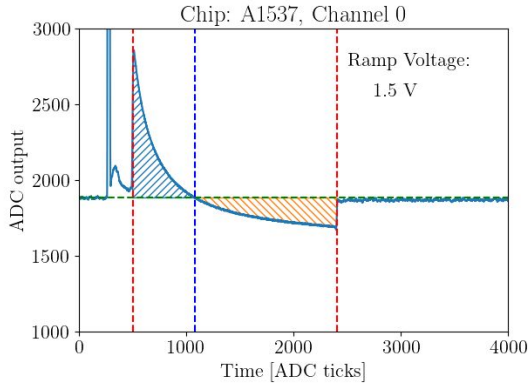


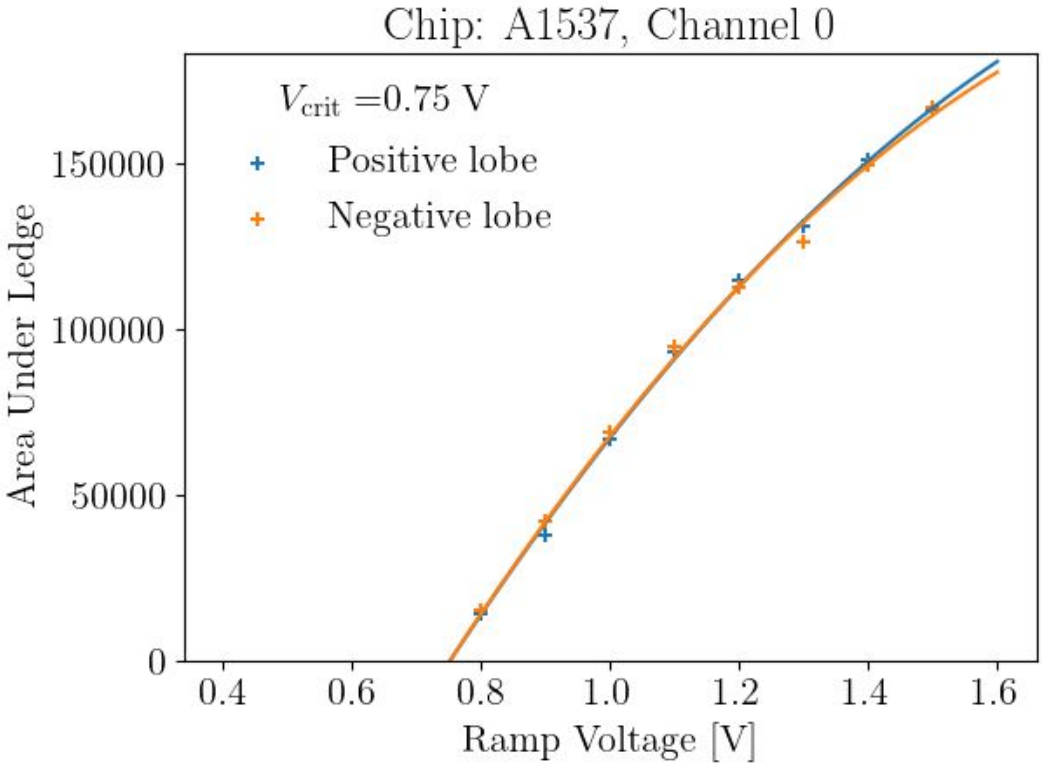
Finding V_{crit}

Find peaks and zero crossing

Calculate area (in ticks × counts)

Fit to quadratics (force them to have the same zero crossing)

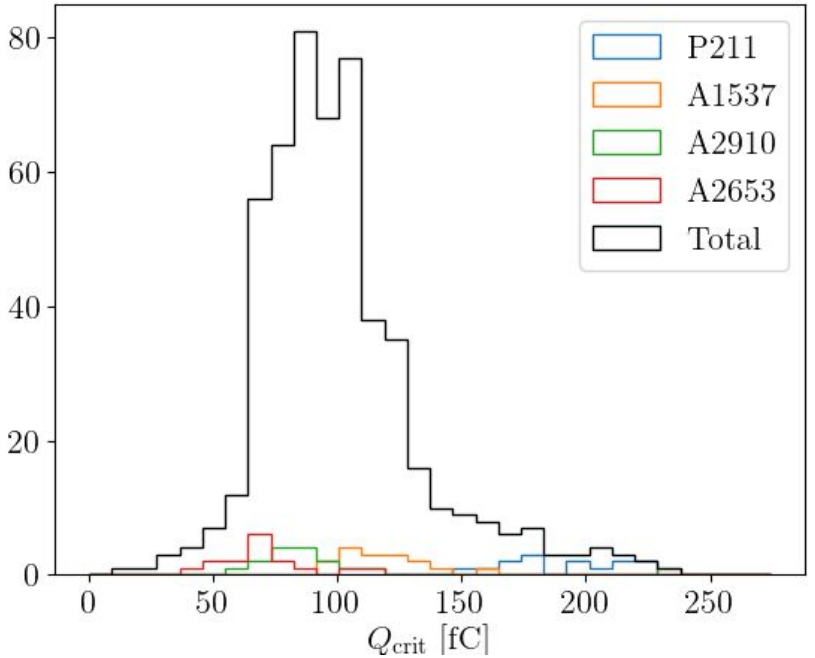




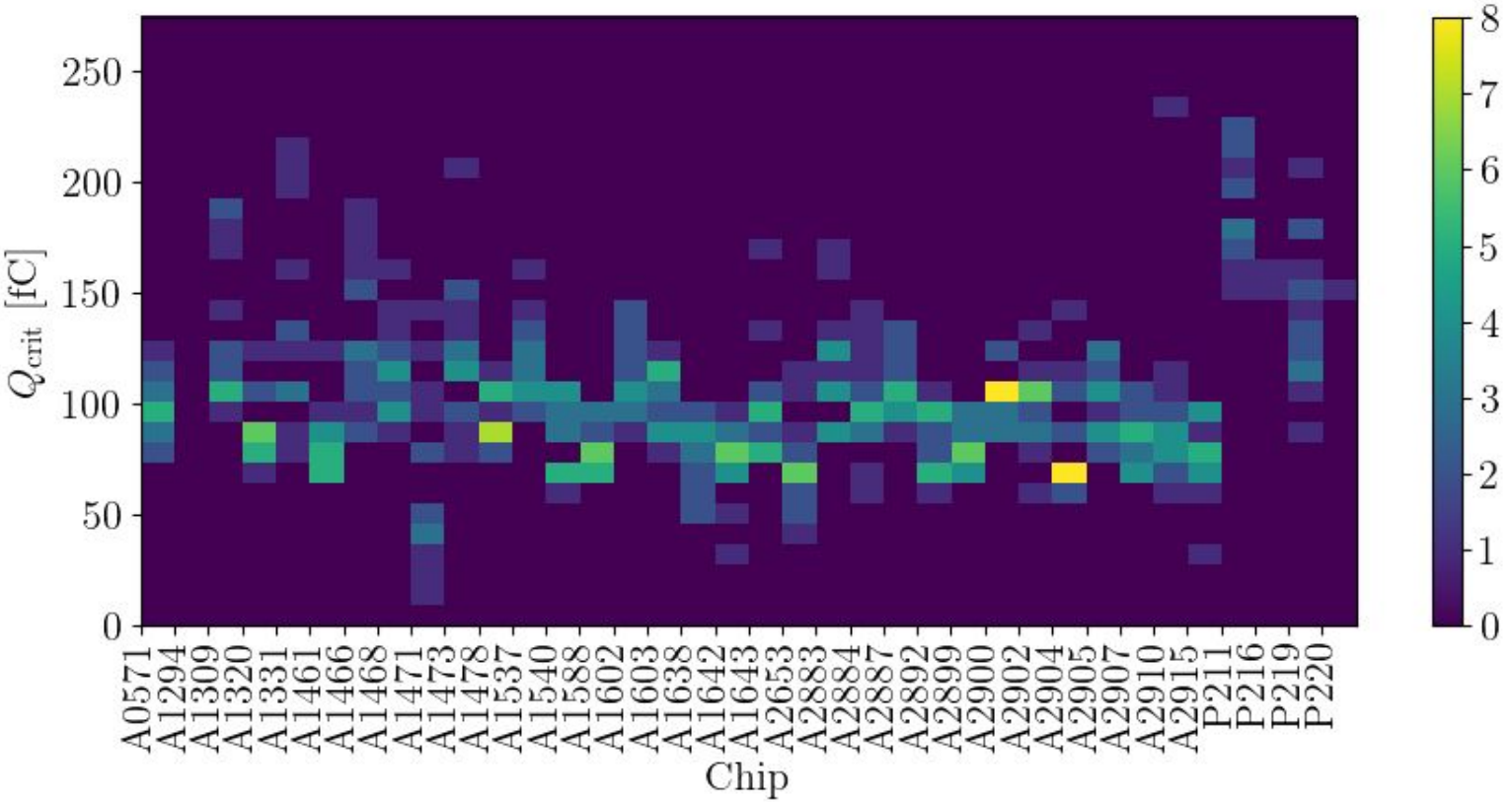
Finding V_{crit} (continued)

Critical voltage varies a lot from chip to chip and from channel to channel.

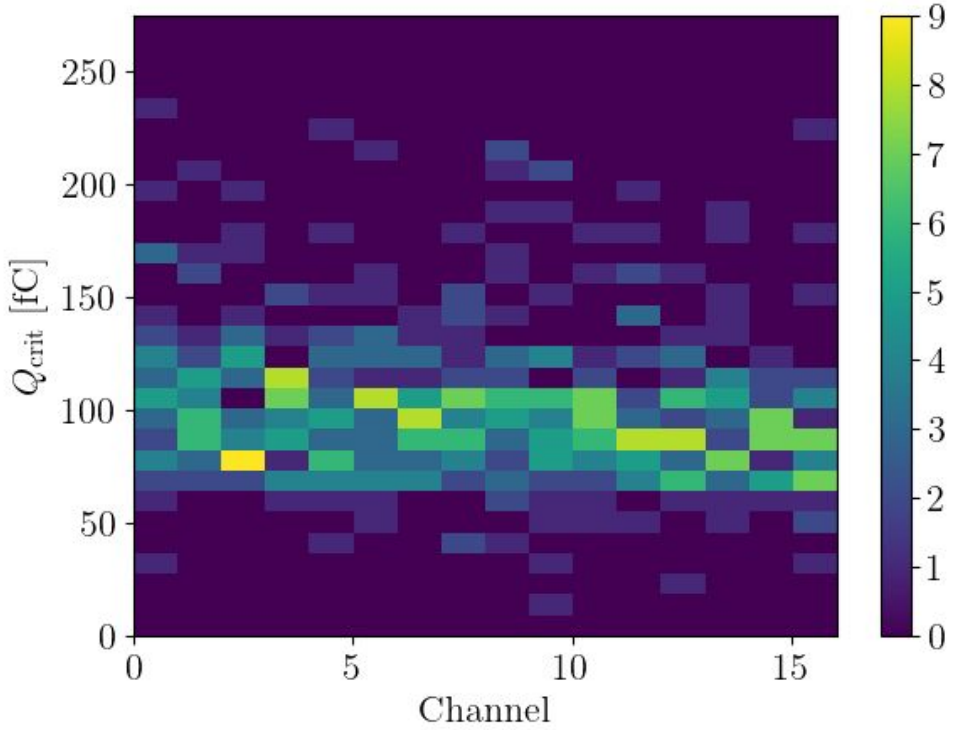
Some chips don't really show the ledge (A1294 is the only one we found with no ledge), and others barely show "non-ledge" behavior



Finding V_{crit} (continued)

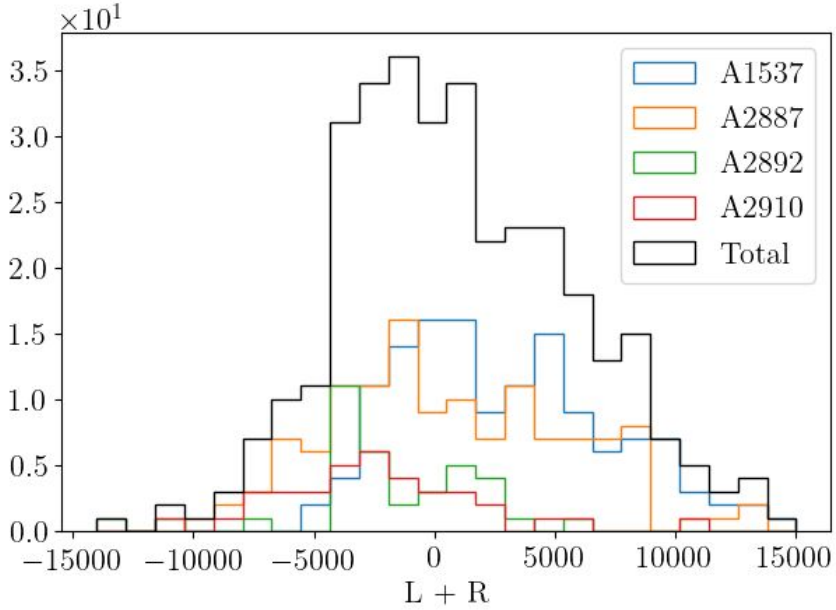


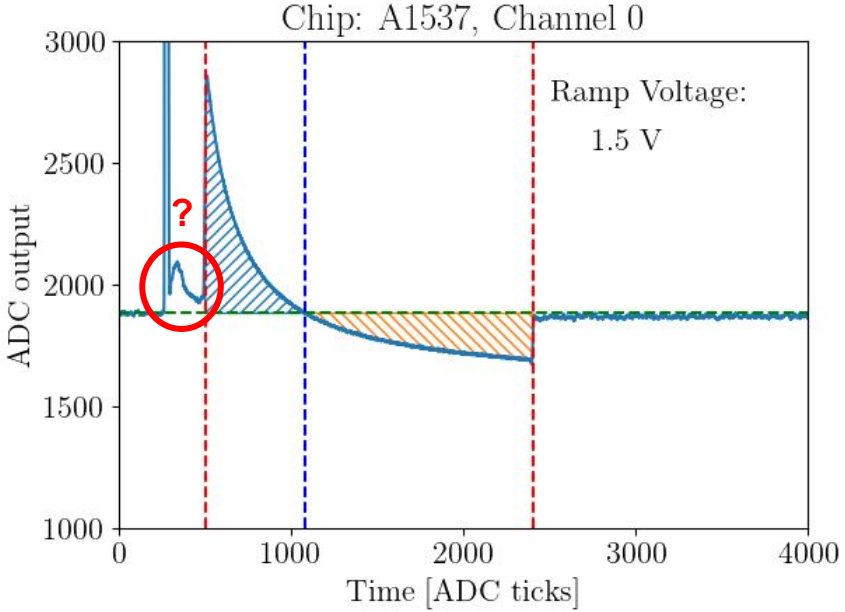
Finding V_{crit} (continued)



Lobe Evenness

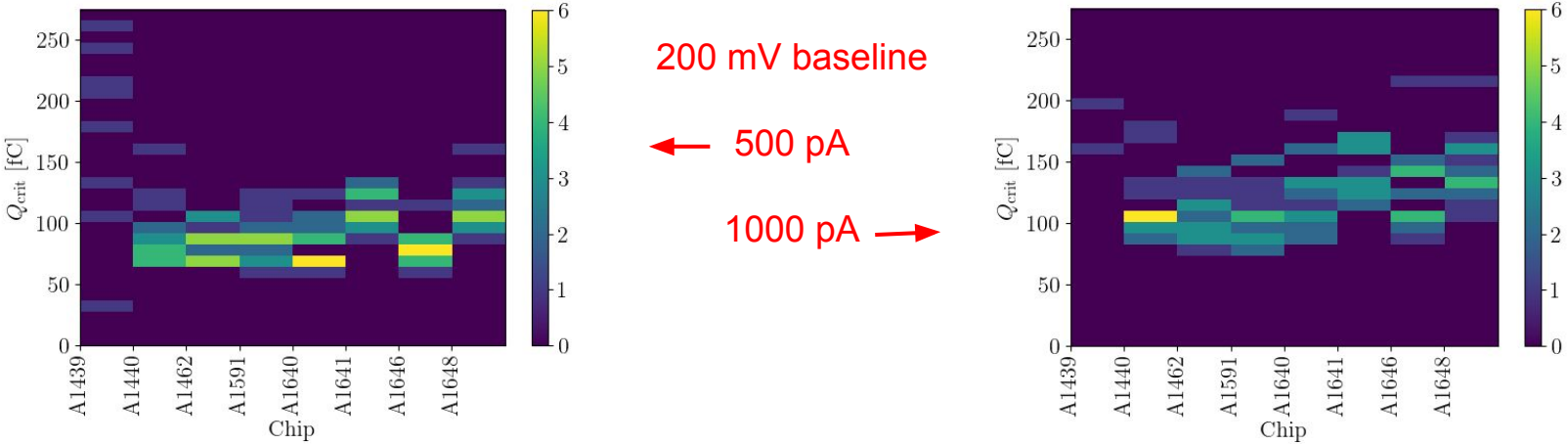
By eye, the two lobes look to have the same area, but the left lobe seems to have slightly more area, on average. Maybe to do with weirdness post-pulse?





Next Steps

Look into mitigation, e.g., which baseline/leakage settings yield the highest thresholds?

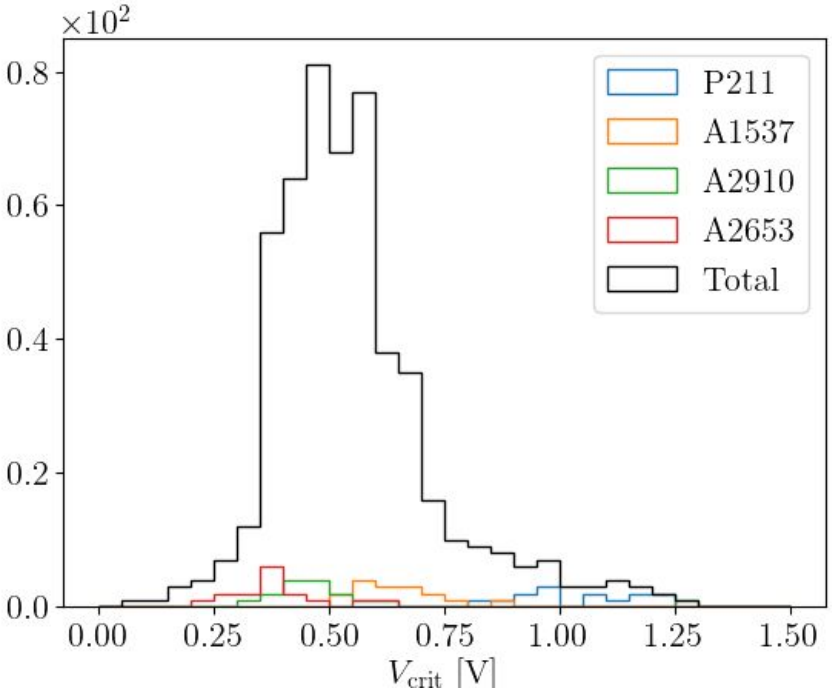


Still a WIP, different settings introduce baseline noise and jitter, so writing a generalized ledge-finding algorithm is difficult...

Thank For Listening!

BACKUP

Plots in Input Voltage



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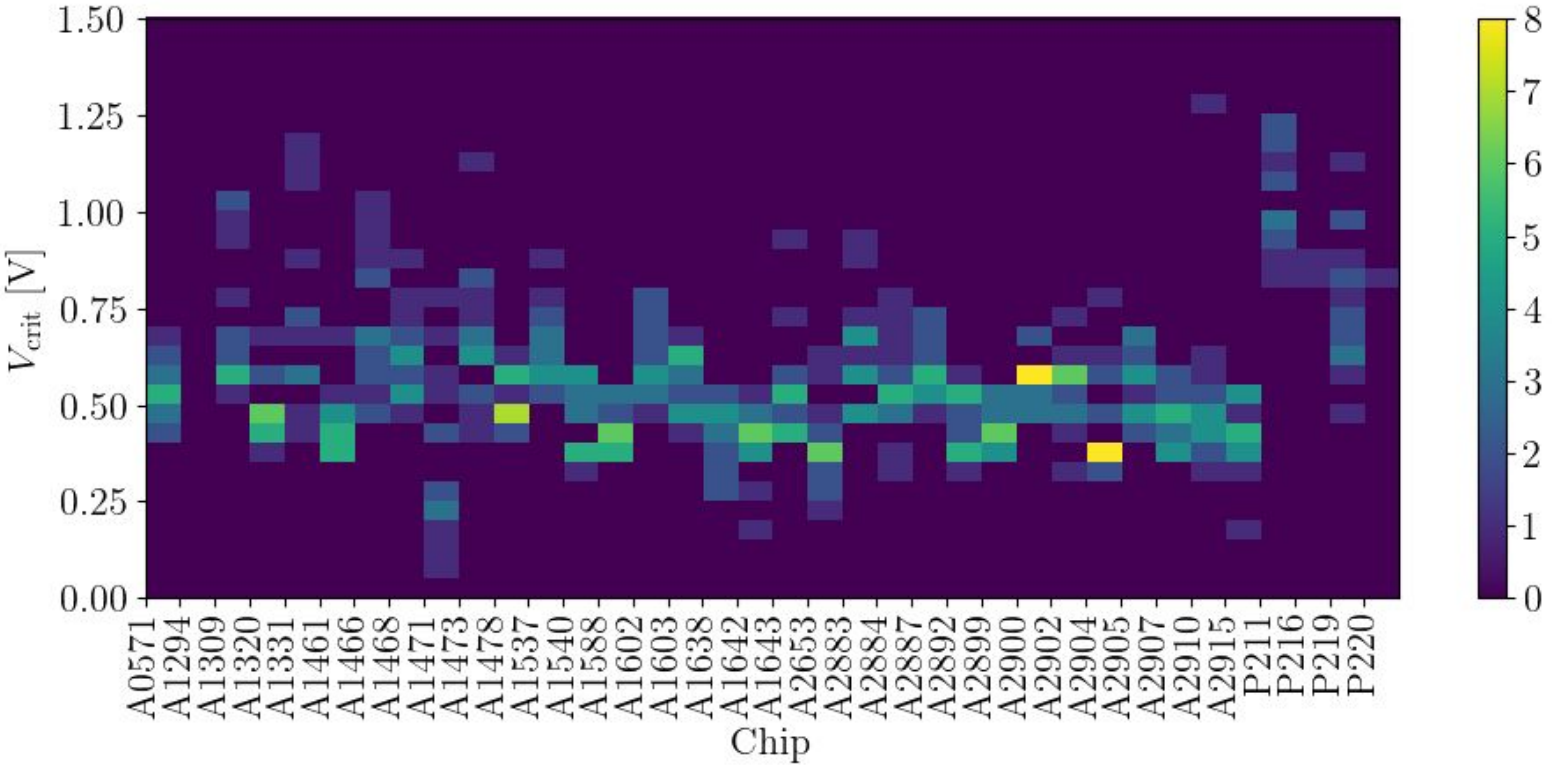

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