DIGITAL LOW LEVEL RF DEVELOPMENT AT DIAMOND LIGHT SOURCE

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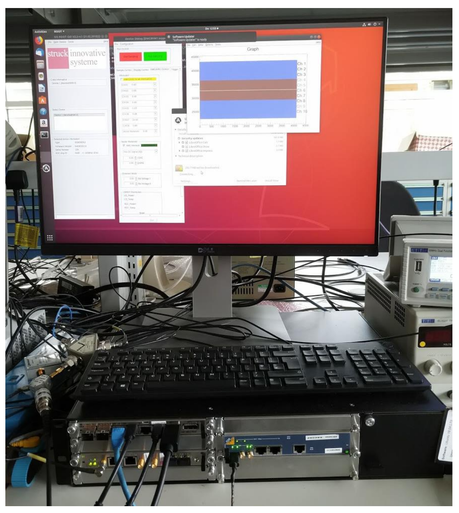
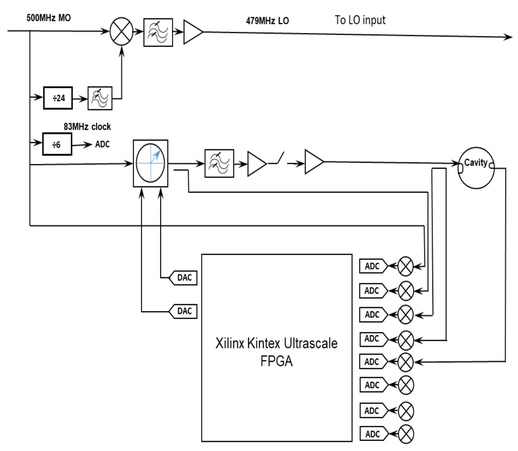
Introduction

DLLRF was successfully tested on the booster cavity of Diamond and is in routine operation with two normal conducting HOM-damped cavities in the Diamond stor-age ring. Six systems were built in total and three have been deployed. In the last few years, MTCA rear-transition-modules (RTM) with integrated RF front-ends working at 500 MHz and 3 GHz have become available. This offers more integrated solution for DLLRFs. The new SIS8300-KU with RTM was chosen for the next stage of the DLLRF development. Firmware, software and supporting hardware are being developed and tested. We are aiming to develop a common platform for the different RF systems in Diamond, including the storage ring, the booster and the linac.

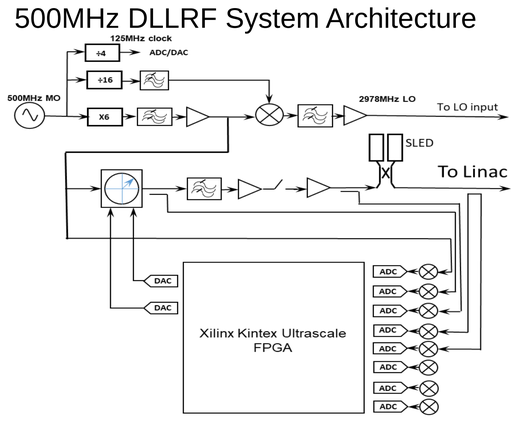
DLLRF Hardware

The DLLRF consists of a 2U MTCA.4 chassis, a MCH, an AMC computer board, a Struck SIS8300-KU card, a Struck DWC8VM1 RTM with supporting clock/local oscillator (LO)/reference generation RF circuits.





500MHz DLLRF System Architecture



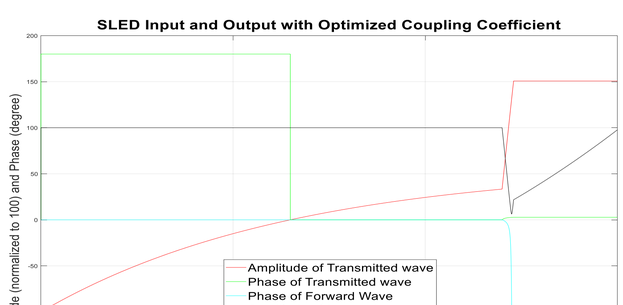
3GHz DLLRF System Architecture

SLED Operation Requirement

When operating in top-up mode for user beam the linac accelerates a single bunch of electrons, which is compatible with the generation of a peaked power pulse in the simplest mode of SLED operation. To fill the ring, from empty, however, the linac must accelerate a train of up to 120 bunches. A standard phase switch mode operation results in around 7% energy spread and so a flat-top pulse is required. I and Q components of SLED input pulse should follow the equations below.

$$F_x = \frac{R_x}{\alpha-1} + \alpha\left(1 - e^{-\frac{t1}{Tc}} - \frac{R_x}{\alpha-1}\right)e^{-\frac{(\alpha-1)(t-t1)}{Tc}} \quad 1)$$

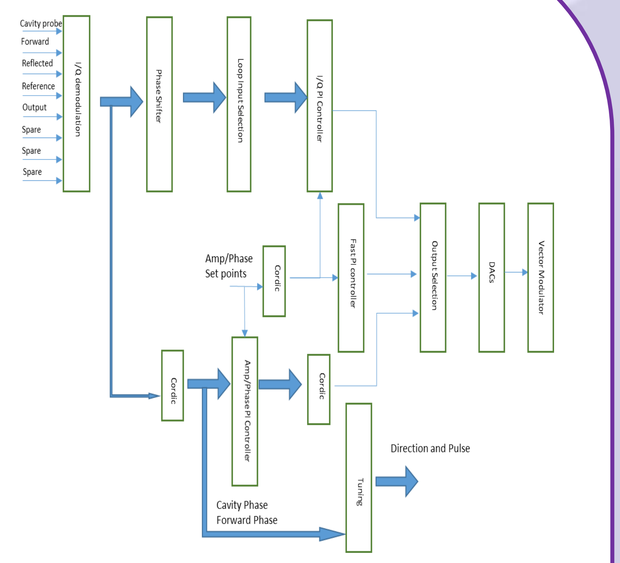
$$F_y = \frac{R_y}{\alpha-1} - \frac{\alpha R_y}{\alpha-1}e^{-\frac{(\alpha-1)(t-t1)}{Tc}} \quad 2)$$



DLLRF Firmware

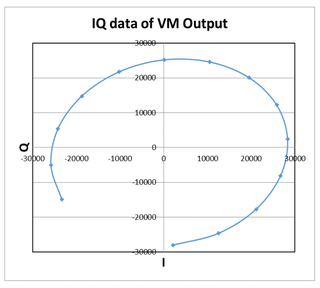
The 500MHz DLLRF and 3GHz DLLRF share many common modules, like IQ demodulation, Cordic, PI loop etc. . The 500MHz DLLRF can be configured to run 3 modes, namely the normal conducting booster cavity mode, superconducting storage ring cavity mode and normal conducting storage ring cavity mode.

3GHz DLLRF works in pulse mode. SLED operation requires the DLLRF to generate a pulse with phase and amplitude modulation. Phase and amplitude feedback will be needed to correct the pulse to pulse variation and long term drift. Phase and amplitude modulation is required in the final 1μs. A simulation in Xilinx Vivado is shown in Figure on the right. A simple phase switch with feedback control is implemented. This can be easily extended to full phase and amplitude modulation pulse.



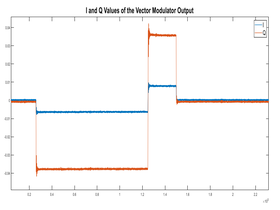
NEW DLLRF TESTS

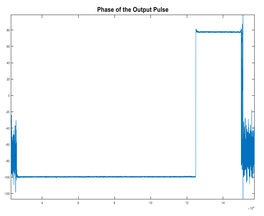
The test of vector modulator output is shown in figure 6. IQ imbalance and offset can clearly be seen. This is not a problem for the storage ring as the feedback loops will correct the output. The 3GHz DLLRF for the Linac may need calibration to compensate these errors.



Vector Modulator Test

The first results of the 3GHz DLLRF are shown in Figure on the right. The top plot shows the IQ data, while the bottom plot shows the phase during the pulse. A phase switch of 180º during the final 1μs can be seen clearly. This IQ profile is sufficient to accomplish pulse compression for single bunch linac operation. This can be easily extended to a phase and amplitude modulation pulse.





3GHz DLLRF Test

References

[1] Pengda Gu, C. Christou et al., “Digital Low Level RF Systems for Diamond Light Source”, in Proc. 8th Int. Particle Accelerator Conf. (IPAC ’17), Copenhagen, Denmark, May 2017, pp. 4089-4091.
[2] Benjamin Woolley, Igor Syratchev et al, “Control and performance improvements of a pulse compressor in use for testing accelerating structures at high power”, in PHYSICAL RE-VIEW ACCELERATORS AND BEAMS 20, 101001 (2017).

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