Characterization of the MicroTCA.4-based 8 Channel, Direct Sampling, Single Channel Up-Converter Board.

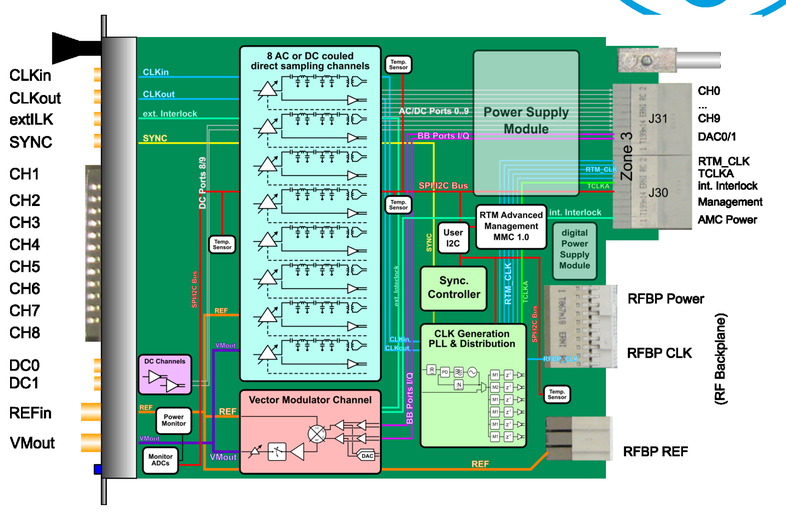
F. Abdi, L. Butkowski, Ç. Gümüş, M. Hoffmann*, F. Ludwig, U. Mavrič, H. Schlarb, DESY

Abstract

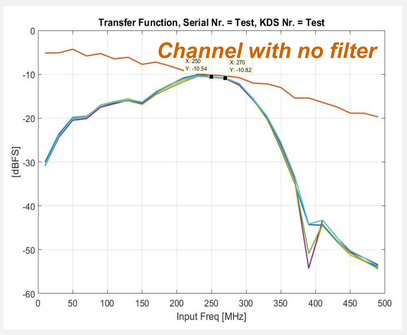
In preparation for the next revision we have performed extensive and systematic measurements of the DRTM-DS8VM1. The reconfigurability of the board requires testing various usage scenarios. In the poster we present a list of tested functionalities and parameters. There has been several lessons we learned during the process and we present some of the most representative. Finally, we briefly go through the improvements for the next board revision.

Investigated points

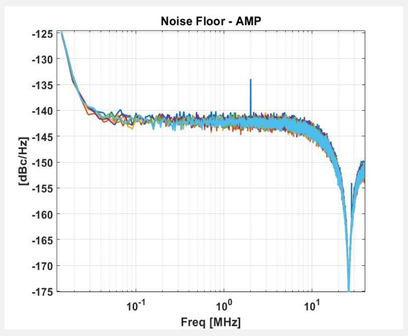
- Receiver characterization (AC and DC)
- Vector modulator characterization
- CLK section characterization



AC coupled channels

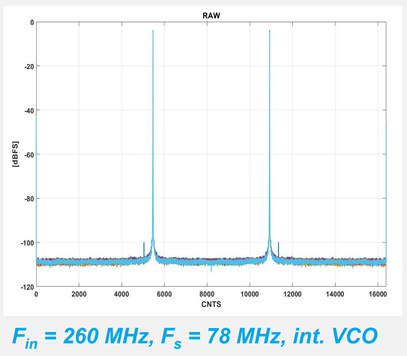


Transfer function, 260 MHz BP

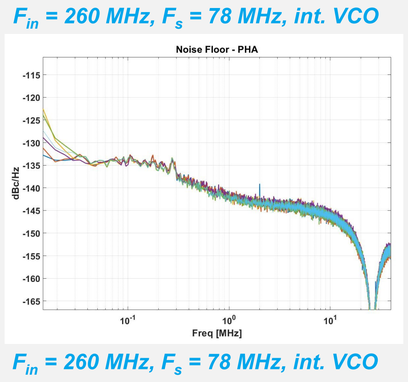


F_{in} = 260 MHz, F_s = 78 MHz, int. VCO

S_{11} for 260 MHz optimized module



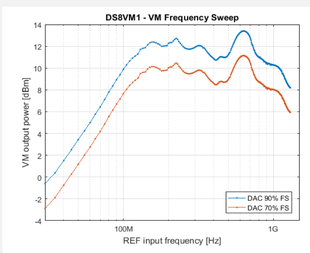
F_{in} = 260 MHz, F_s = 78 MHz, int. VCO



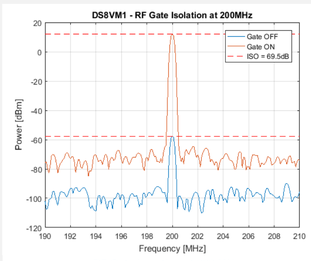
F_{in} = 260 MHz, F_s = 78 MHz, int. VCO

AC RECEIVERS		Values	Units
Clipping Input Power	Ch 1-6	+18	dBm
	Ch 7	+19.5	dBm
	Ch 8	+19.5	dBm
Short-term RMS amp. stability	BW = Fs/2, -3dBFS	0.25	%
Short-term RMS phase stability	BW = Fs/2, -3dBFS	0.026	deg
AN Noise Floor	at 5 MHz offset	-132	dBc/Hz
PN Noise Floor	at 5 MHz offset	-145	dBc/Hz
Non-harmonics SFDR	In Fs/2 bandwidth	< -105	dBFS
	No Input SFDR (except cross-talk) at -3dBFS	-120	dBFS
Harmonic SFDR	In FS/2 bandwidth at -3dBFS	-66	dBFS
PIP3	At 260 MHz	+46	dBm
$P_{0.05dB}$	At 260 MHz	+15.7	dBm
Cross-Talk	At 260 MHz	-70	dBc
Matching (S_{11})	Ch1-6	<-20	dB
	Ch7 (FBM in) – Standard input	<-20	dB
	Ch8 (FBM in) – Standard input	<-20	dB

Vector Modulator

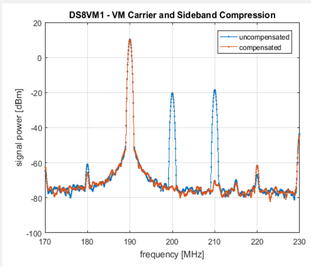


VM output power vs REF input frequency, f_{mod} = 0 Hz

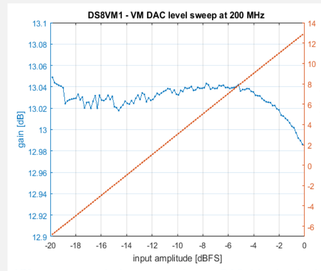


RF Gate Isolation at 200 MHz

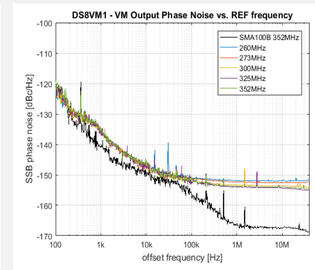
Parameter	Conditions and Comments	Result			Unit
		Min	Typ.	Max	
VECTOR MODULATOR					
VM RF frequency range	3 dB band width	110		960	MHz
	9 dB	50			
VM modulation bandwidth				50	MHz
VM output power level	110…960 MHz, at 90% (-1 dBFS) of DAC full scale	10.4	12.0	13.4	dBm
	at 50 MHz		4.2		dBm
VM attenuator range	f_c = 200 MHz	0		15.75	dB
RF gate isolation	f_c = 200 MHz	69.5			dB
Short-term RMS amplitude stability		0.0032	0.0035	0.0054	%
[10 Hz…1 MHz]					
Short-term RMS phase stability	at 108 MHz		70		fs
[100 Hz...1 MHz]	at 352 MHz		12		fs
	at 650 MHz		7.5		fs
AM noise floor		-157.6	-154.7	-146	dBc/Hz
at 10 MHz offset					
PM noise floor	at 108 MHz		-146.8		dBc/Hz
at 10 MHz offset	at 352 MHz		-154.1		dBc/Hz
	at 650 MHz		-156.0		dBc/Hz
Long-term stability	(amplitude/phase drifts)				
Sideband and carrier suppression	compensated		80.3	84.6	dBc
f_c = 200 MHz , f_{mod} = 10 MHz	uncompensated		28.8	32.5	dBc
Nonlinearity/compression error	at 90% (-1 dBFS) DAC full scale		-0.04		dB
f_c = 200 MHz	at 70% (-3 dBFS) DAC full scale		-0.014		dB
Non harmonic spurious			78		dBc
REF input return loss	REFin SMA connector				dB
VM output return loss	VMout SMA connector				dB



Carrier and sideband suppression in compensated and uncompensated state at fc = 200 MHz and fmod = 10 MHz with DAC signal level at -3 dBFS;

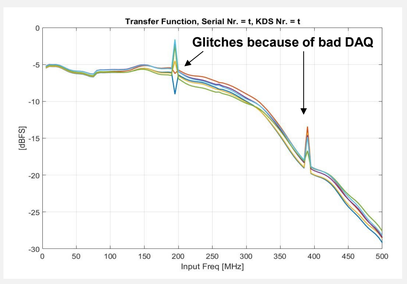


VM output power/gain compression vs. DAC drive level, with f_{mod} = 0 Hz;

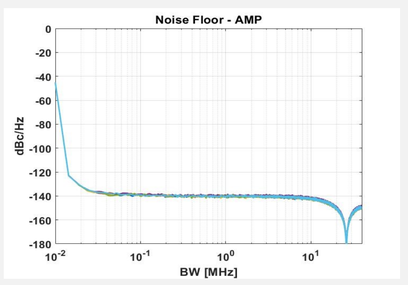


VM output phase noise at different carrier frequencies; DAC signal level at -3 dBFS with f_{mod} = 0 Hz;

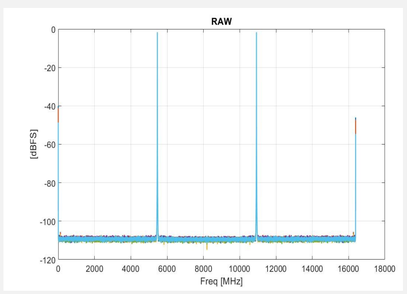
DC coupled channels



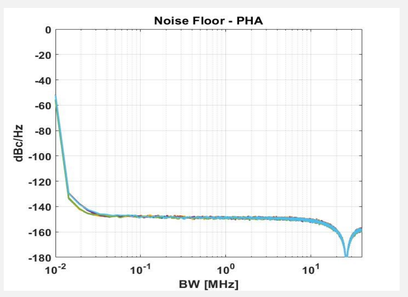
Transfer function, DC Input



F_{in} = 26 MHz, F_s = 78 MHz, int. VCO

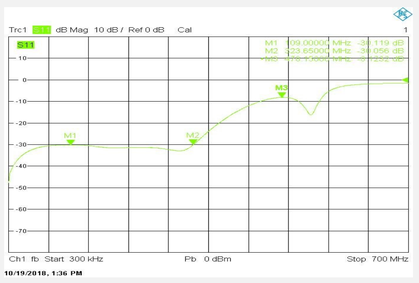


F_{in} = 26 MHz, F_s = 78 MHz, int. VCO



F_{in} = 26 MHz, F_s = 78 MHz, int. VCO

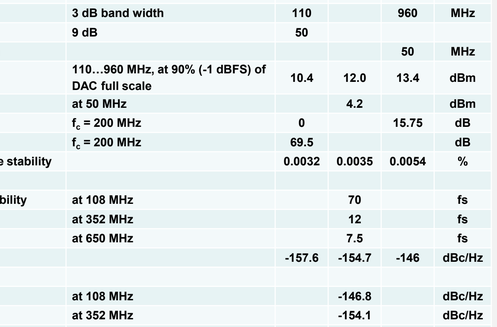
RECEIVER			
Channel Bandwidth	-3dB	250	MHz
Clipping Input Power	26 MHz	+12	dBm
Short-term RMS amp. stability	BW = Fs/2, -3dBFS		
	Frf = 26 MHz	0.021	%
	Frf = 260 MHz	0.062	%
Short-term RMS phase stability	BW = Fs/2, -3dBFS		
	Frf = 26 MHz	0.012	deg
	Frf = 260 MHz	0.050	deg
AN Noise Floor	at 5 MHz offset, -3dBFS		
	Frf = 26 MHz	-135	dBc/Hz
	Frf = 260 MHz	-124	dBc/Hz
PN Noise Floor	at 5 MHz offset, -3dBFS		
	Frf = 26 MHz	-149	dBc/Hz
	Frf = 260 MHz	-137	dBc/Hz
Cumm. Ampl. Uncertainty	[4.8kHz – Fs/2]		
	Frf = 26 MHz	0.020	%
	Frf = 260 MHz	0.061	%
Cumm. Jitter	[4.8kHz – Fs/2]		
	Frf = 26 MHz	1280	fs
	Frf = 260 MHz	534	fs
Non-harmonics SFDR	In Fs/2 bandwidth		
	Frf = 26 MHz	<-105	dBFS
	Frf = 260 MHz	-85	dBFS
Harmonic SFDR	In FS/2 bandwidth at -3dBFS		
	Frf = 23 MHz	-55	dBFS
	Frf = 257 MHz	-35	dBFS
Compression			
	P_{1dB} ,257 MHz	+7	dBm
	P_{3dB} ,257 MHz	+11	dBm
Cross-Talk			
	At 26 MHz	-85	dBc
	At 260 MHz	-70	dBc
Matching (S_{11})	Ch1-8 , < 300 MHz	<-25	dB



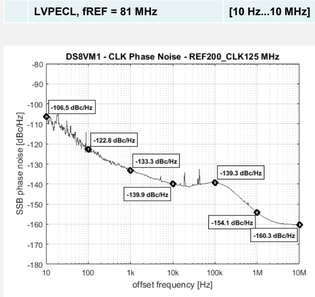
S_{11} for DC coupled channels

Clock generation

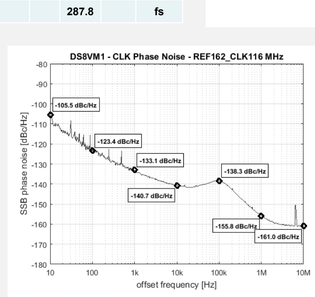
Parameter	Conditions and comments	Result			Unit
		Min	Typ.	Max	
CLOCK SECTION					
CLK input frequency range	3dB bandwidth, Based on measurements and datasheet	30		950	MHz
CLK input power level		0		13	dBm
CLK output frequency range	3dB bandwidth	30		950	MHz
CLK output power level			tbd		dBm
CLK input/output return loss	MMCX connector		tbd		dB
REF input frequency range	with REF divider set to DIV by 4	200		2000	MHz
	without REF divider	10		500	MHz
REF input power level	without Channel 7 REF monitoring	10	20	22	dBm
	with Channel 7 REF monitoring	15	20	22	dBm
Single-PLL mode (internal VCO)					
CLK RMS timing jitter at 125 MHz	[10 kHz…250 MHz]²		294.7		fs
LVPECL, fREF = 200 MHz	[10 Hz…10 MHz]		127.1		fs
CLK RMS timing jitter at 116 MHz	[10 kHz...250 MHz]²		294.3		fs
LVPECL, fREF = 162.5 MHz	[10 Hz…10 MHz]		129.4		fs
Single-PLL mode (external VCO)					
CLK RMS timing jitter at 78 MHz	[10 kHz…250 MHz]²		786.0		fs
LVPECL, fREF = 260 MHz	[10 Hz...10 MHz]		447.6		fs
CLK RMS timing jitter at 108 MHz	[10 kHz...250 MHz] ²		573.7		fs
LVPECL, fREF = 81 MHz	[10 Hz...10 MHz]		287.8		fs



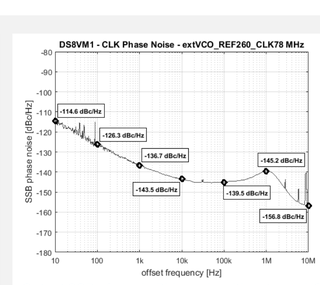
Dual PLL operation, with TCLKA at 54 MHz as reference, coming from x2timer via MCH. PLL settings are not optimized. PLL1 loop bandwidth at ~3 kHz, PLL2 loop bandwidth at ~40 kHz. Jitter cleaned from 10-15 ps down to 2.6 ps at 115 MHz clock frequency.



CLK output SSB phase noise; in single PLL mode with internal VCO (LMK04906), locked to 200 MHz reference (R&S SMC100), generate 125 MHz output clock.



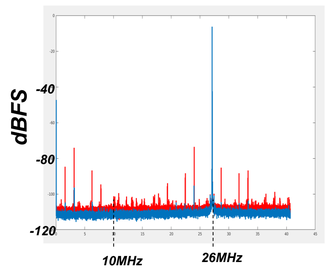
CLK output SSB phase noise; in single PLL mode with internal VCO (LMK04906), locked to 162 MHz reference (R&S SMC100), generate 116 MHz output clock.



Output SSB of single PLL mode with external VCO (CVCO55CL-0305-0345), locked to 260 MHz reference (R&S SMC100), generate 78 MHz output clock.

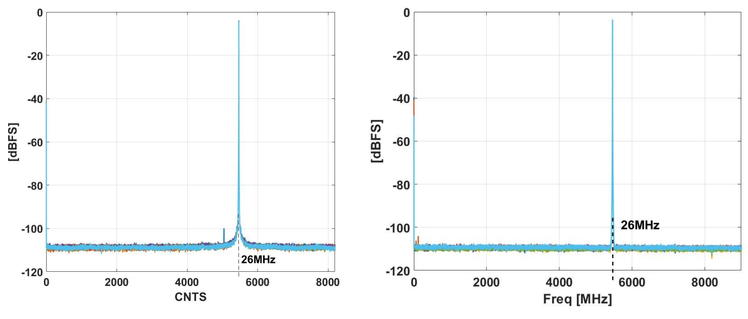
Design decisions for next revision

- We omit the PLL loop locked to the external VCO. For a single PLL mode there is no performance advantage
- The external VCXO is only used in dual-PLL mode
- The output divider of the clock distribution has to be set at maximum possible value
- The clock lines feeding the LMK04906 have to be differential
- The F_{in} pin of the LMK04906 needs an LVPECL buffer at the input
- Omit additional DC/DC converter for voltages for the clock tree
- The next revision of the DRTM-DS8VM1 (revision 1.3) will tentatively be available in Q1 2020 by SIS struck innovative systeme



Long investigation process

- EMI (external, internal)
- PLL operation
- Heat sources on the board, overheating
- Power distribution
- Control circuitry and its influence



*m.hoffmann@desy.de

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