Digital Low-Level RF Control System for the Advanced Light Source Storage Ring

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   - Loop Performance
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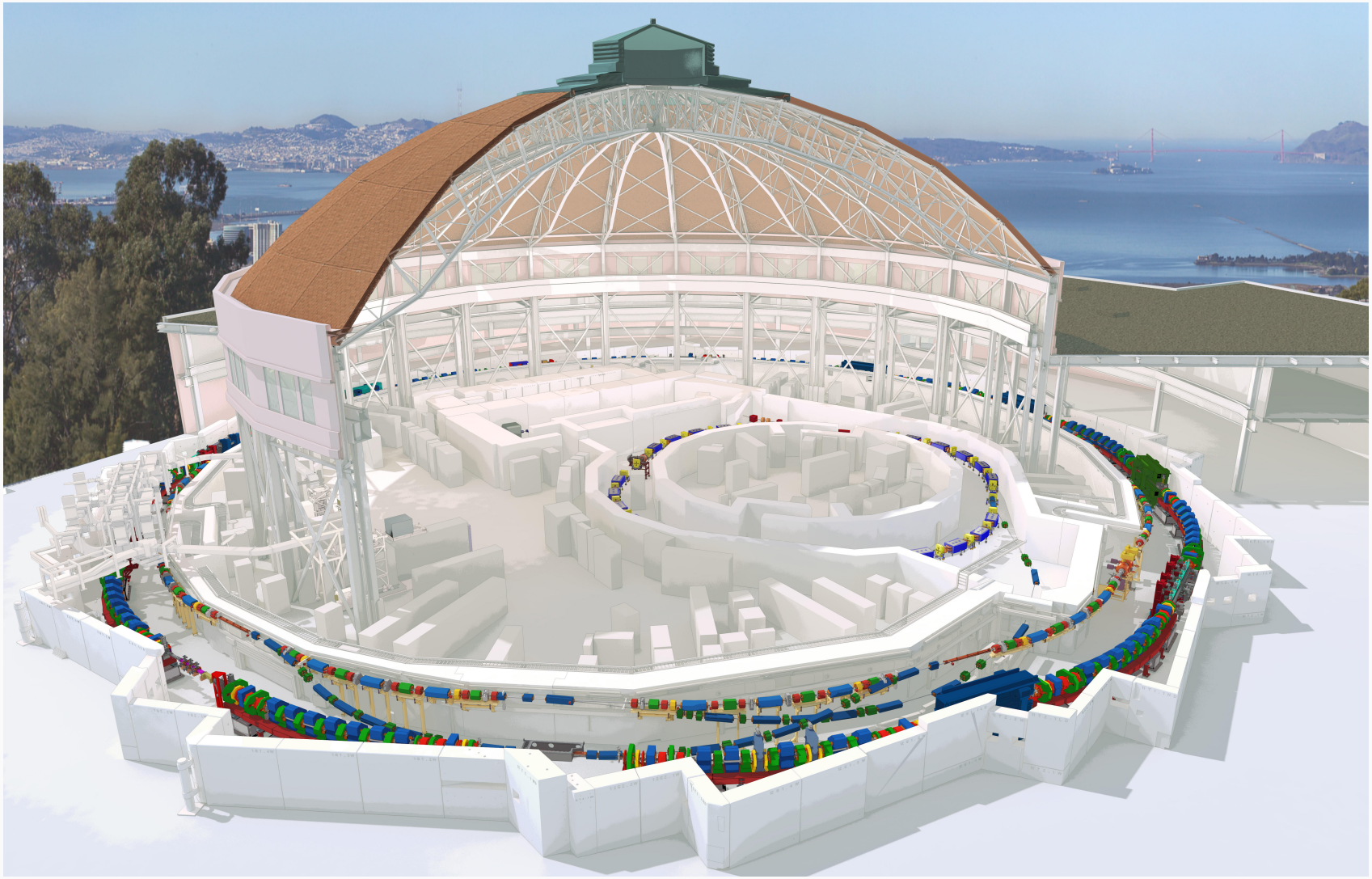
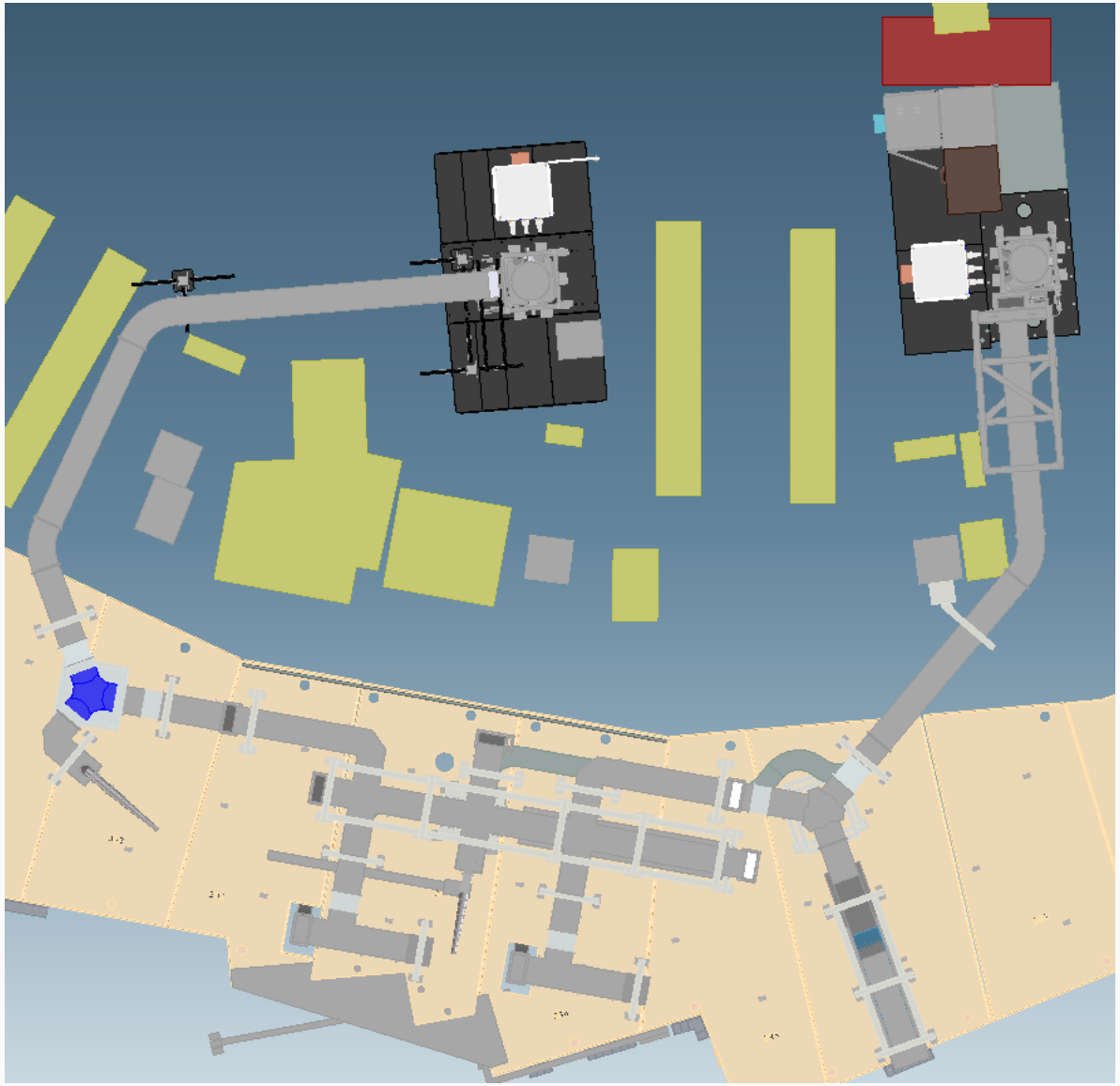
Introduction

Advanced Light Source at Berkeley Lab



ALS: 1.9GeV 500mA synchrotron light source since 1993,
with upgrade ALS-U started 2018 Image Credit: Berkeley Lab

ALS Storage Ring RF: Two 300kW Klystrons Driving Two Cavities



ALS Storage Ring RF system: two klystrons with waveguide matrix

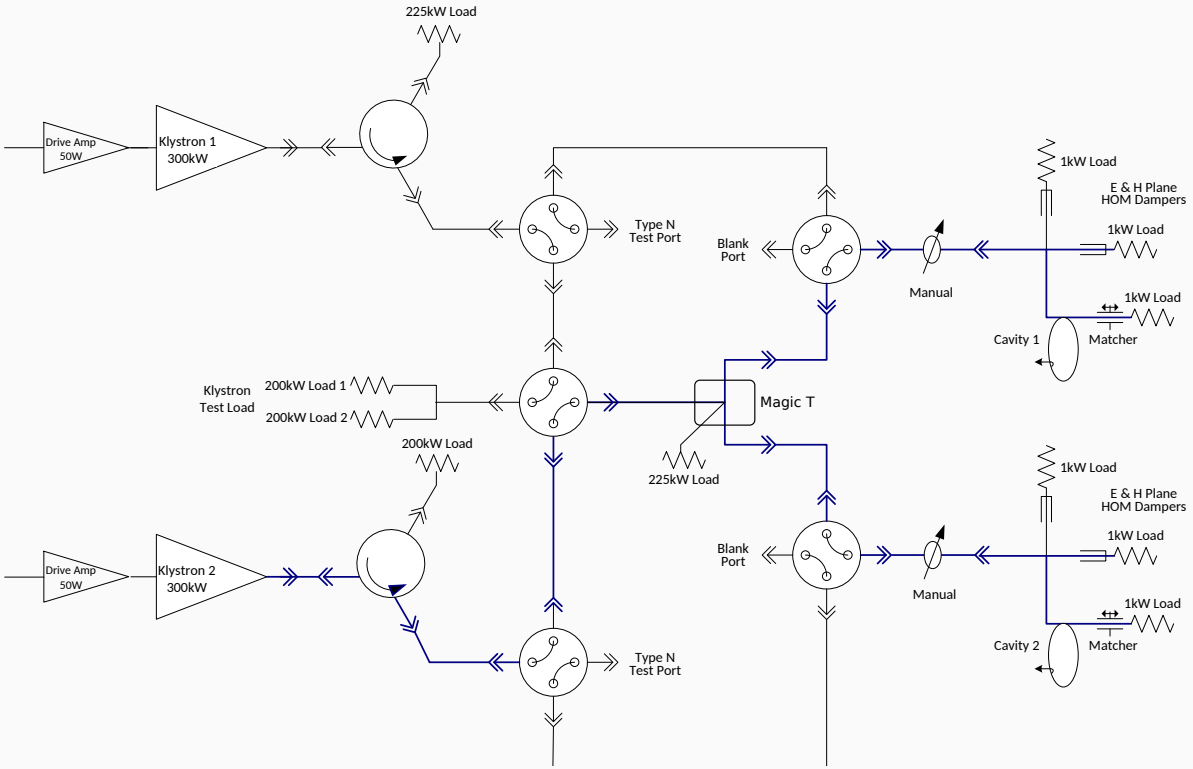
ALS Storage Ring RF: Two 300kW Klystrons Driving Two Cavities

	ALS SR 1.9GeV	ALS-U SR 2.0GeV	
Cavity RF Frequency	499.64	500.394	MHz
Number of Cavities	2	2	
$\frac{R}{Q}$ (ea)	4.9	4.9	MΩ
Cavity voltage	671	300	kV
β	2.9	10.07	
Energy loss per trun	329	329	keV
BM Beam Power	141	125	kW
ID Beam Power	42	35	kW
3HC Beam Power	7.3	4.4	kW
Parasitic Beam Power	2.9 (est.)	2.2 (est.)	kW
Total Beam Power	192.9	166.9	kW
Cavity Power(no beam)	46	9.2	kW
Cavity Power(beam)	142.5	127.6	kW
Waveguide Loss	9.2 (est.)	2.6 (est.)	kW
High Power Amplifier	294.0	257.8	kW

Klystron Site 1 with -56kV HV Switch

Klystron Site 2 with Mod-anode

Need for ~~Analog~~ Digital Low–Level RF system



Configurable waveguide mode to drive two cavities

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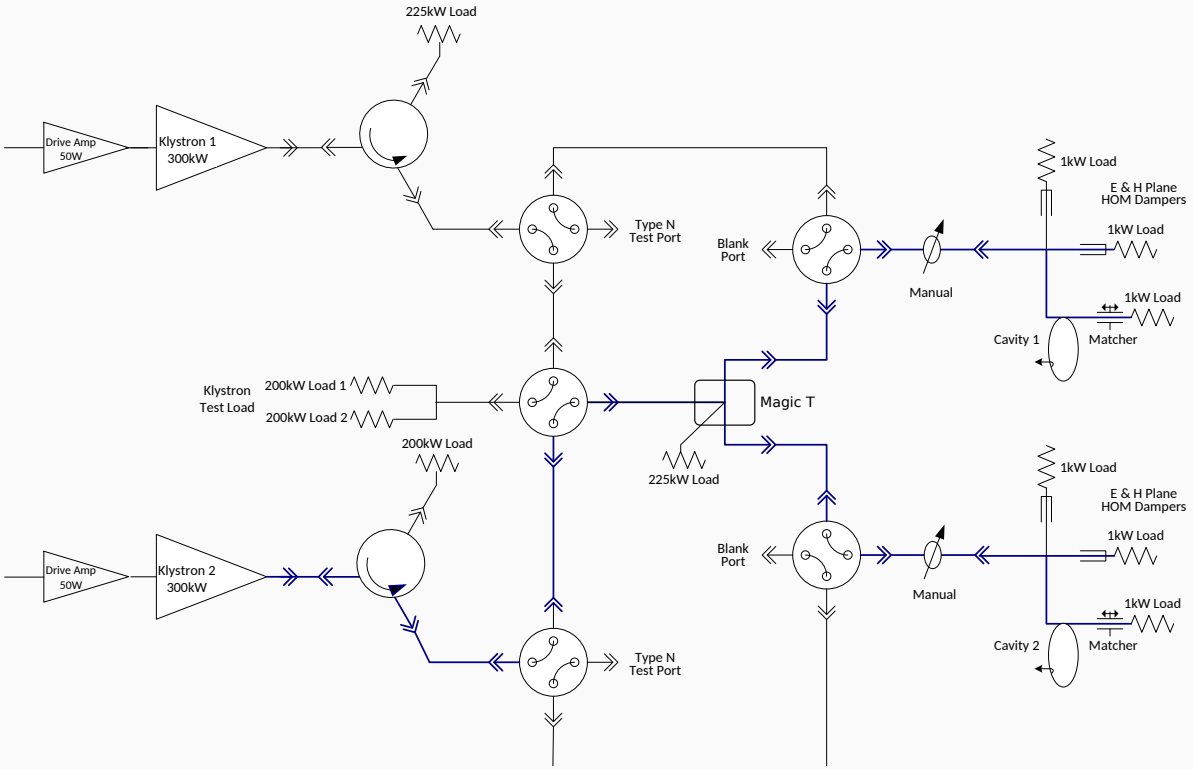
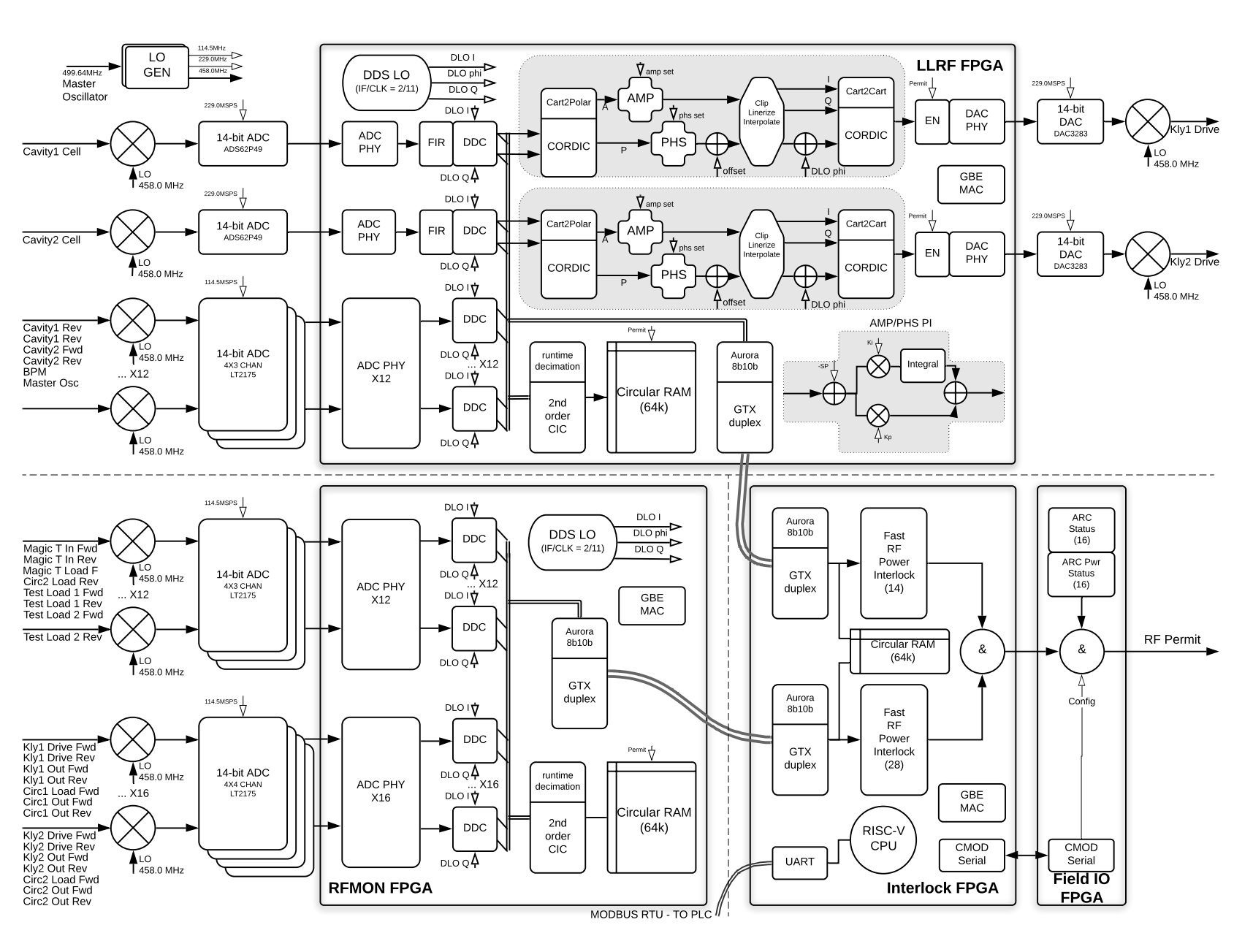


Configurable waveguide mode to drive two cavities

Requirements	
Num. Klystrons	2
Num. Cavities	2
Num. Signals	42
f_{RF}[MHz]	499.65
Cavity Q_0	28670
Cavity Q_L	16700
Cavity τ	10.6 μs
Revolution Freq.	1.5 MHz
Interlock	< 4 μs
Amp. stability	< 0.1 %
Phase stability	< 0.1 $^\circ$

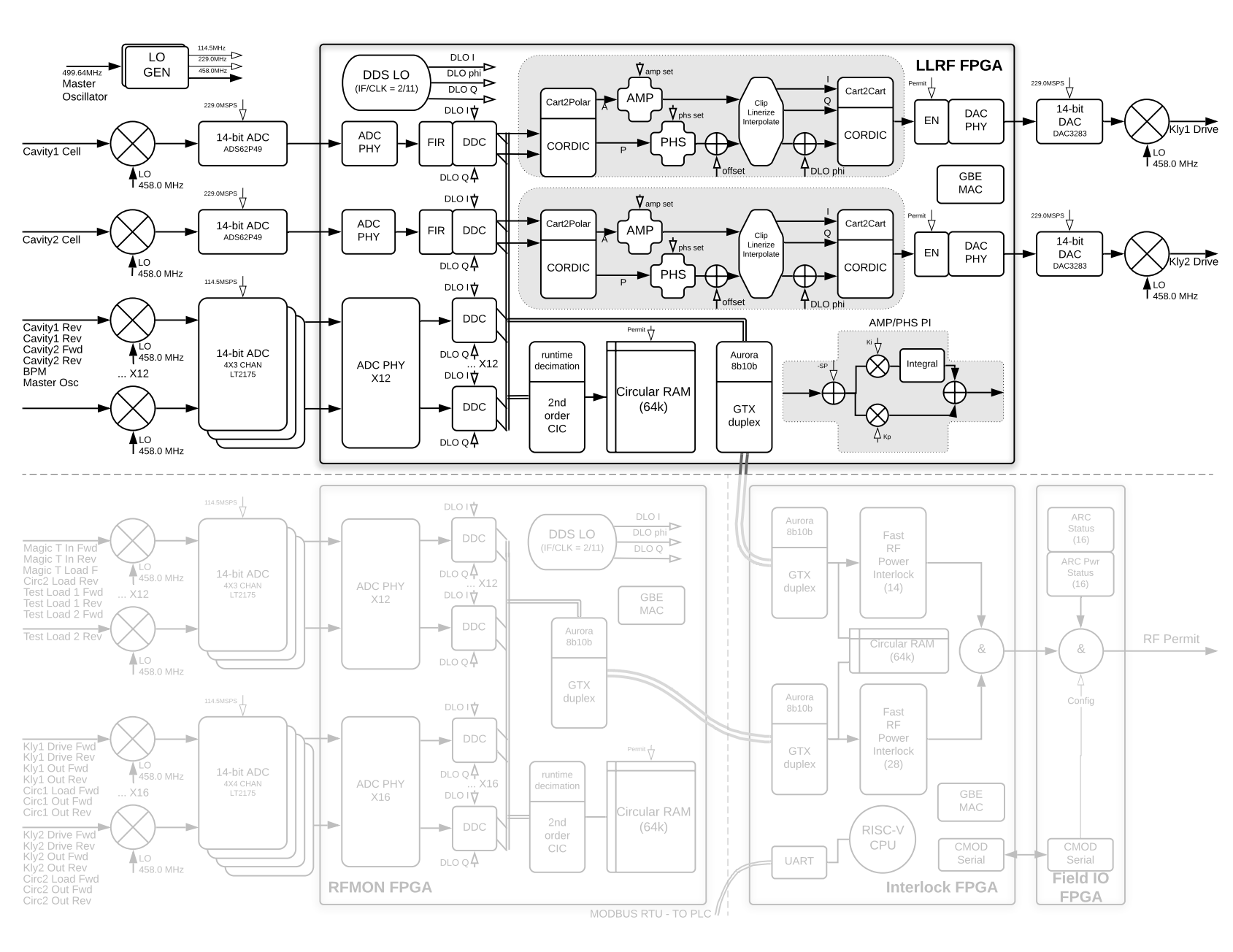
- Variable klystron gain
- Variable group delay
- Support all drive modes
- Software-free operation

ALS SRRF LLRF System Overview

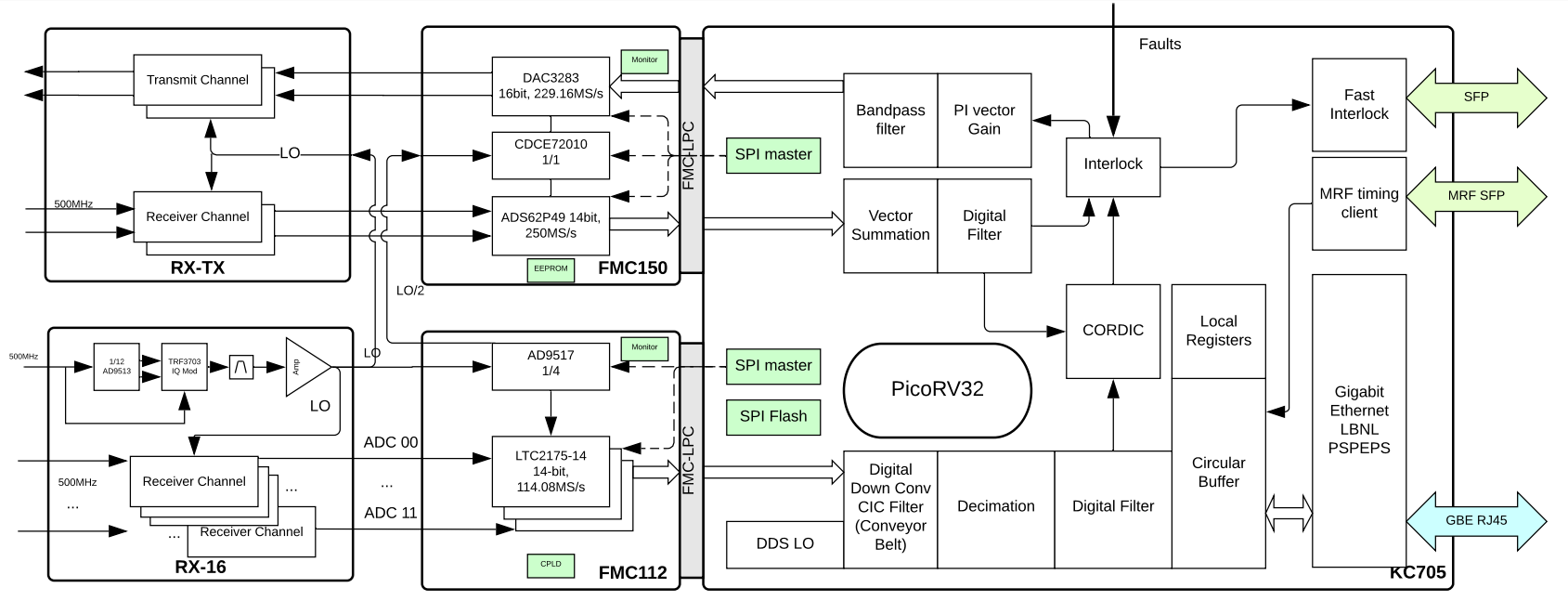


Hardware design

LLRF System Overview: Low-Level RF Chassis



Low-Level RF chassis at a glimpse



COTS : Commercial Off-the-shelf parts

ADC : 12 channel 14 bits ADC at 115Msps

2 channel 14 bits at 229Msps

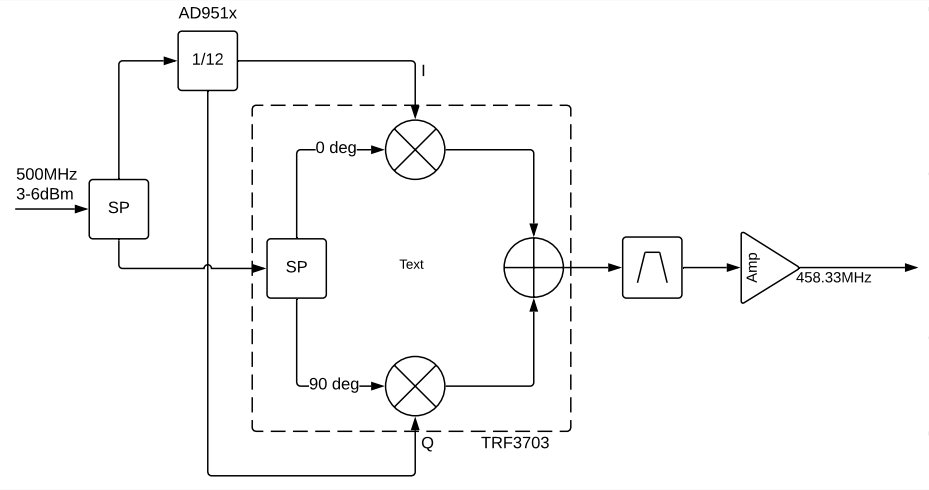
DAC : 2 channel 14 bits at 229Msps

LO : Single Side Band LO Generation

FPGA : Xilinx Kintex7 (KC705) at 229MHz clock

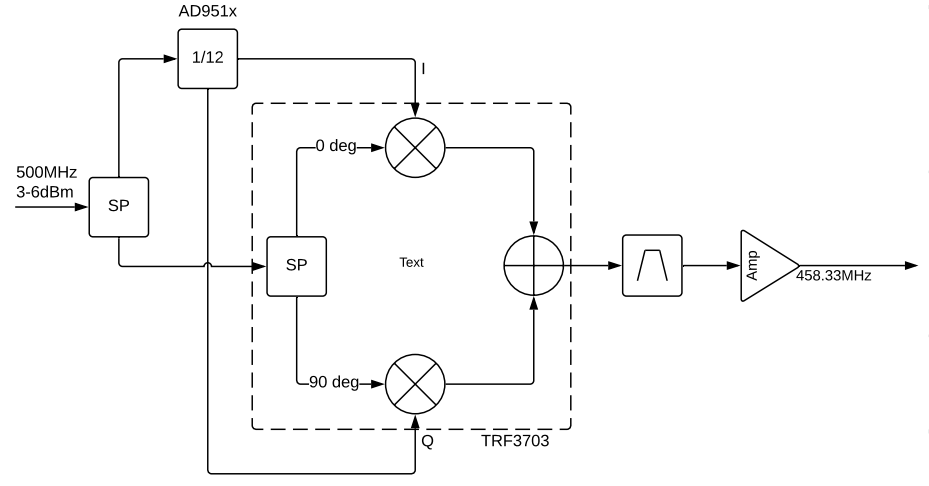
Ports : GBE, UART, GTX, MRF

Single Side Band LO Generation



Carrier feedthrough	-45.4 dB
Image suppression	-59.3 dB
MO phase jitter	107 fs (rms)
LO phase jitter	140 fs (rms)
LO stability	< 0.005 dBm

Single Side Band LO Generation



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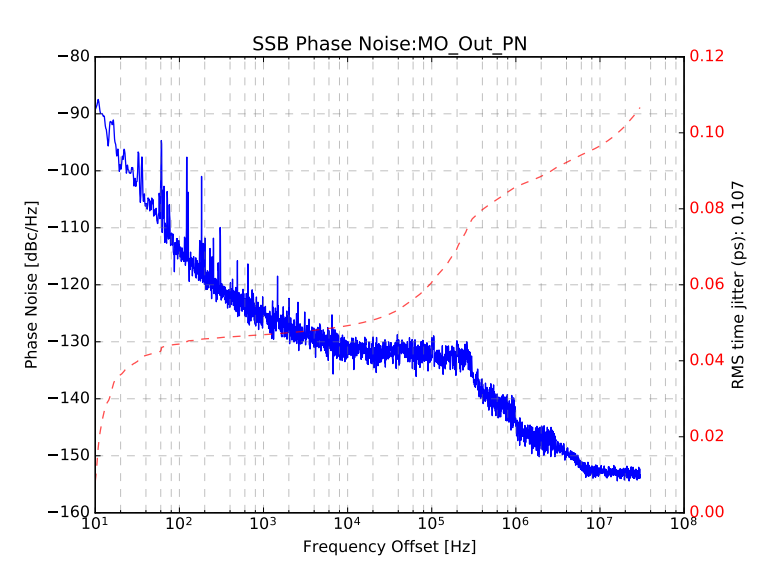
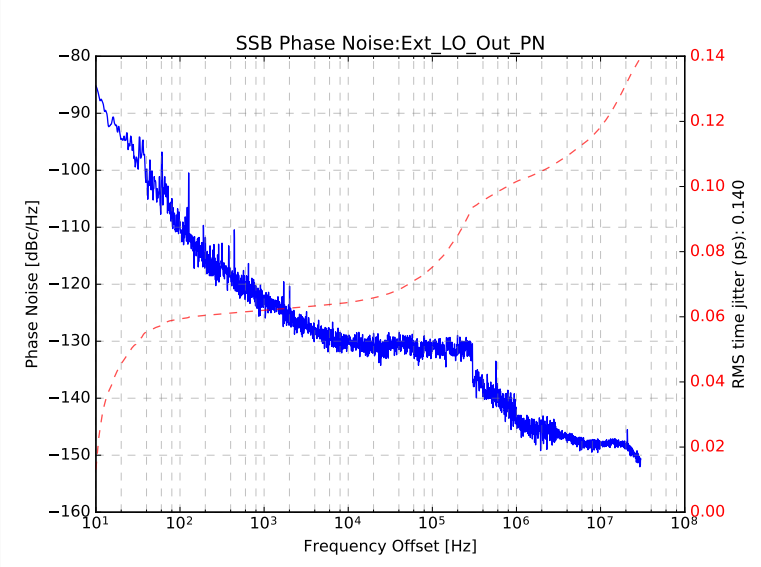
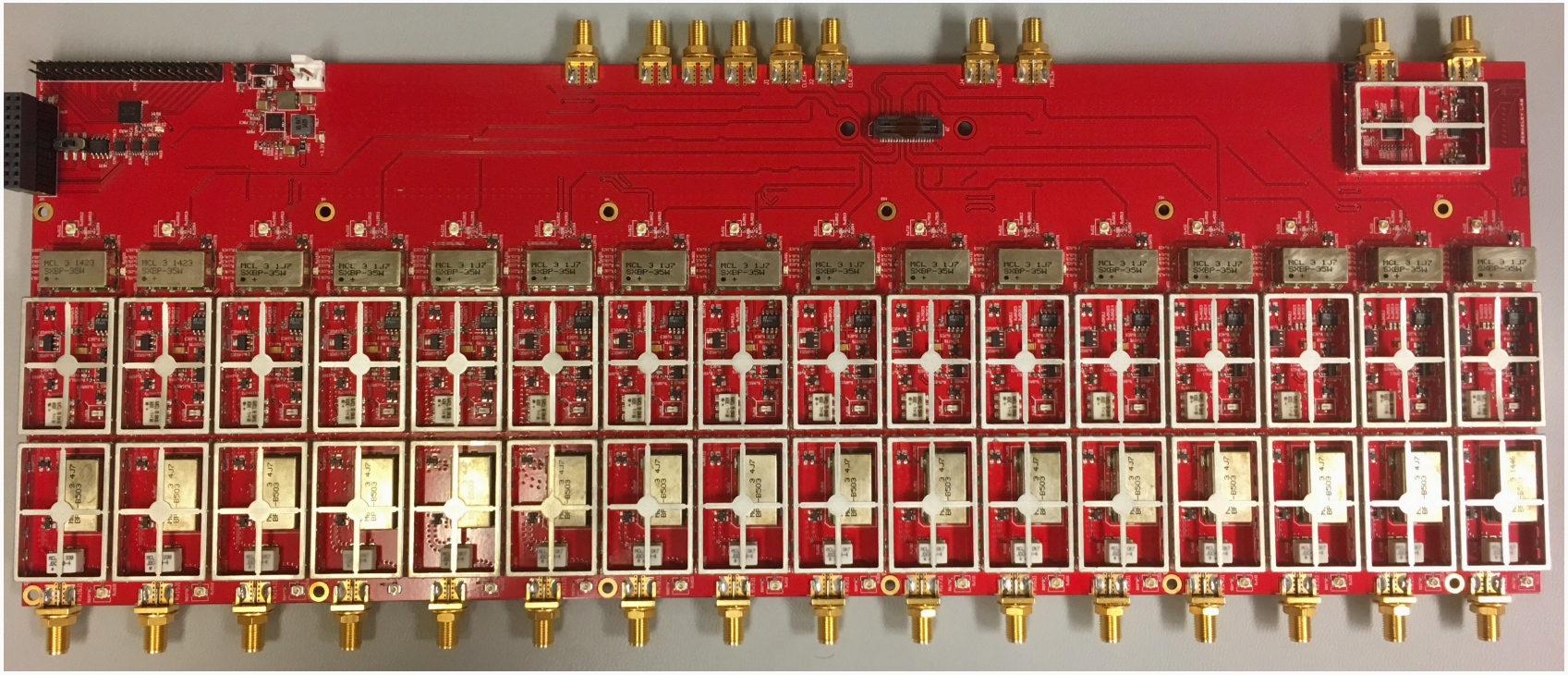


(a) External MO (R&S SMA100) Phase Noise



(b) Generated LO Phase Noise

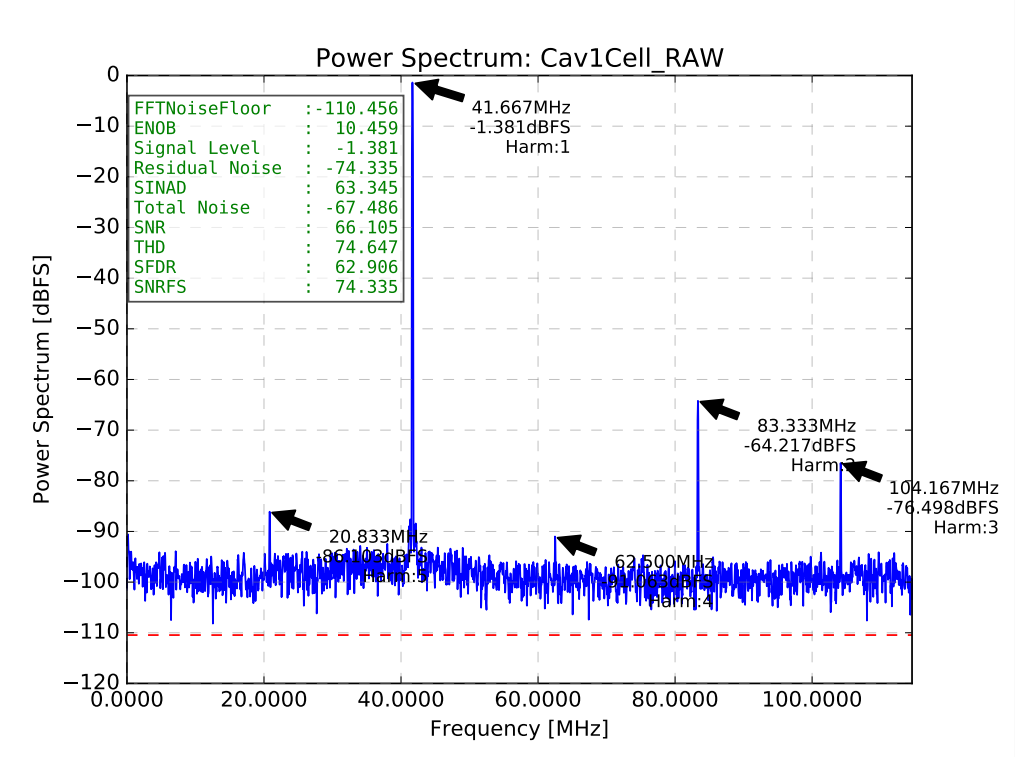
RX–16: Analog RF Down Converters



Stackable 16 channels down–converter, $\times 2$ per chassis

- Externally synchronized switch DC power supply;
- LO generation and distribution;
- Interface to FMC112/FMC116 digitizer;
- Housekeeping monitored through SPI;
- Channel isolations > 55 dB;

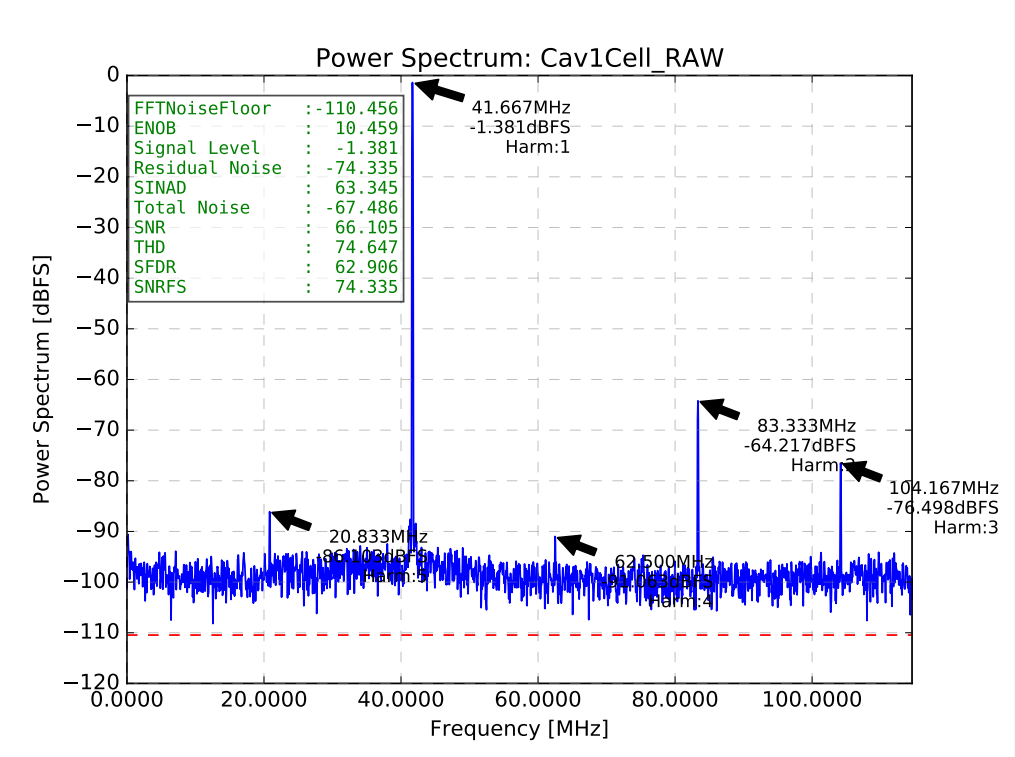
14-bit ADC Benchmark



FMC150 ADC1 spectrum

Signal–Noise Ratio	74.34 dBFS
Isolation (feedback)	$>$ 72 dB
Isolation (interlock)	$>$ 50 dB

14-bit ADC Benchmark



FMC150 ADC1 spectrum

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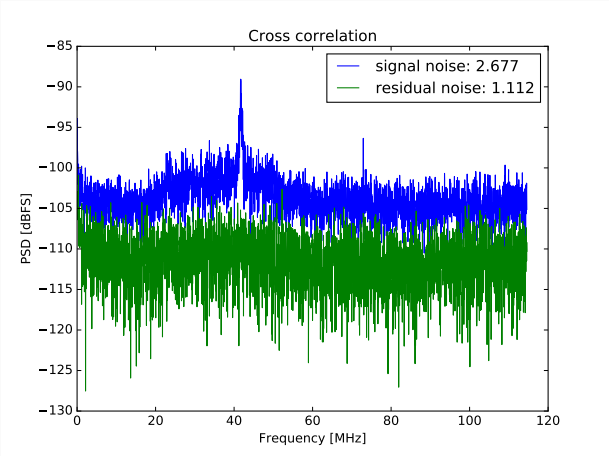
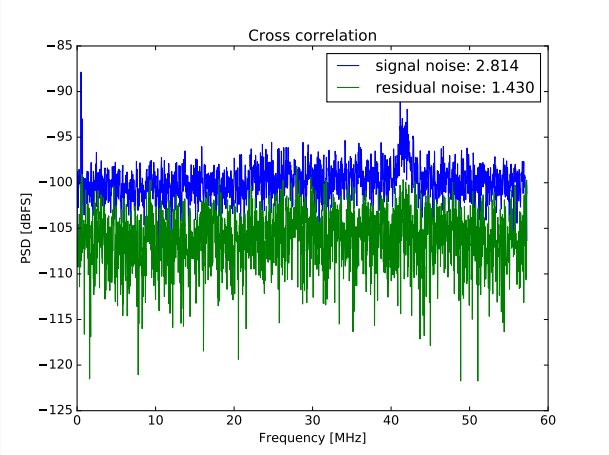
How to get pure ADC noise?

Cross–correlation. [1]

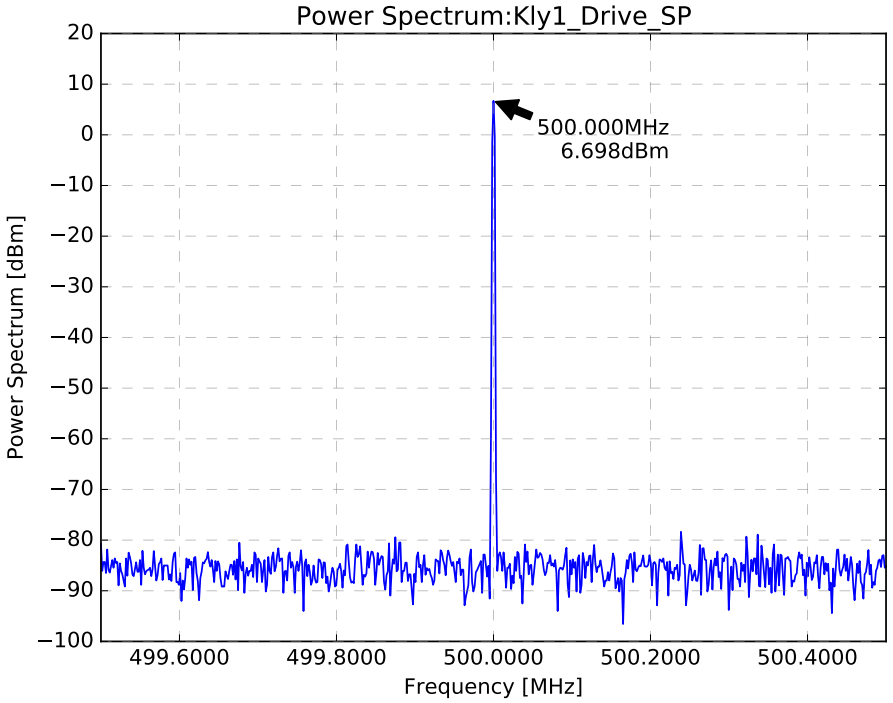


(a) FMC150 residual noise



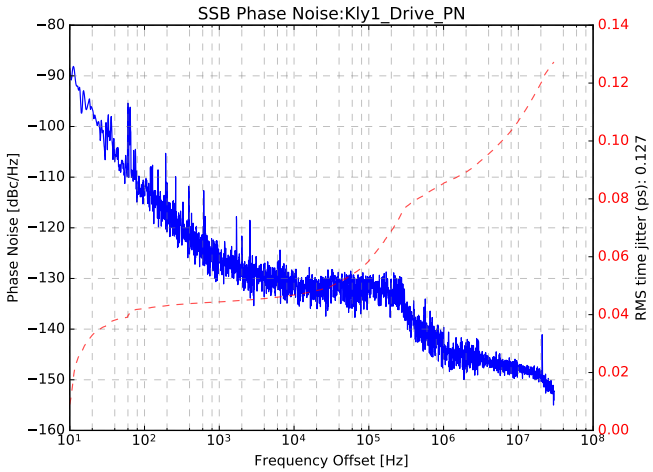
(b) FMC112 residual noise

14-bit DAC Benchmark

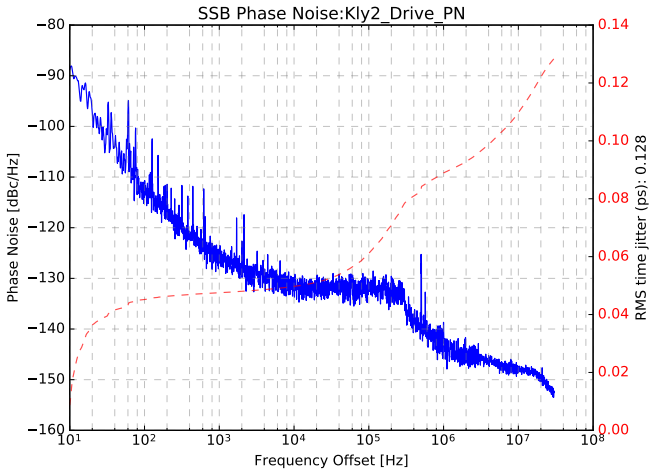


DAC1 power spectrum

DAC1 phase jitter [1Hz, 20MHz]	127 fs
DAC2 phase jitter [1Hz, 20MHz]	128 fs

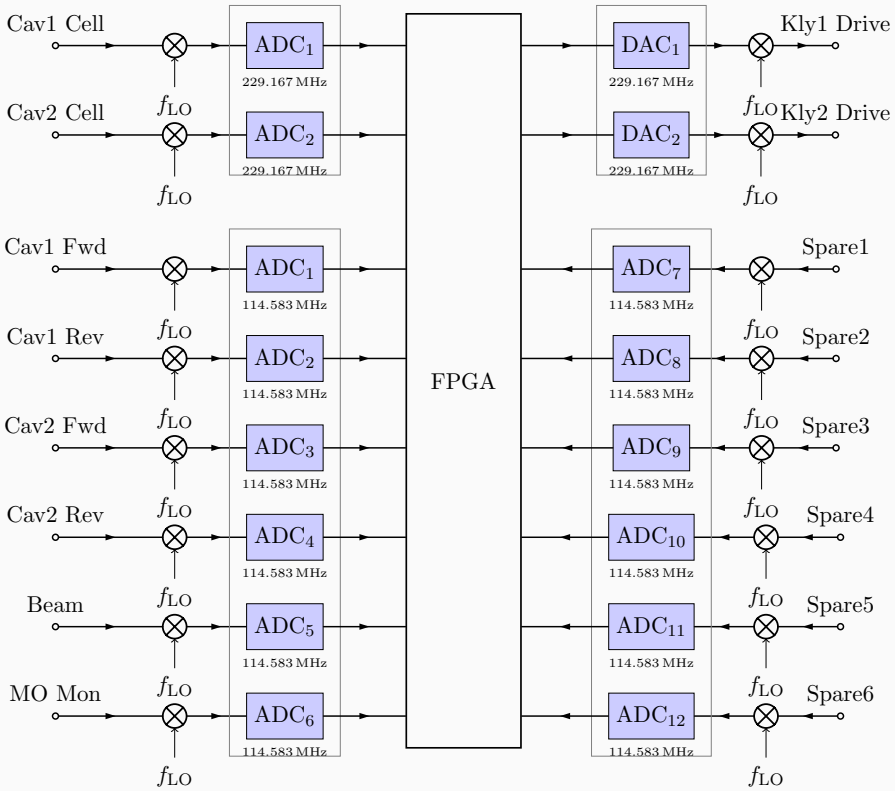


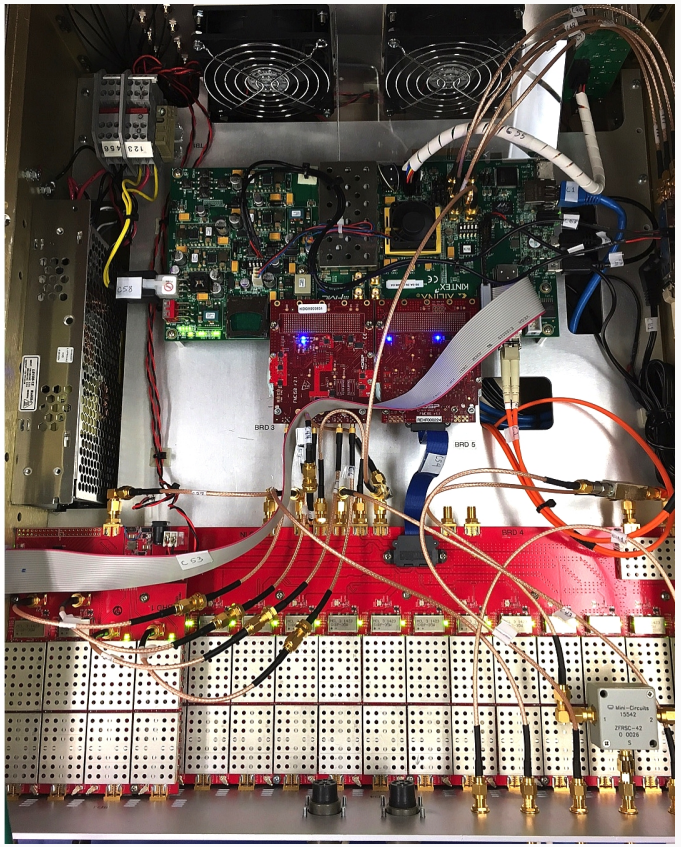
(a) DAC1 phase noise



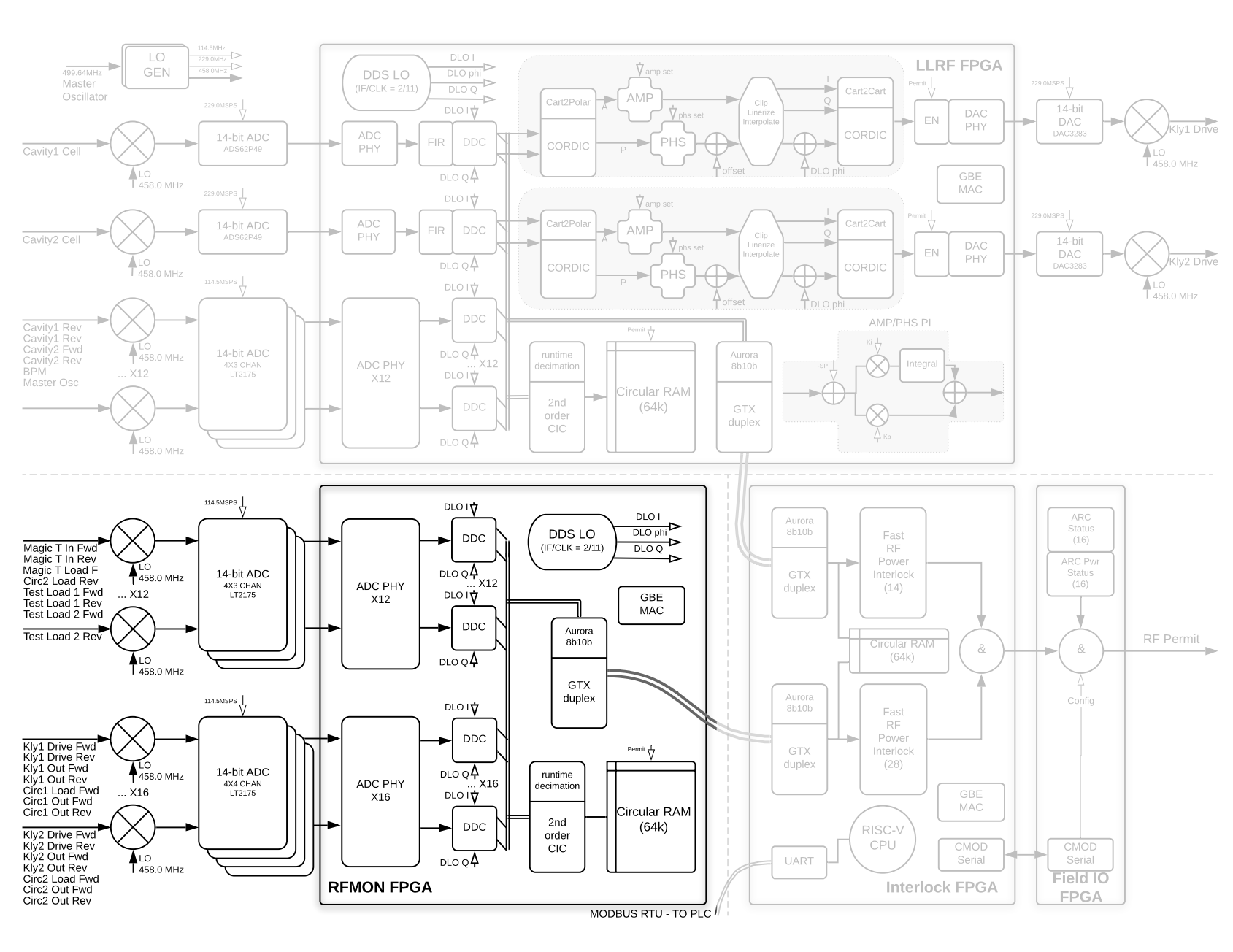
(b) DAC2 phase noise

LLRF chassis in production

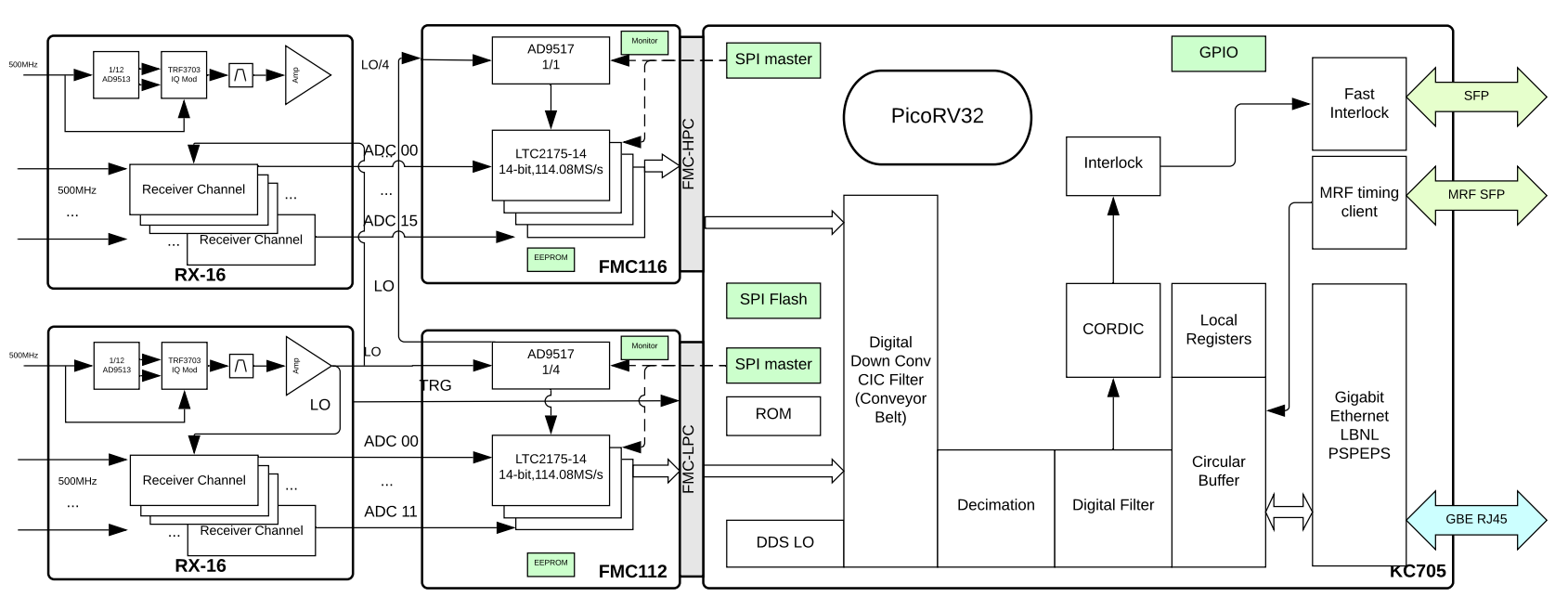




LLRF System Overview: RF Monitor Chassis



RF Monitor chassis at a glimpse



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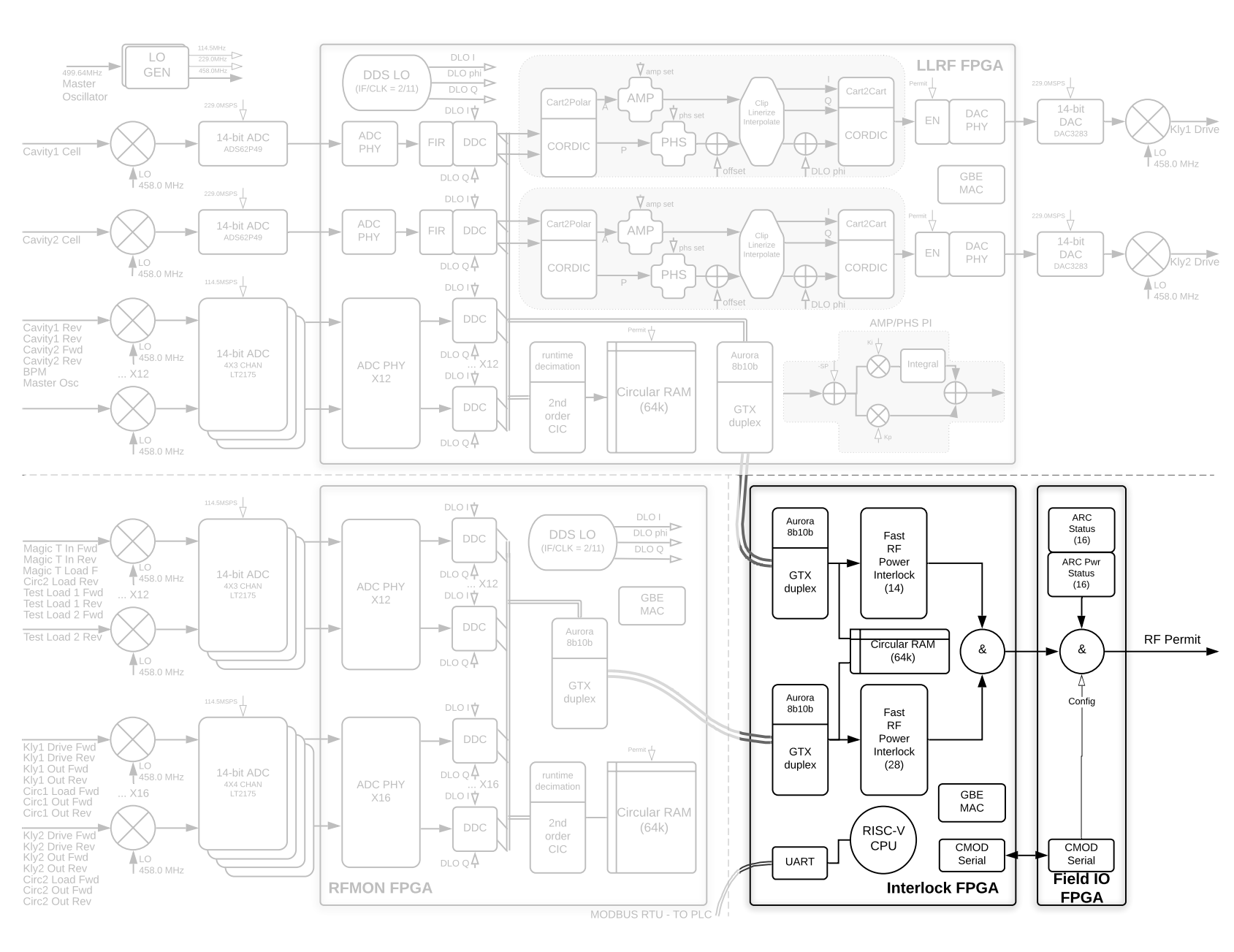
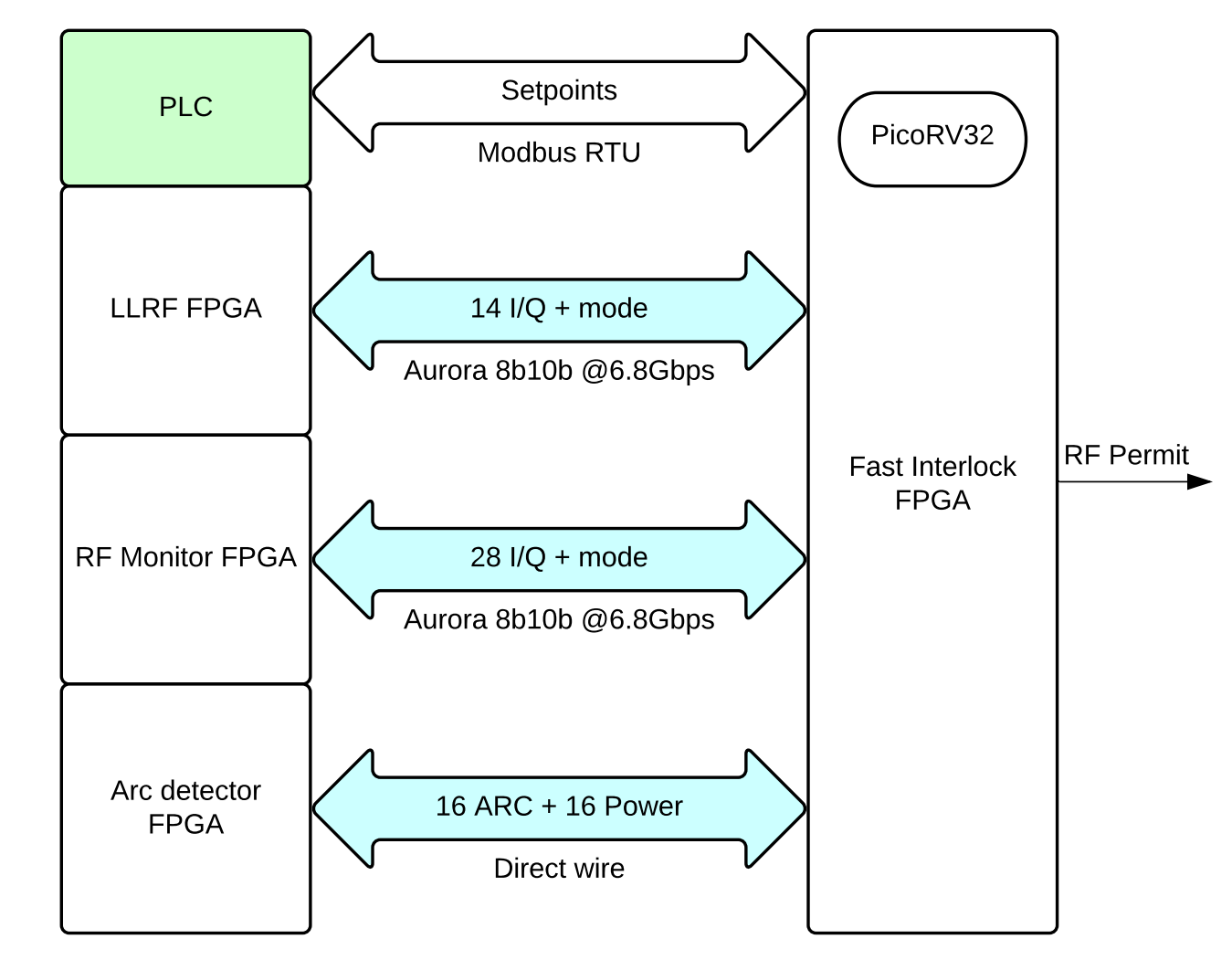
Ports : GBE, UART, GTX, MRF

LLRF System Overview: Fast Interlock

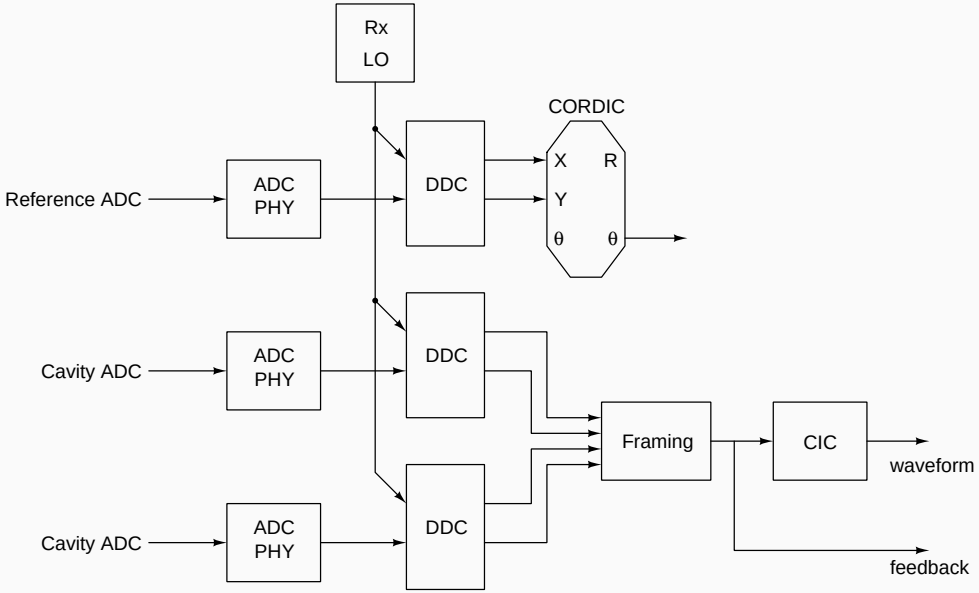


Fast Interlocks: RF Power and ARC detector



Firmware design

Firmware Overview

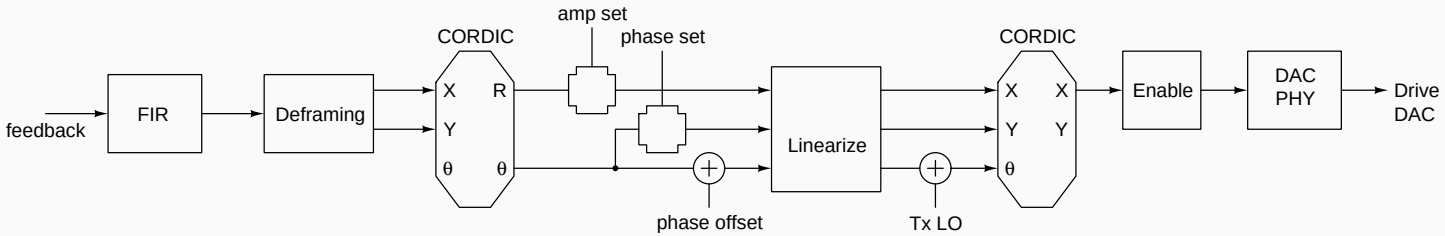


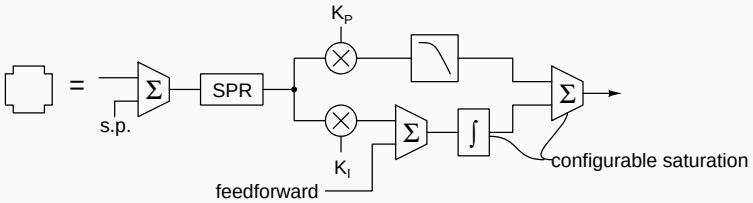
Notes and diisclaimers:

Data path schematic only, some of it does not map 1:1 to hardware

Not shown:

- Clocks and other timing
- Host/controller access/monitoring
- Upconverter interpolation
- Detune measurement
- Reference line phase averaging
- Hooks for Beam-Based Feedback





Non-IQ sampling Direct Digital Down-conversion

Non-IQ sampling avoids aliasing for high precision digitization.[2]

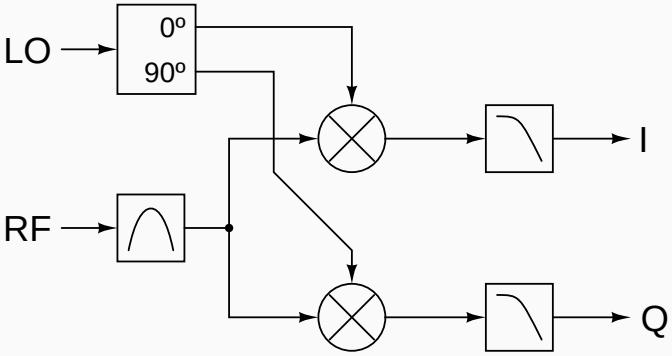
Both LO and sampling frequency are derived from ALS master oscillator f_{MO}:

$$f_{\mathrm{MO}} = 499.645\,\mathrm{MHz}$$
$$f_{\mathrm{LO}} = f_{\mathrm{MO}}\frac{11}{12} = 458.008\,\mathrm{MHz}$$
$$f_{\mathrm{IF}} = f_{\mathrm{MO}}\frac{1}{12} = 41.636\,\mathrm{MHz}$$
$$f_{\mathrm{Sample}} = f_{\mathrm{LO}}\frac{1}{2} = 229.004\,\mathrm{MHz}$$

With $\frac{f_{\mathrm{IF}}}{f_{\mathrm{Sample}}} = \frac{2}{11} = \theta \simeq 65.45^\circ$:

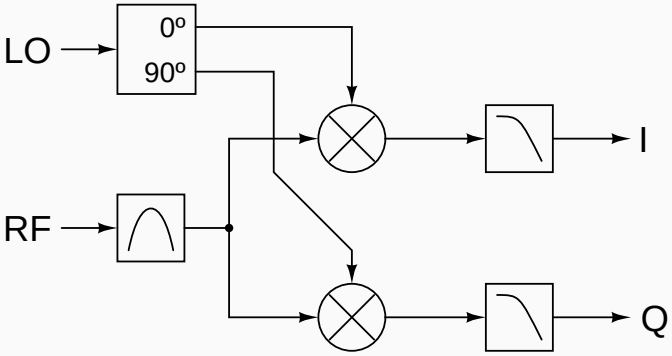
$$\begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix} = \begin{pmatrix} \cos(n\theta) & \sin(n\theta) \\ \cos((n+1)\theta) & \sin((n+1)\theta) \end{pmatrix} \begin{pmatrix} I \\ Q \end{pmatrix}$$
$$\begin{pmatrix} I \\ Q \end{pmatrix} = \frac{1}{\sin\theta} \begin{pmatrix} \sin((n+1)\theta) & -\sin(n\theta) \\ -\cos((n+1)\theta) & \cos(n\theta) \end{pmatrix} \begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix}$$

Non-IQ sampling Direct Digital Down-conversion



(a) Analog IQ Down-Conversion

Non-IQ sampling Direct Digital Down-conversion



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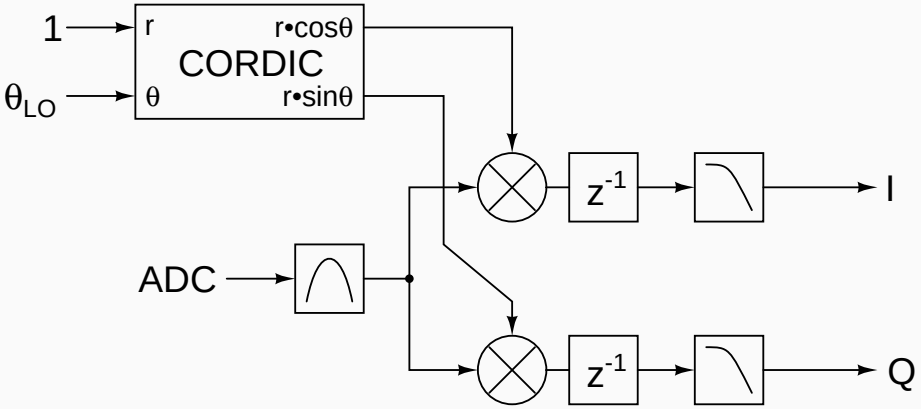
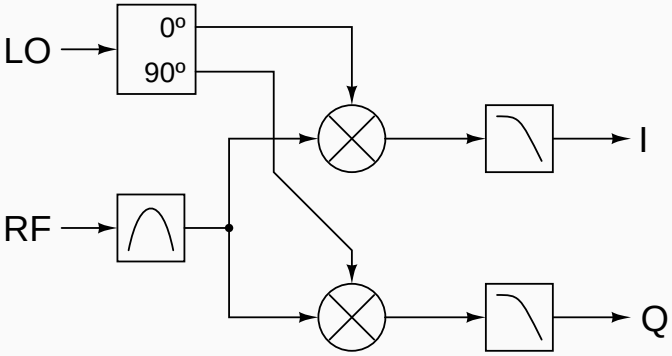


(b) Digital Non-IQ DDS

Non-IQ sampling Direct Digital Down-conversion



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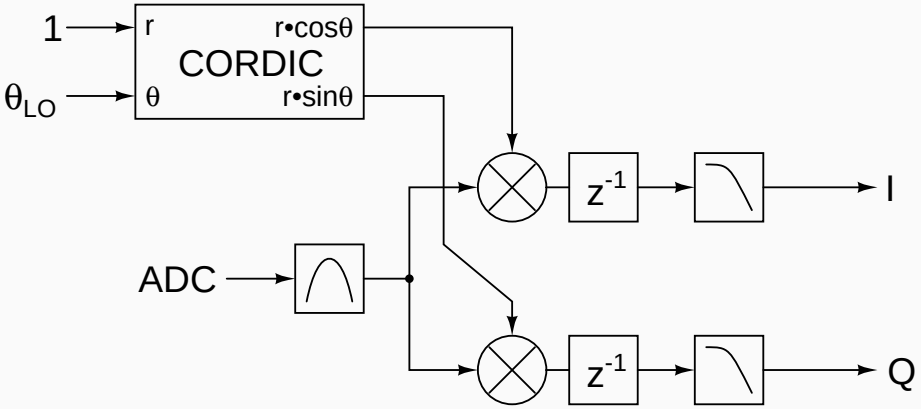
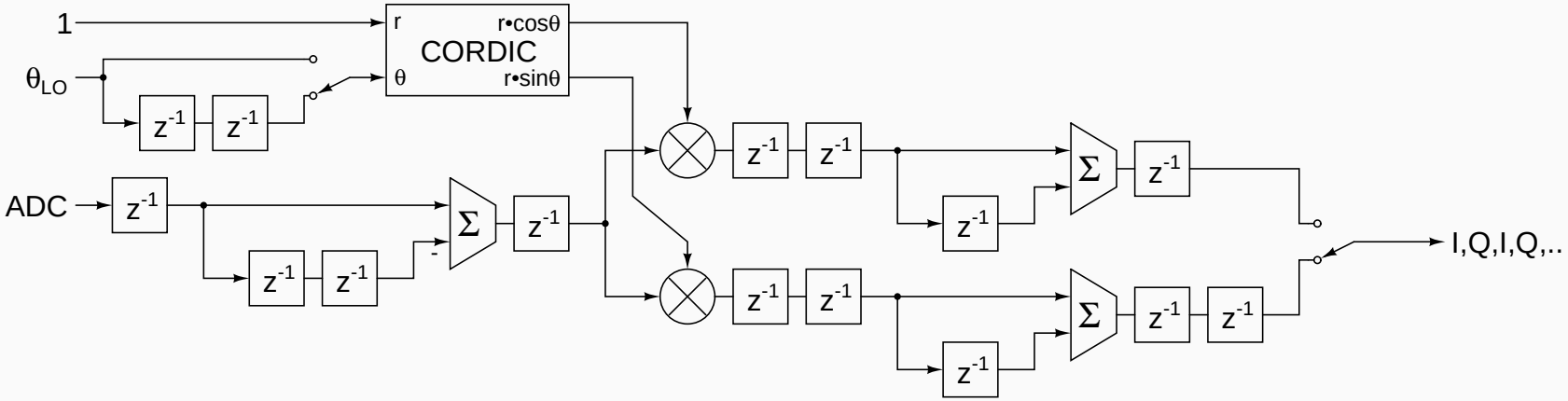
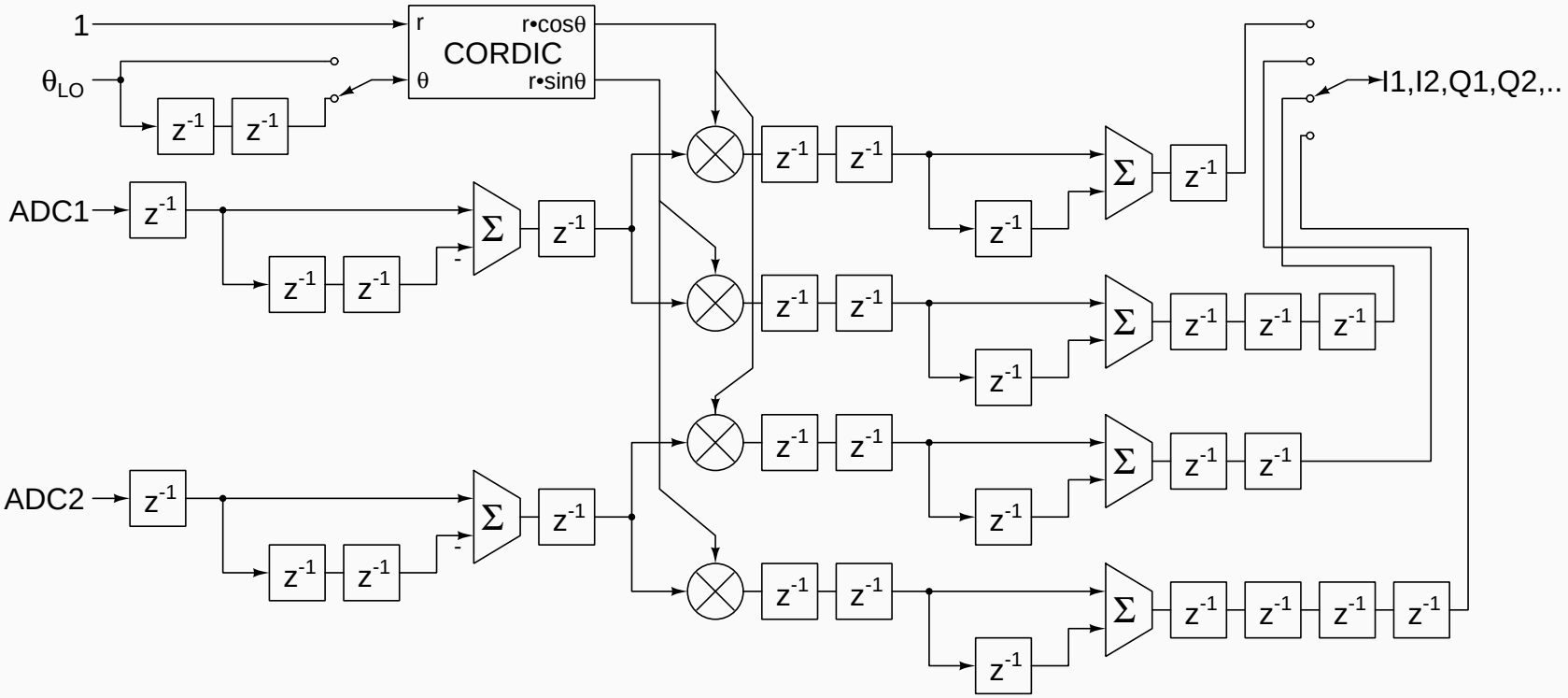


(b) Digital Non-IQ DDS



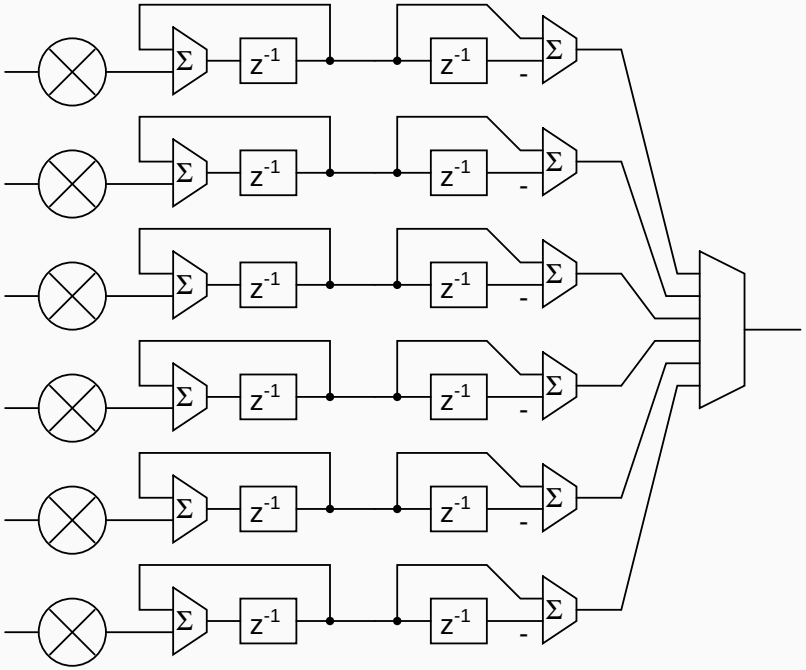
(c) Non-IQ DDS with digital filters and serialization

Double time: Serialized Dual Signal Path



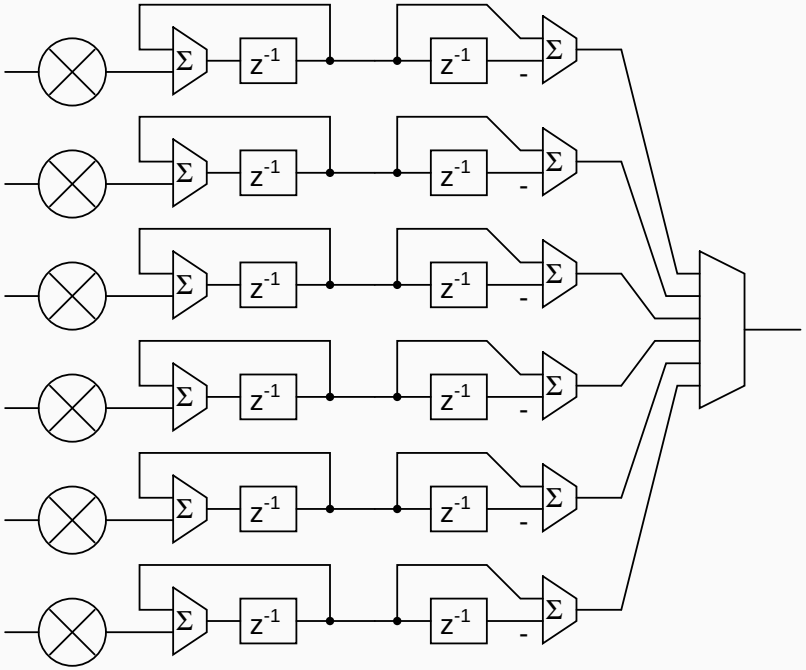
Two DSP clock cycles per ADC sample

Waveforms: Conveyor Belt with CIC filter



(a) Parallel

Waveforms: Conveyor Belt with CIC filter



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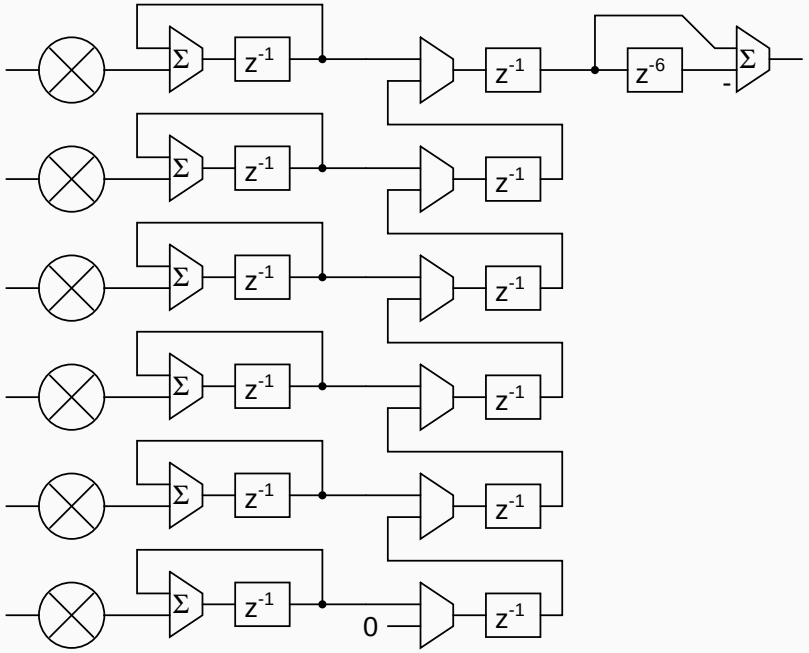
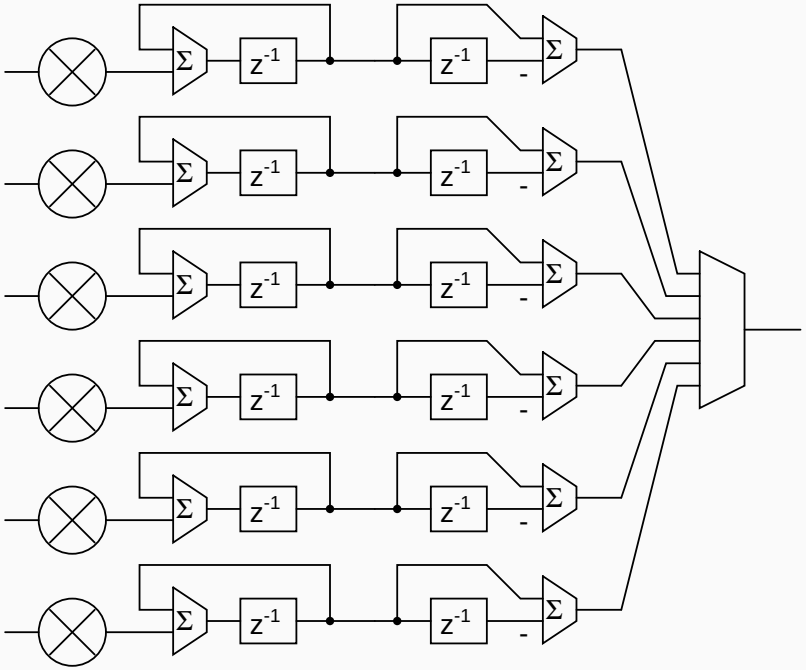


(b) Serial

Waveforms: Conveyor Belt with CIC filter



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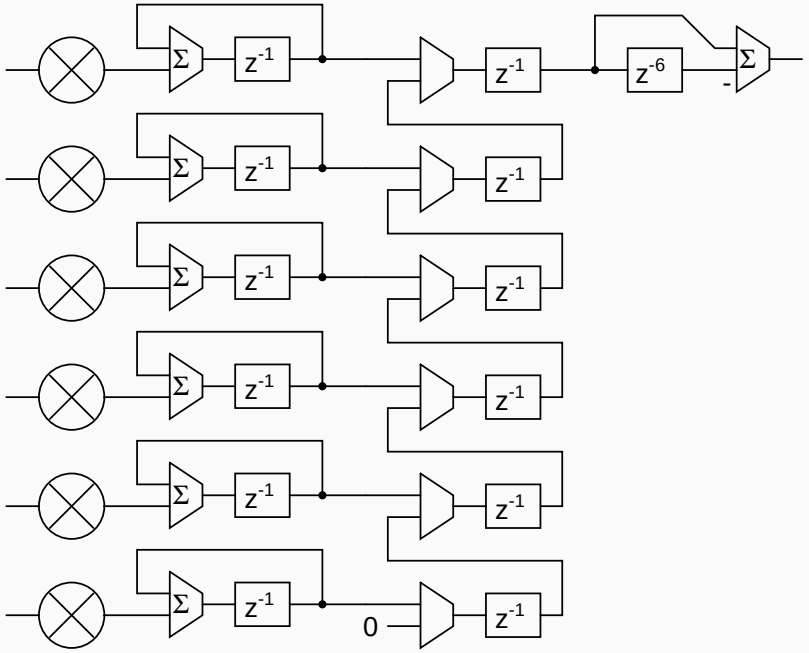


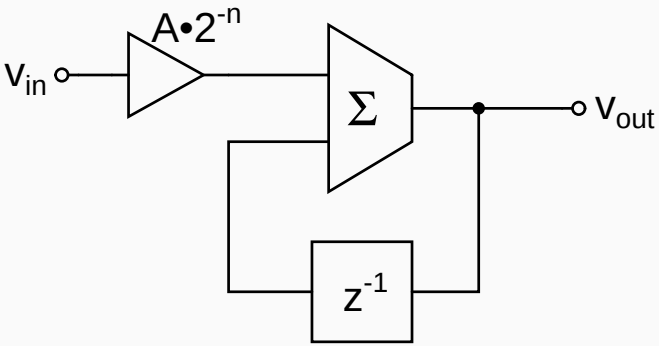
(b) Serial

Features:

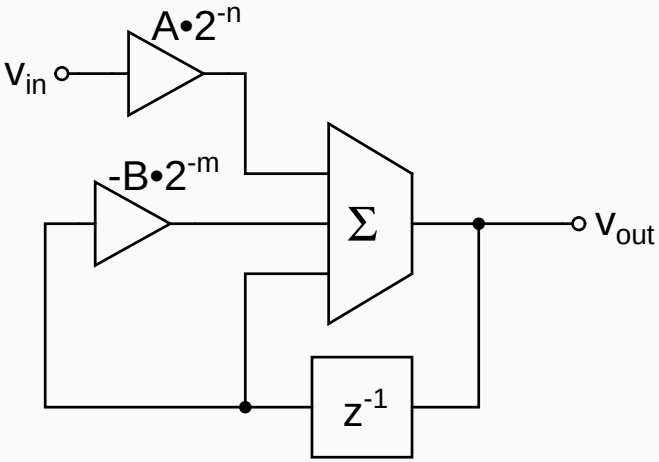
- Multi–channel selection;
- Ping–pong buffering to avoid read–write confliction;
- Configurable decimation factor;
- Fault capturing;
- Associated statistics for each channel with timestamps;

Feedback: Proportional–Integral Controller

$$C(z) = K_p + K_i \frac{1}{1 - z^{-1}}, \qquad T = \frac{4}{f_{\text{clk}}}$$



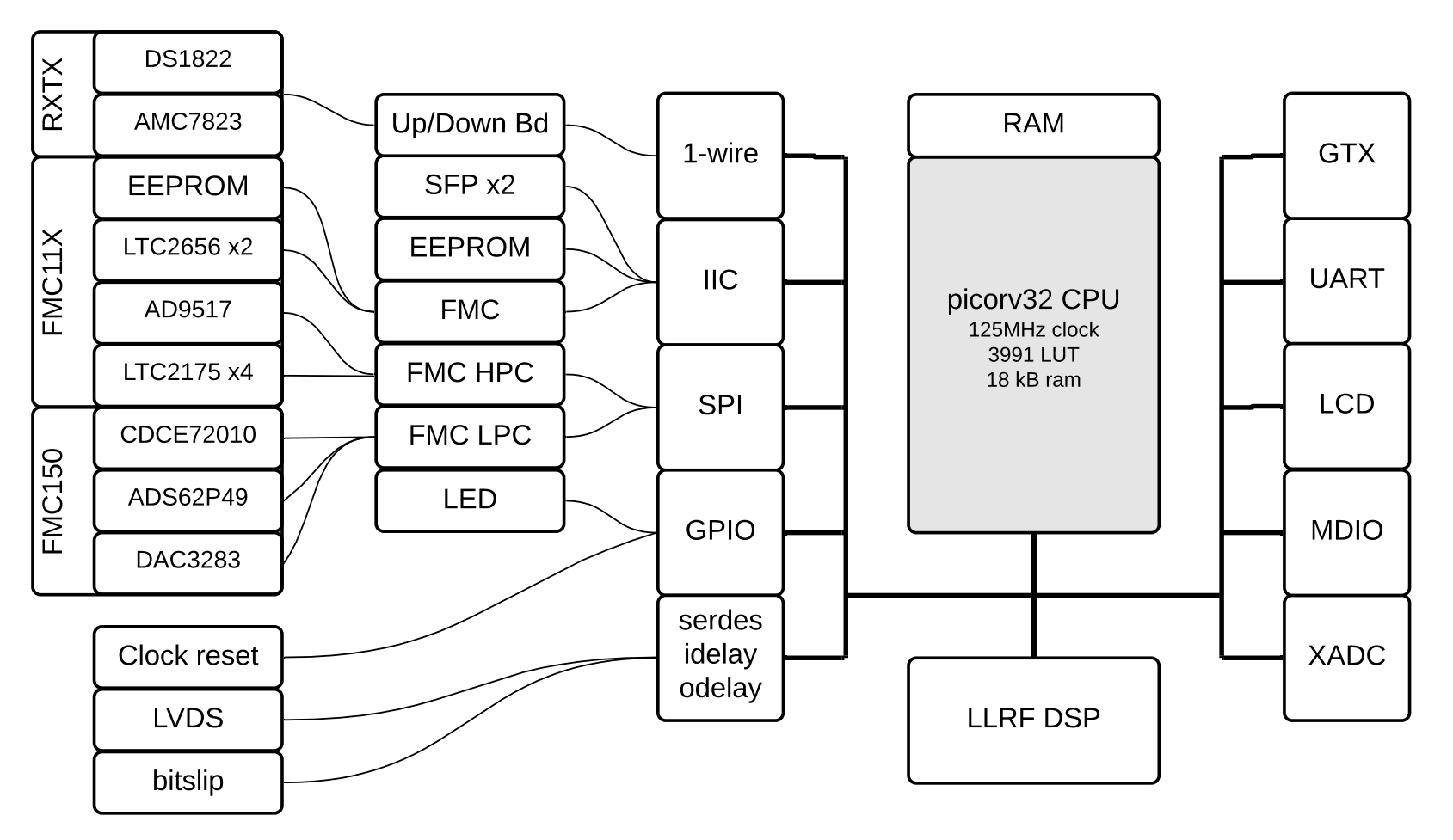
(a) Abstract of DSP integrator



(b) PI controller, with gain scaling

- Double time architecture
- Error slew rate limiter, output clip, reset, $\cdots$
- Simulated with an IIR virtual cavity in z domain;
- Calibrated control register scaling;

Housekeeping: Simple solution to complex hardware



Peripheral management and power–on initialization by CPU

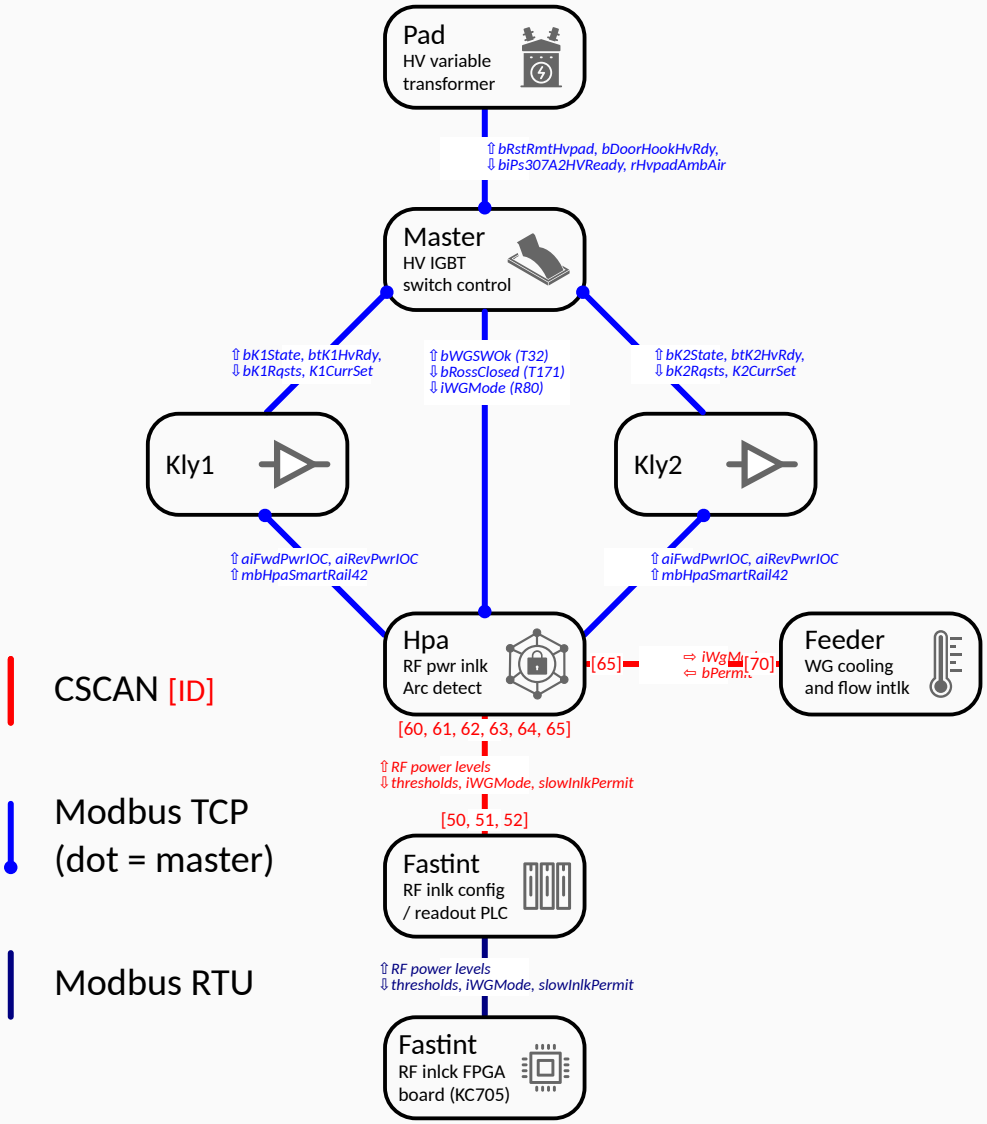
PicoRV32 – A Size-Optimized RISC–V CPU

PicoRV32 Features: [3]

- RISC–V RV32IMC instruction set
- Small (750–2000 LUTs) in 7-Series Xilinx Architecture
- High $f_{max} = 250 \sim 450$ MHz
- Native memory interface or AXI4-Lite or Wishbone master
- IRQ, Co-Processor interface (MUL, DIV)
- Open source: BSD license
- Open source standard RISC–V gcc cross–compiler

github.com/cliffordwolf/picorv32

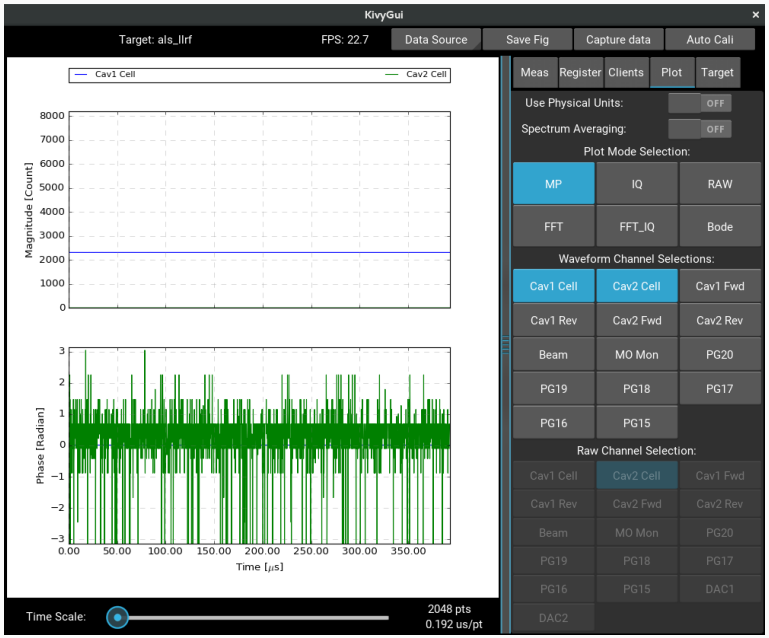
Standalone: Direct Interfacing with PLC via Modbus



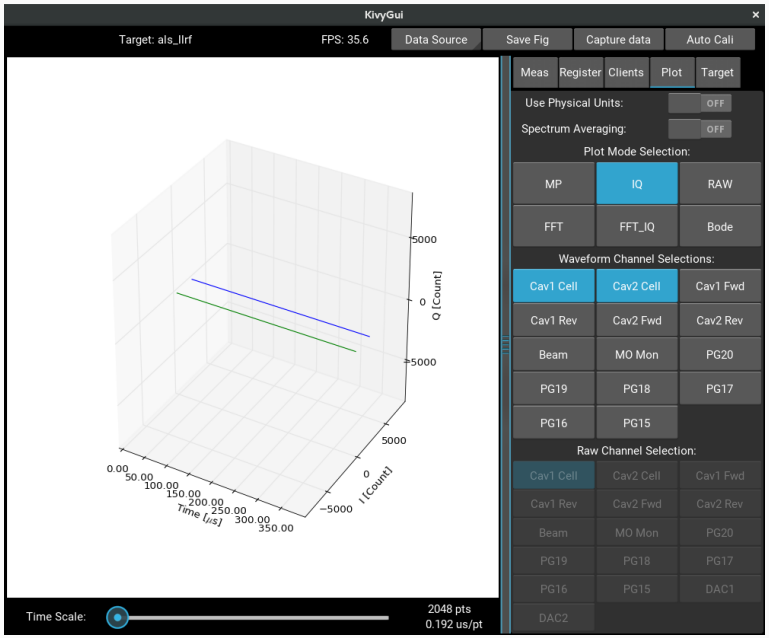
ALS SRRF PLC–FPGA interfaces

Software design

Engineering GUI: a python based standalone GUI

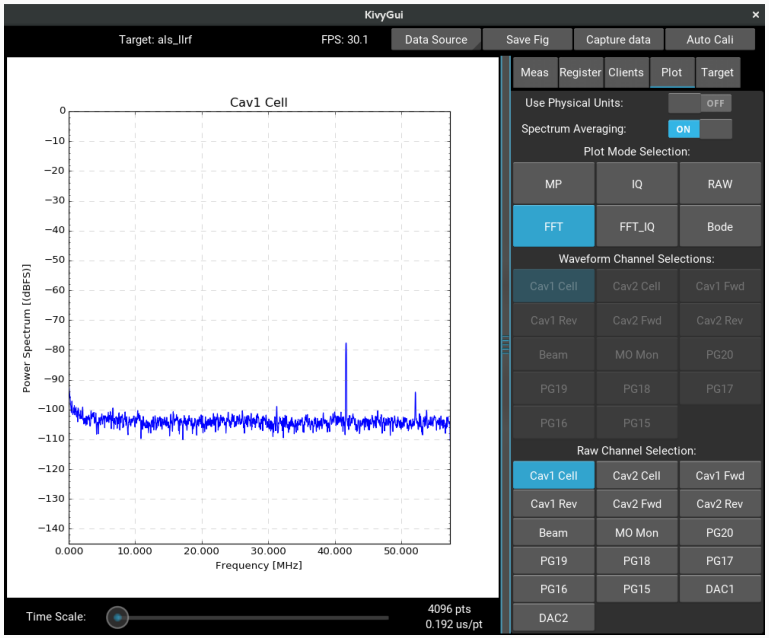


(a) Vector Oscilloscope

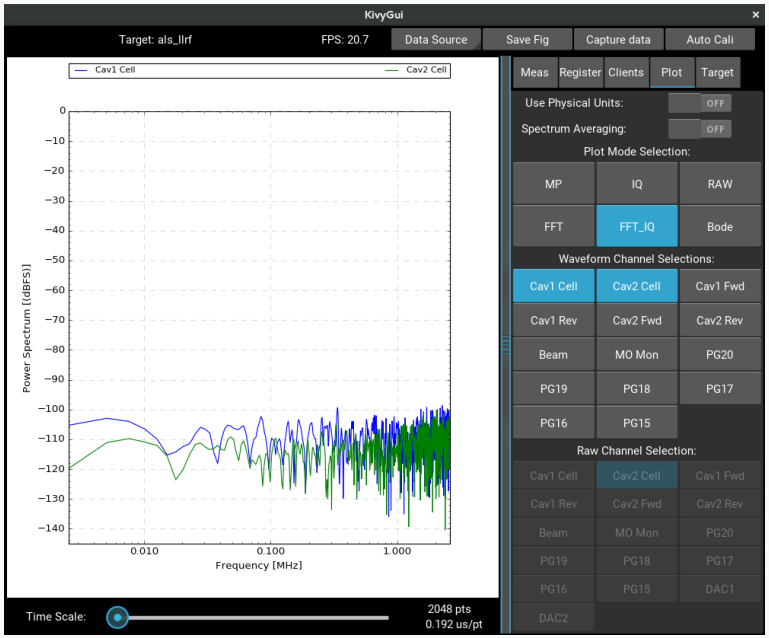


(b) Vector IQ Polar 3D plot

Engineering GUI: a python based standalone GUI

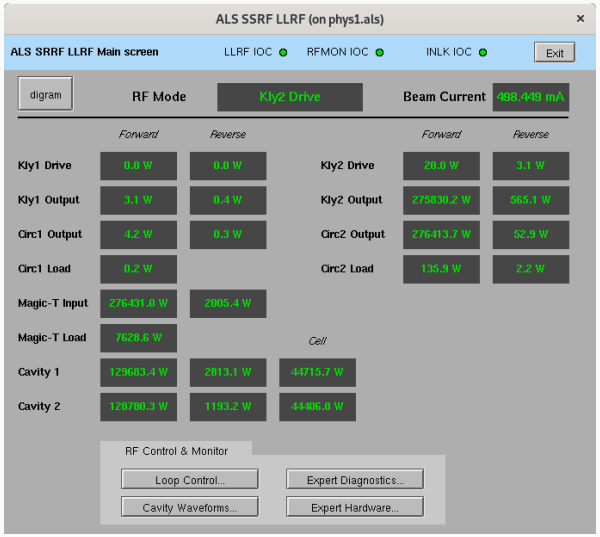


(a) IF band spectrum analyzer

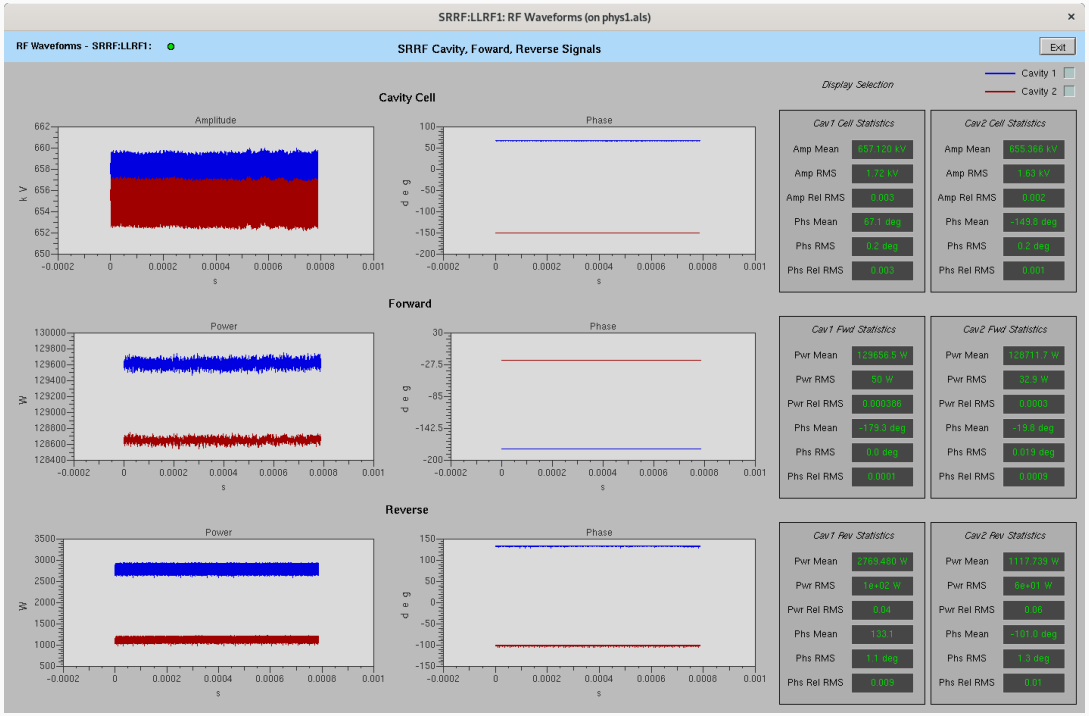


(b) Baseband FFT analyzer

EPICS IOC and Operation GUI



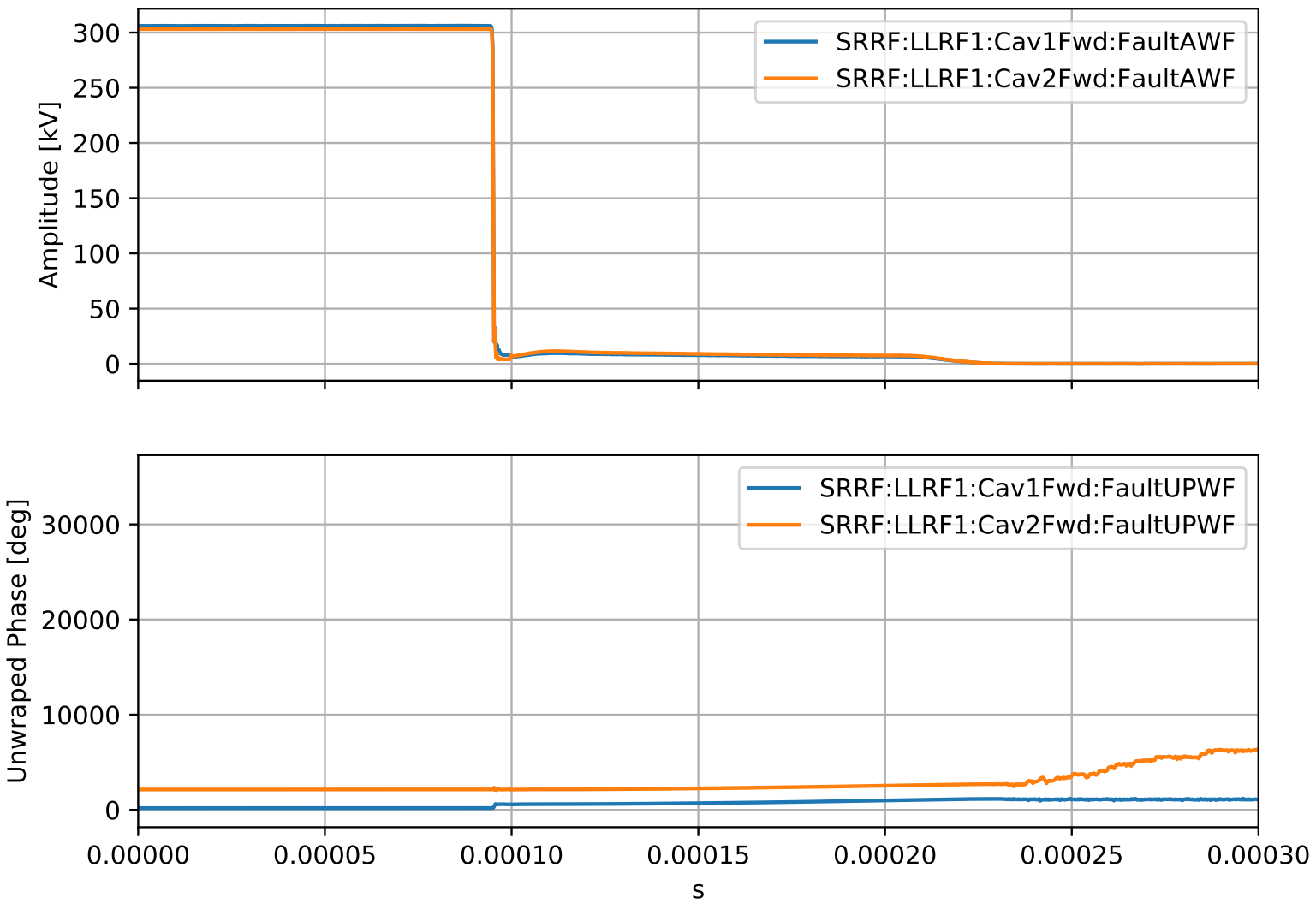
(a) SRRF Overview



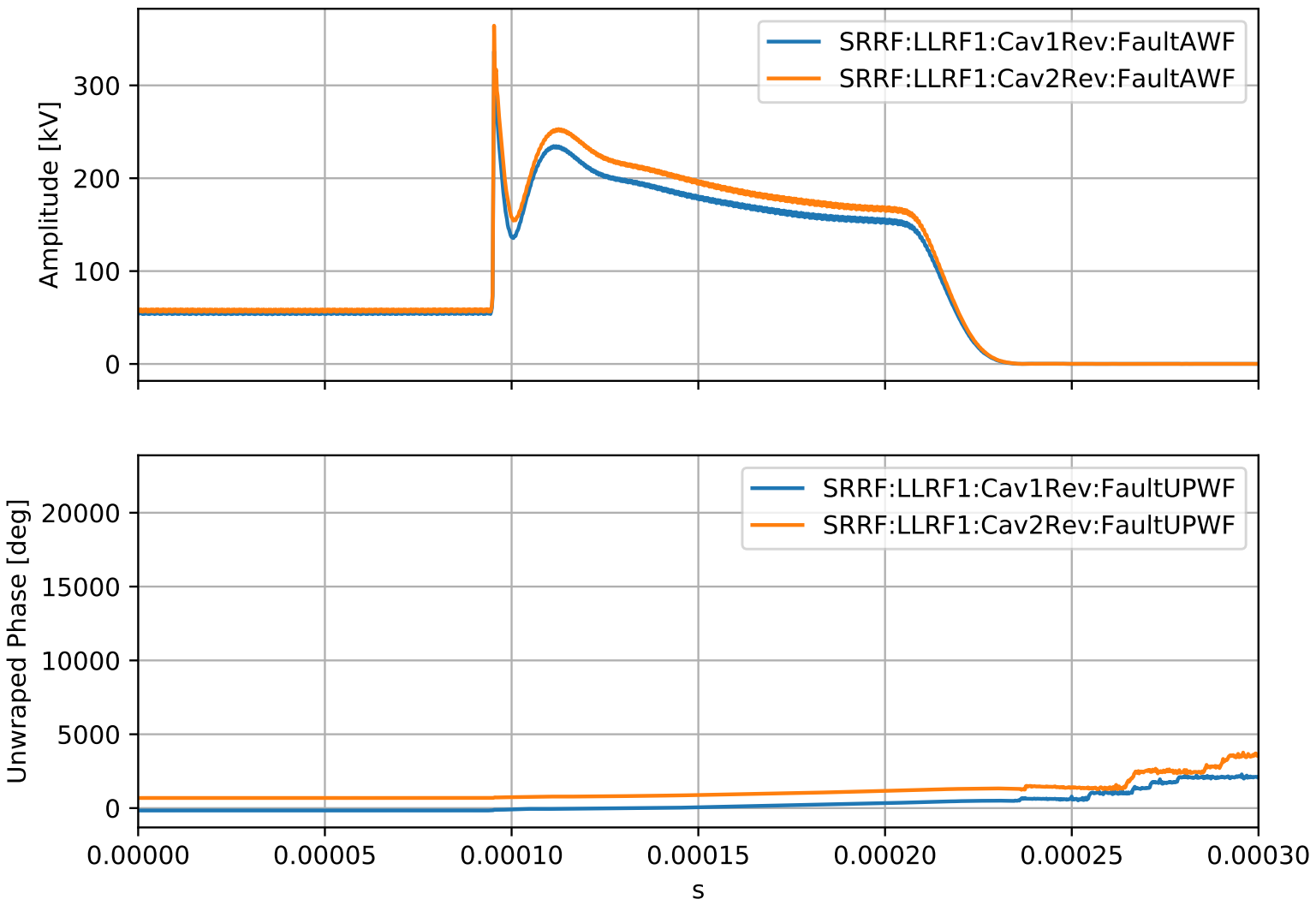
(b) Cavity Waveforms

Shared software architecture with LCLS-II LLRF control. [4]

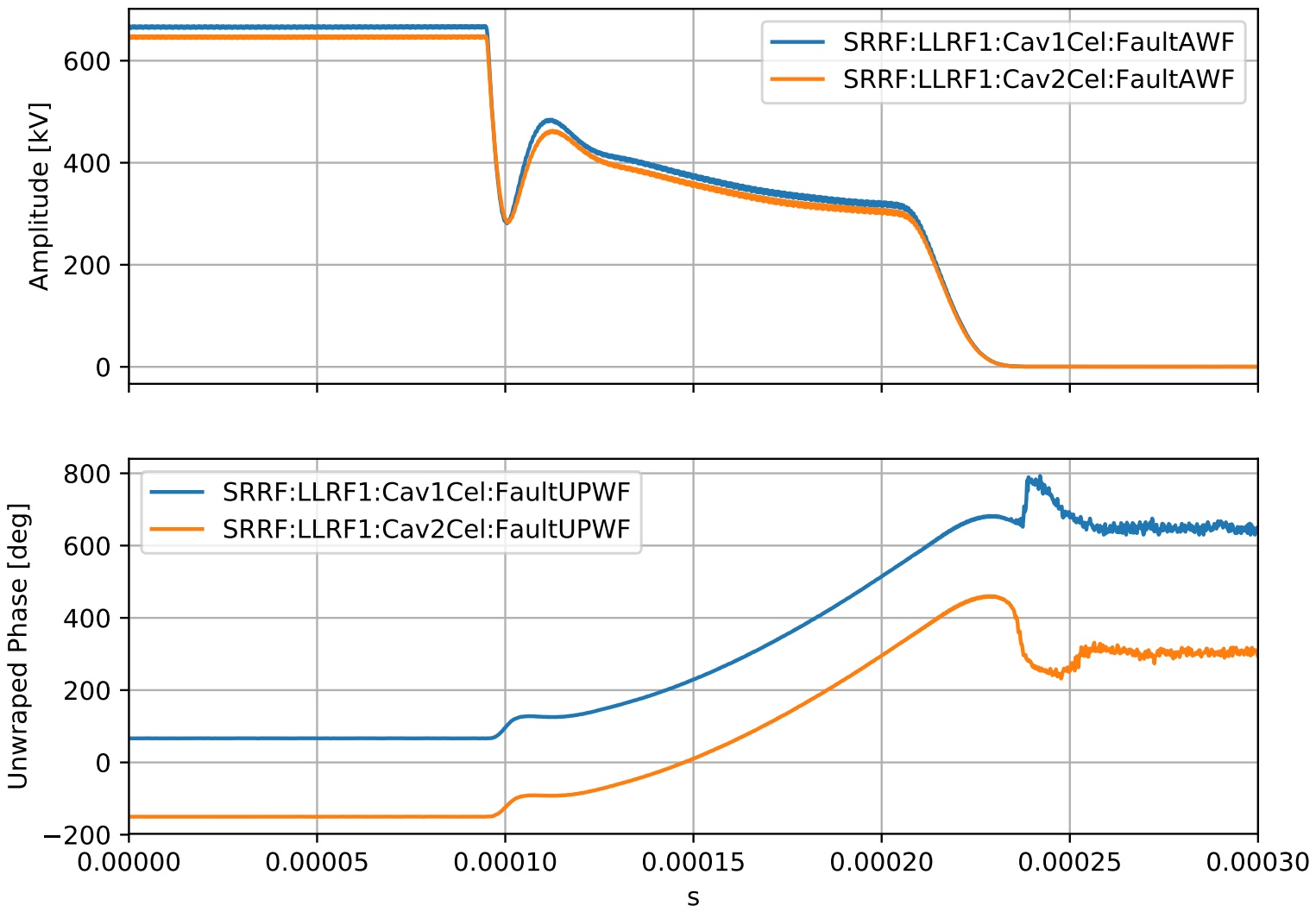
Fault Waveform Capturing: Cavity forward



Fault Waveform Capturing: Cavity reverse

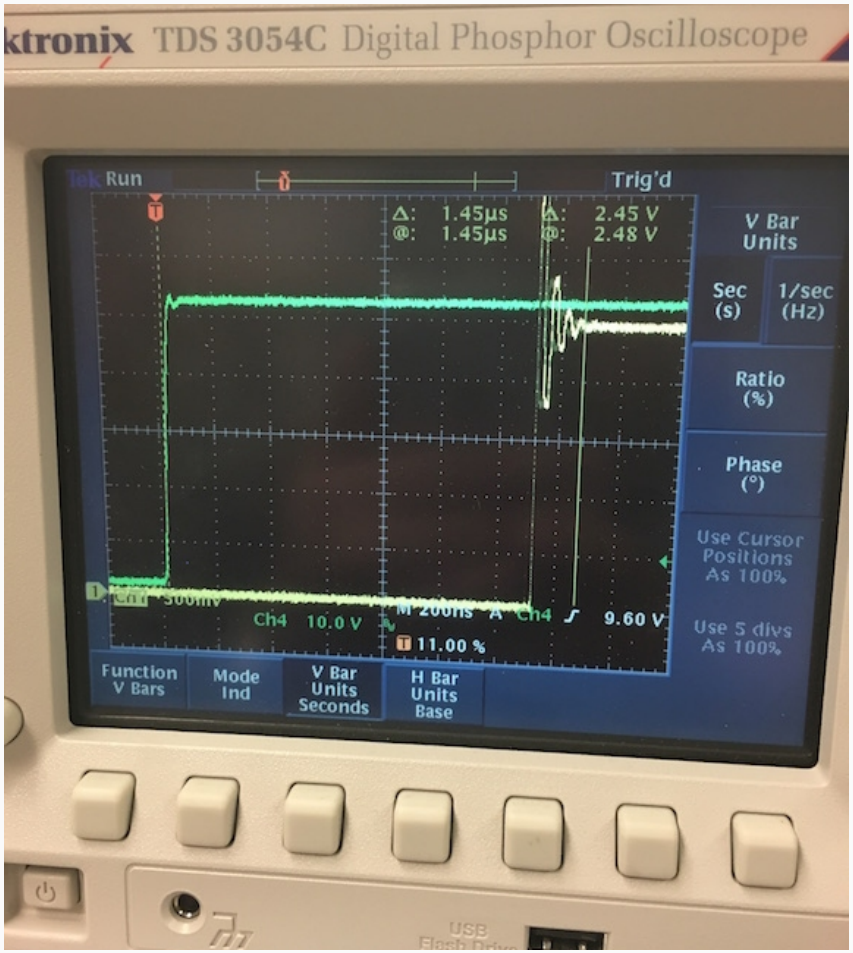


Fault Waveform Capturing: Cavity cell probes



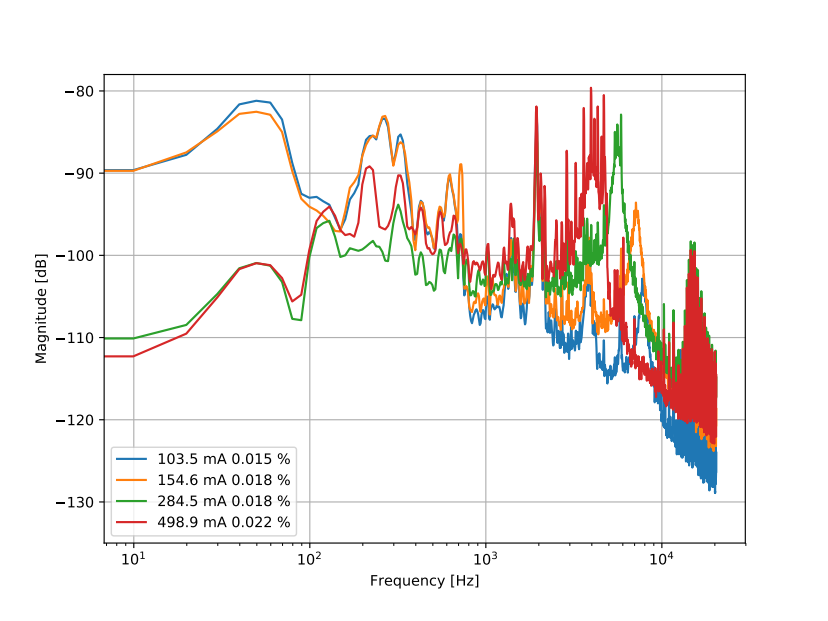
Operation and Performance

1.45μs inter-chassis interlock latency

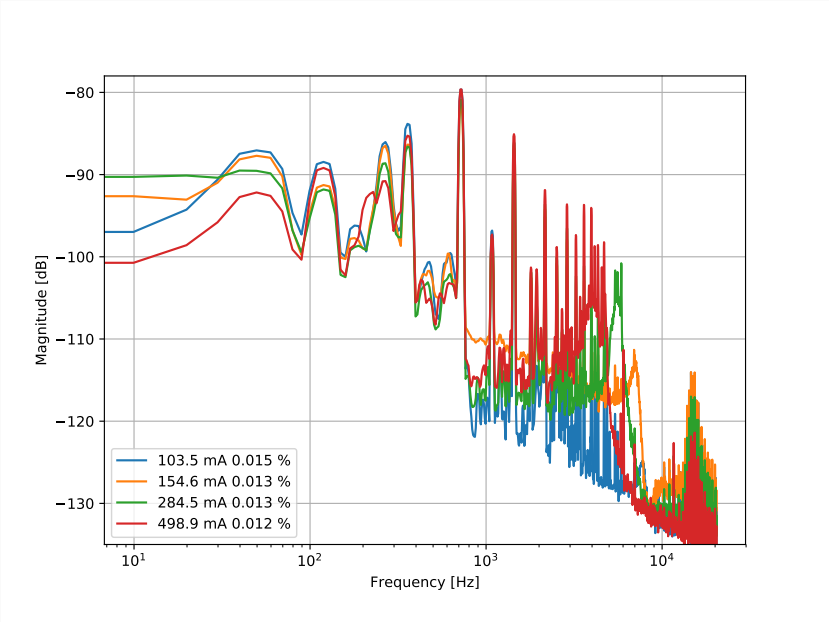


RF Power (Lab)	1.45μs
RF Power (ALS)	$< 3\mu$s
ARC det. latency	$< 2\mu$s

Amplitude and Phase Stability: with different beam load



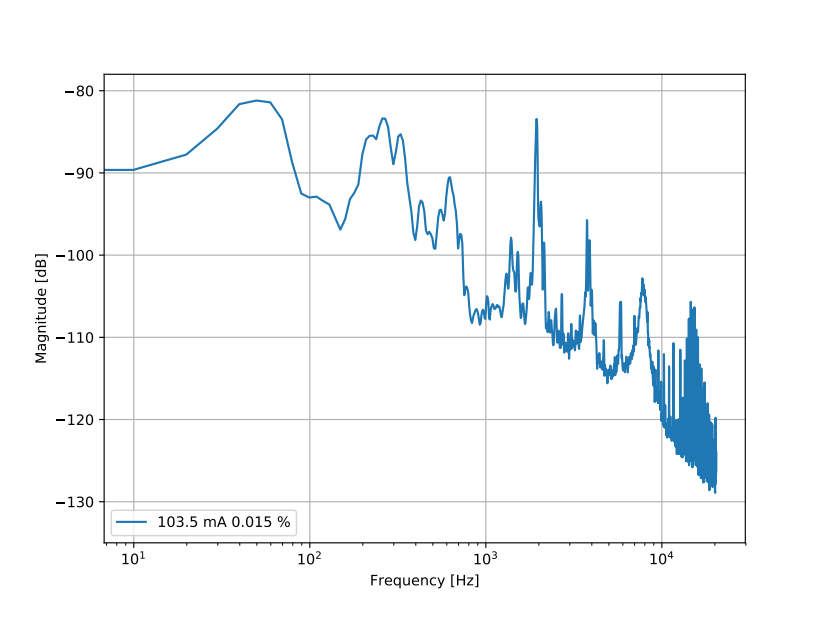
(a) Amplitude loop stability: $< 0.03\%$ RMS



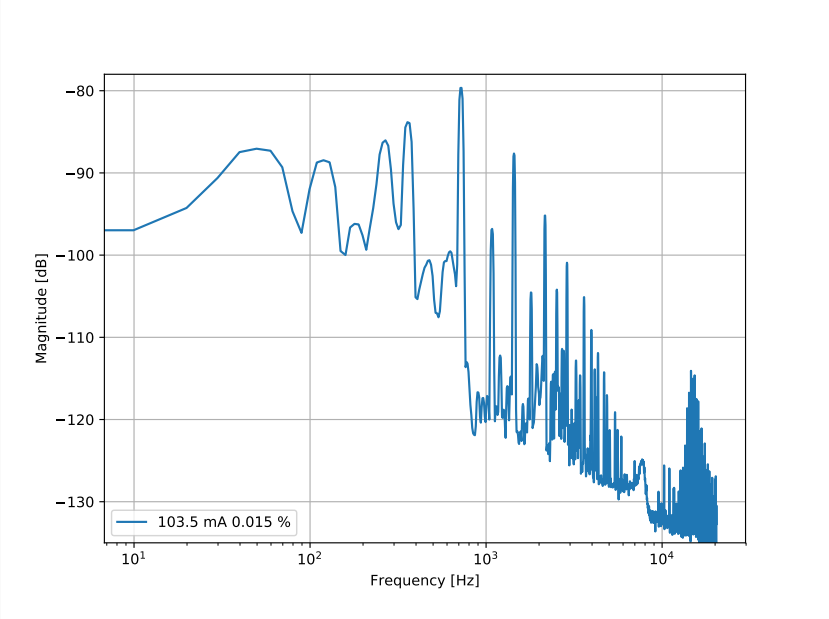
(b) Phase loop stability: $< 0.02^\circ$ RMS

Measured under klystron 2 drive mode, where average of two cavity cell voltages are regulated.
Loop parameters are at operation nominal setting, with $\sim$ 1 kHz bandwidth, integral only.
Statistics are from in–loop waveform measurements.

Amplitude and Phase Stability: at 104 mA beam current

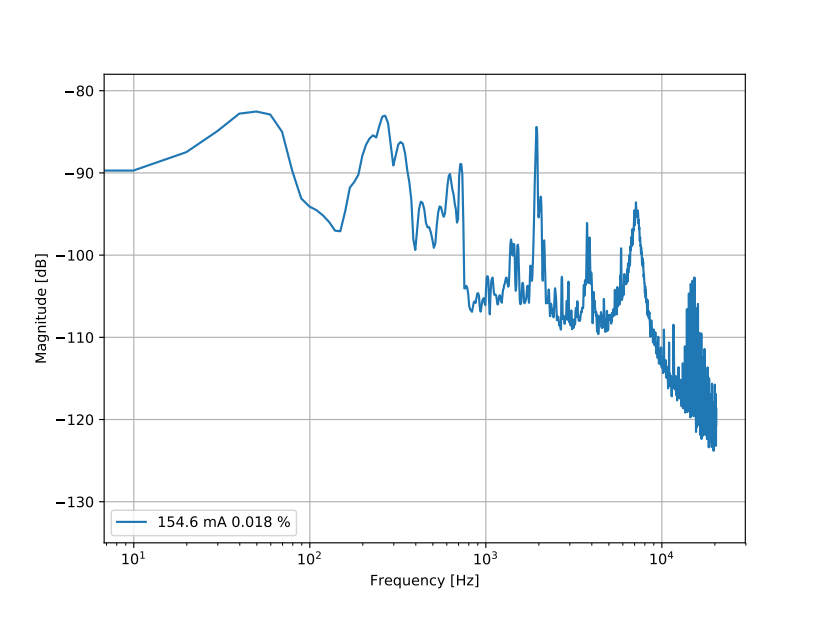


(a) Amplitude loop stability

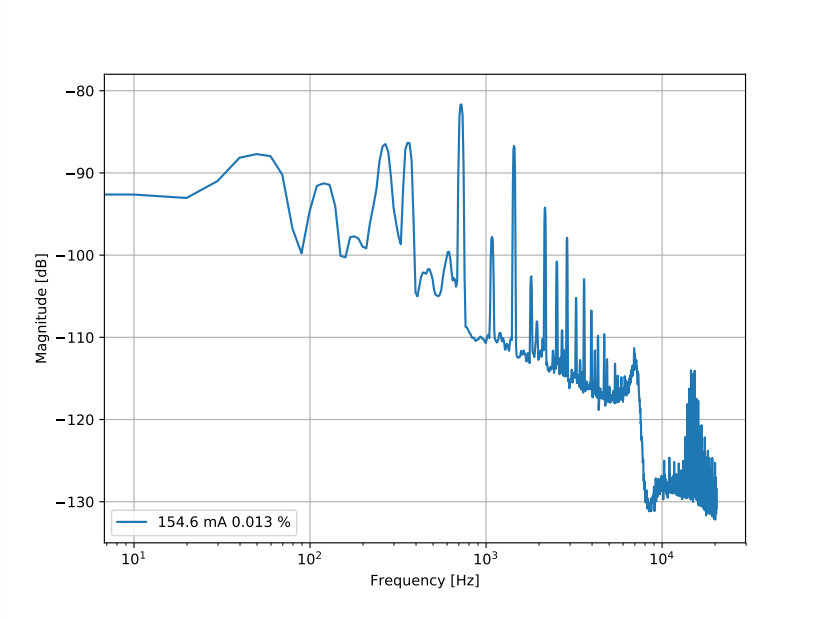


(b) Phase loop stability

Amplitude and Phase Stability: at 155 mA beam current

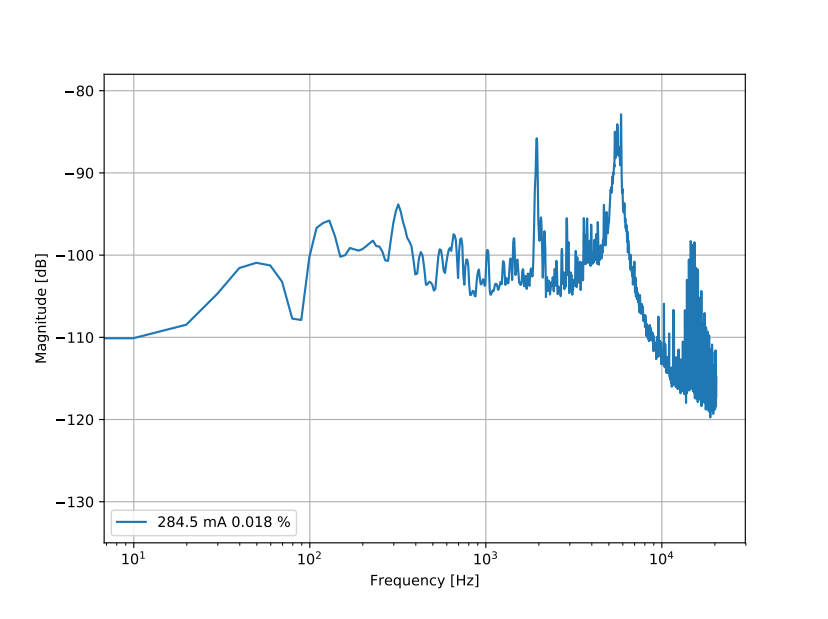


(a) Amplitude loop stability

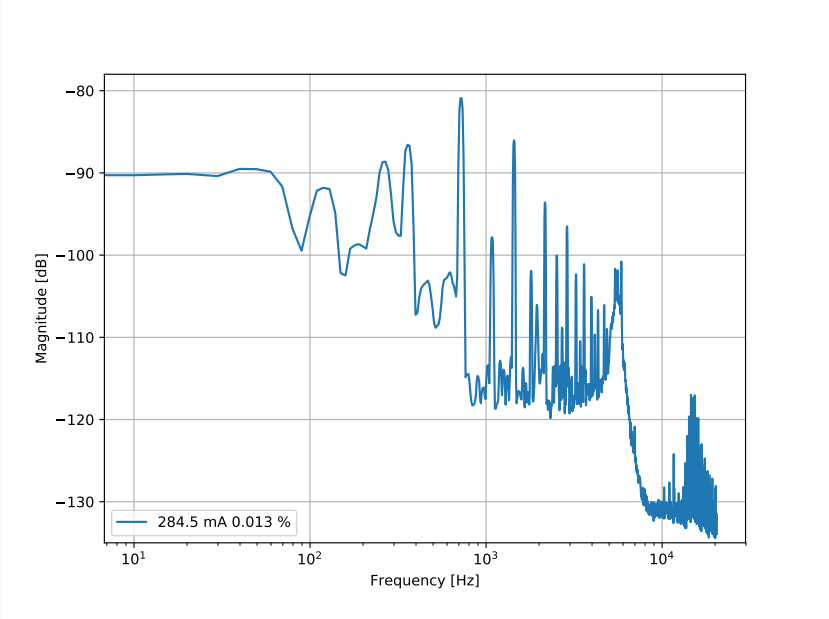


(b) Phase loop stability

Amplitude and Phase Stability: at 285 mA beam current

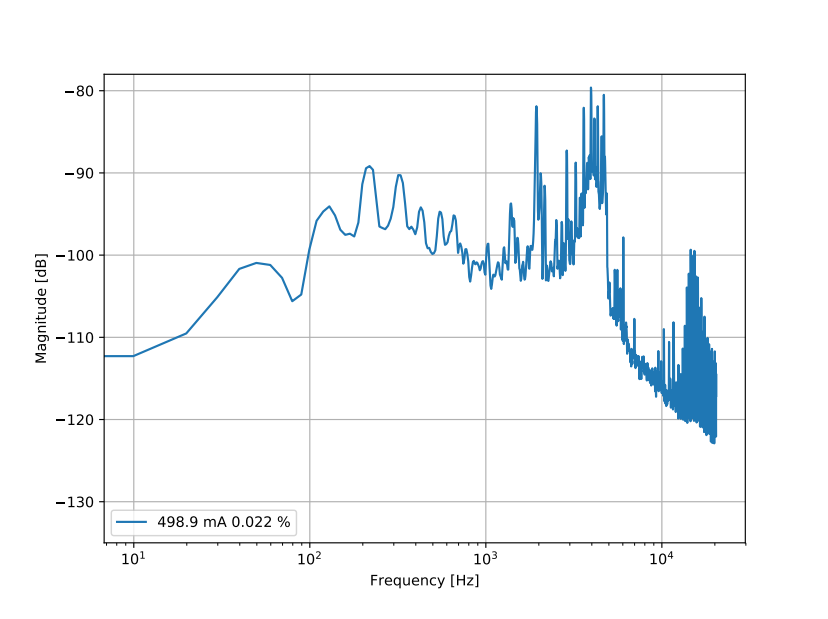


(a) Amplitude loop stability

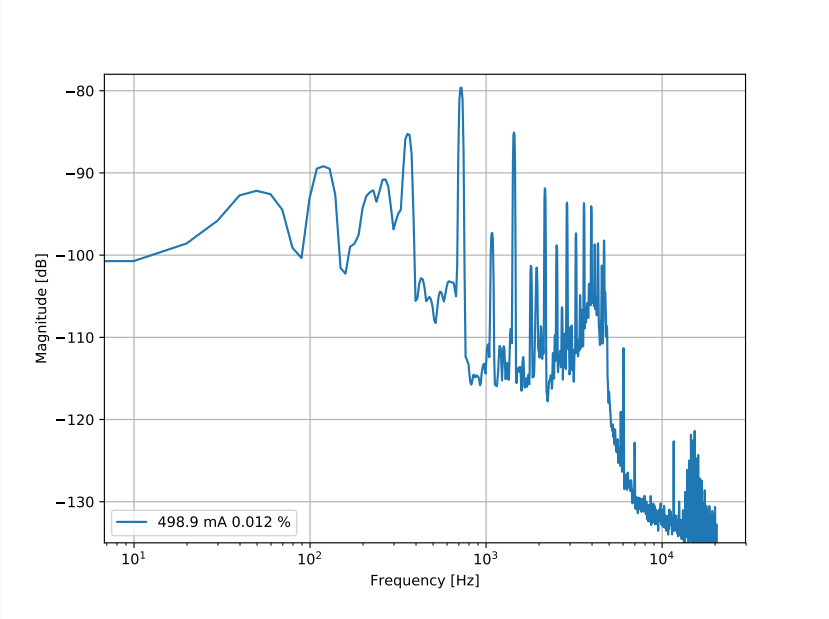


(b) Phase loop stability

Amplitude and Phase Stability: at 499 mA beam current

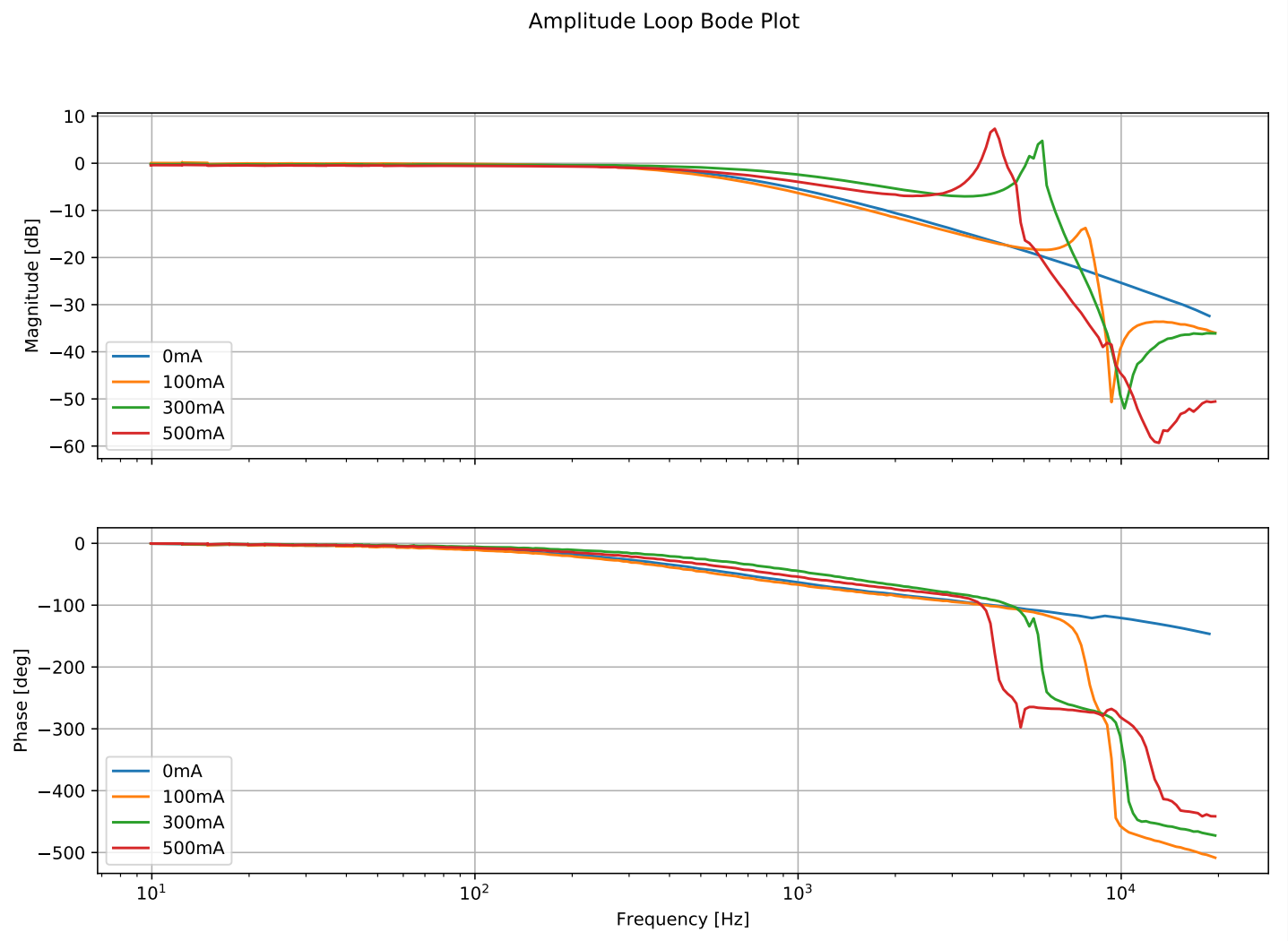


(a) Amplitude loop stability

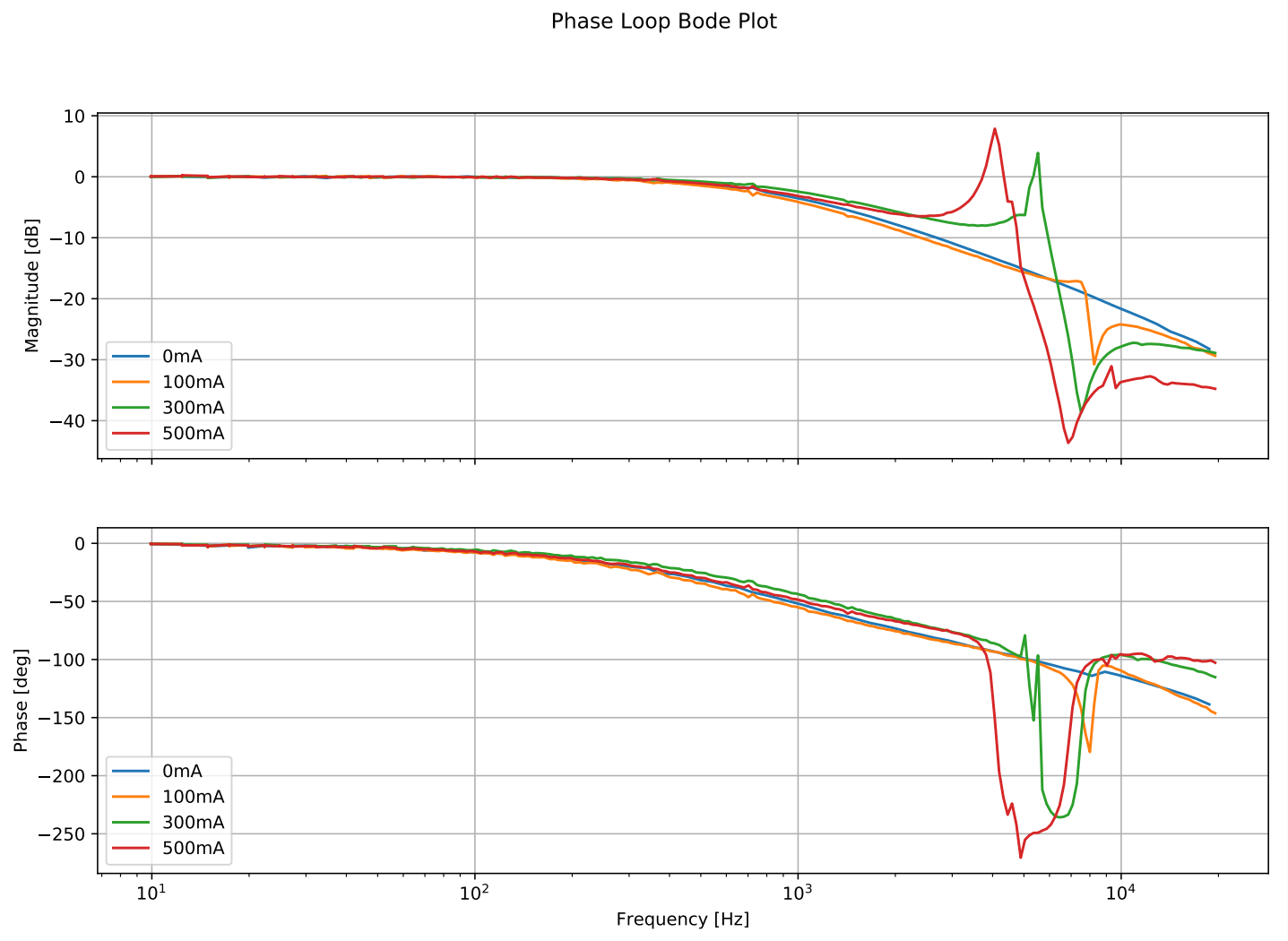


(b) Phase loop stability

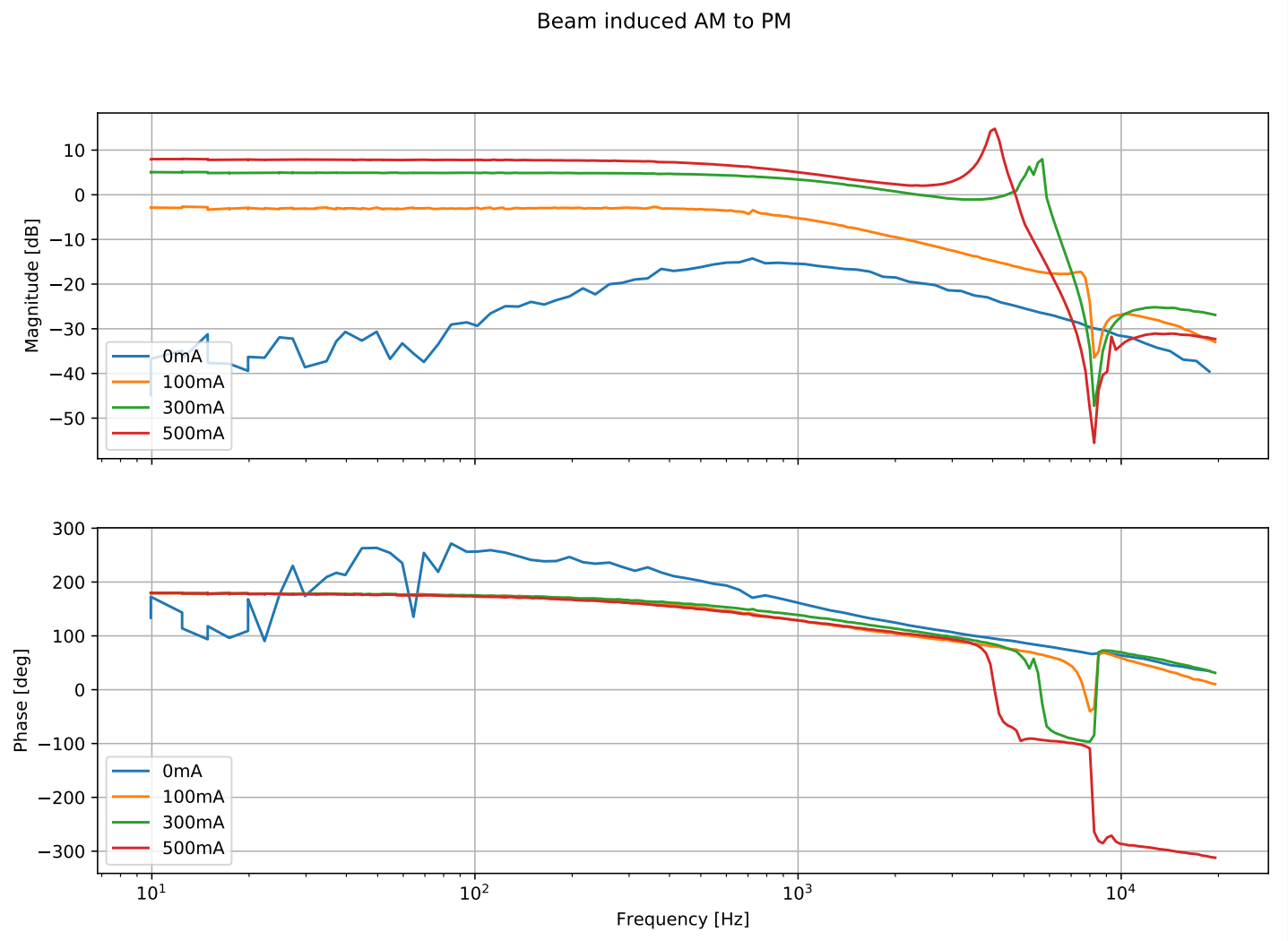
Amplitude Loop Frequency Response



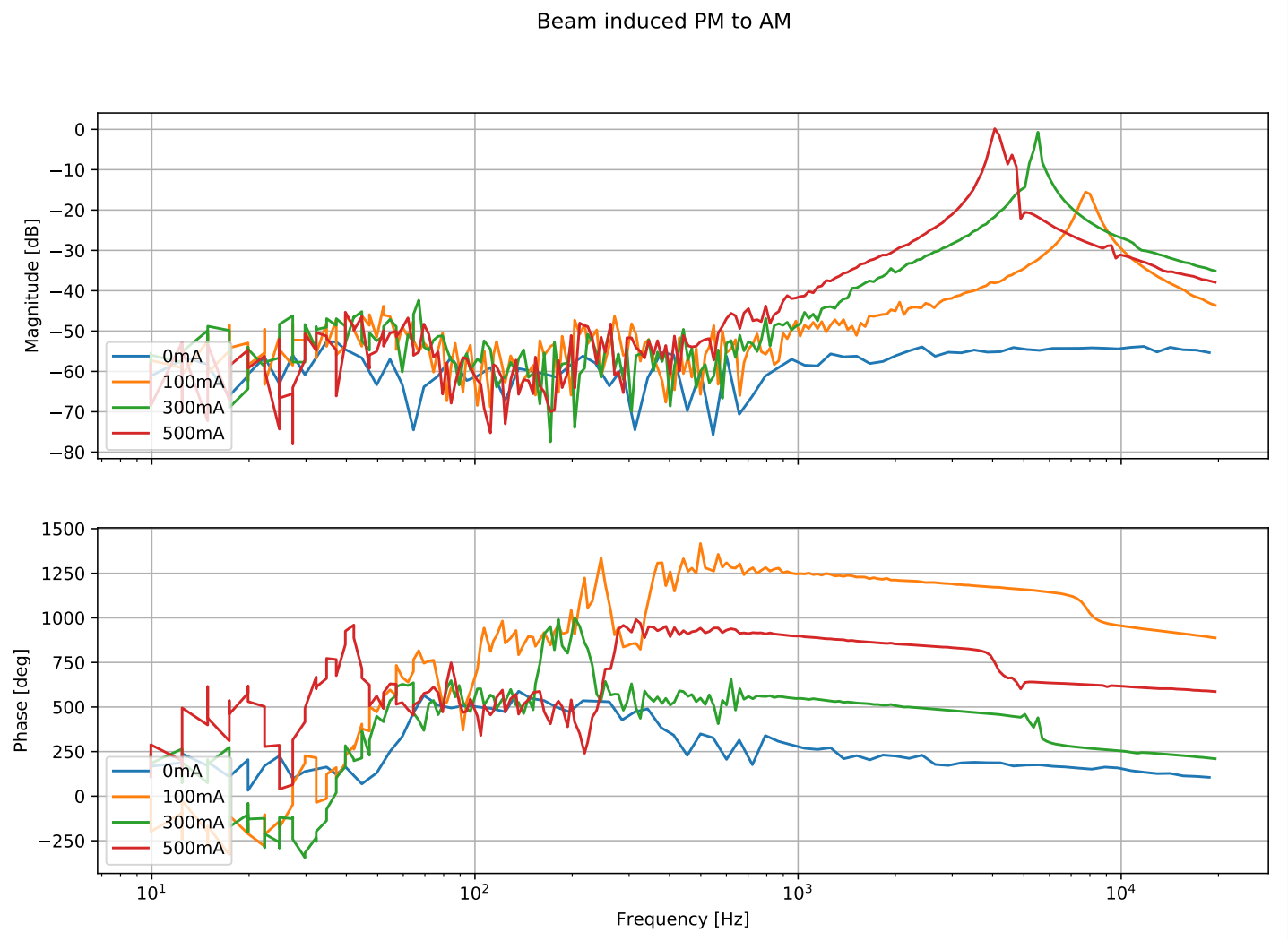
Phase Loop Frequency Response



Beam induced Amplitude to Phase modulation



Beam induced Phase to Amplitude modulation



Conclusion

Summary

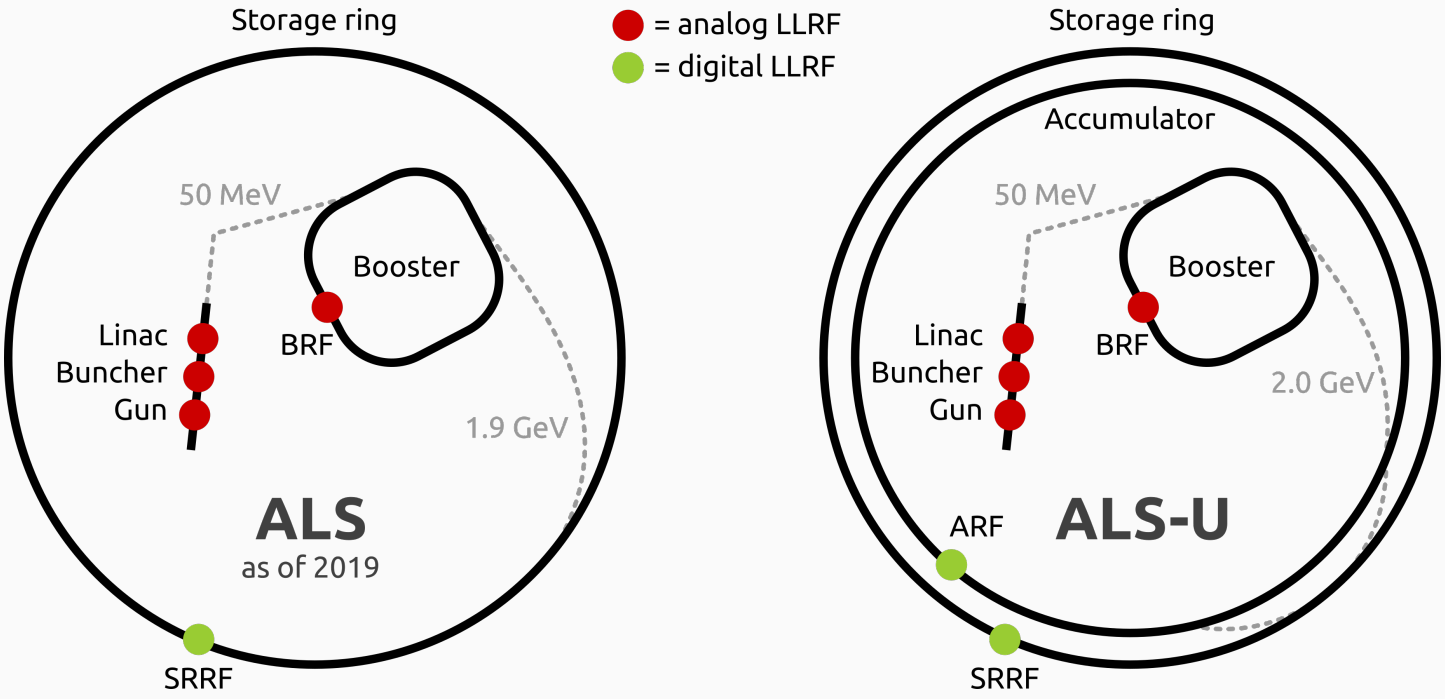
Philosophy Emphasize open source hardware, firmware, software design under BSD License;

Age Operational since March 2017;

Reliability Mean time between failure: $\approx$ 6 months;

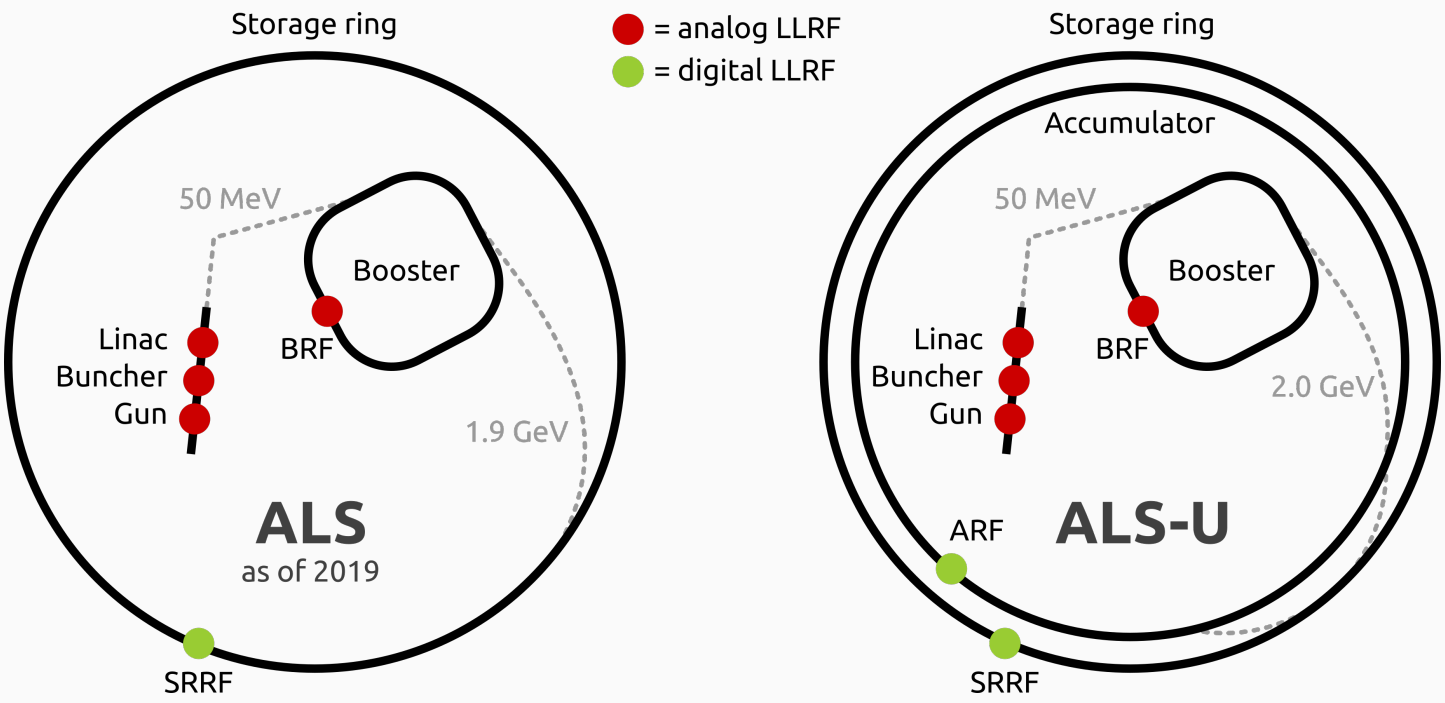
Performance
- $< 0.1\%$ RMS amplitude stability
- $< 0.1^\circ$ RMS phase stability
- $< 2\mu$s interlock latency

Look Ahead: ALS-U LLRF



New LLRF for Accumulator Ring

Look Ahead: ALS-U LLRF



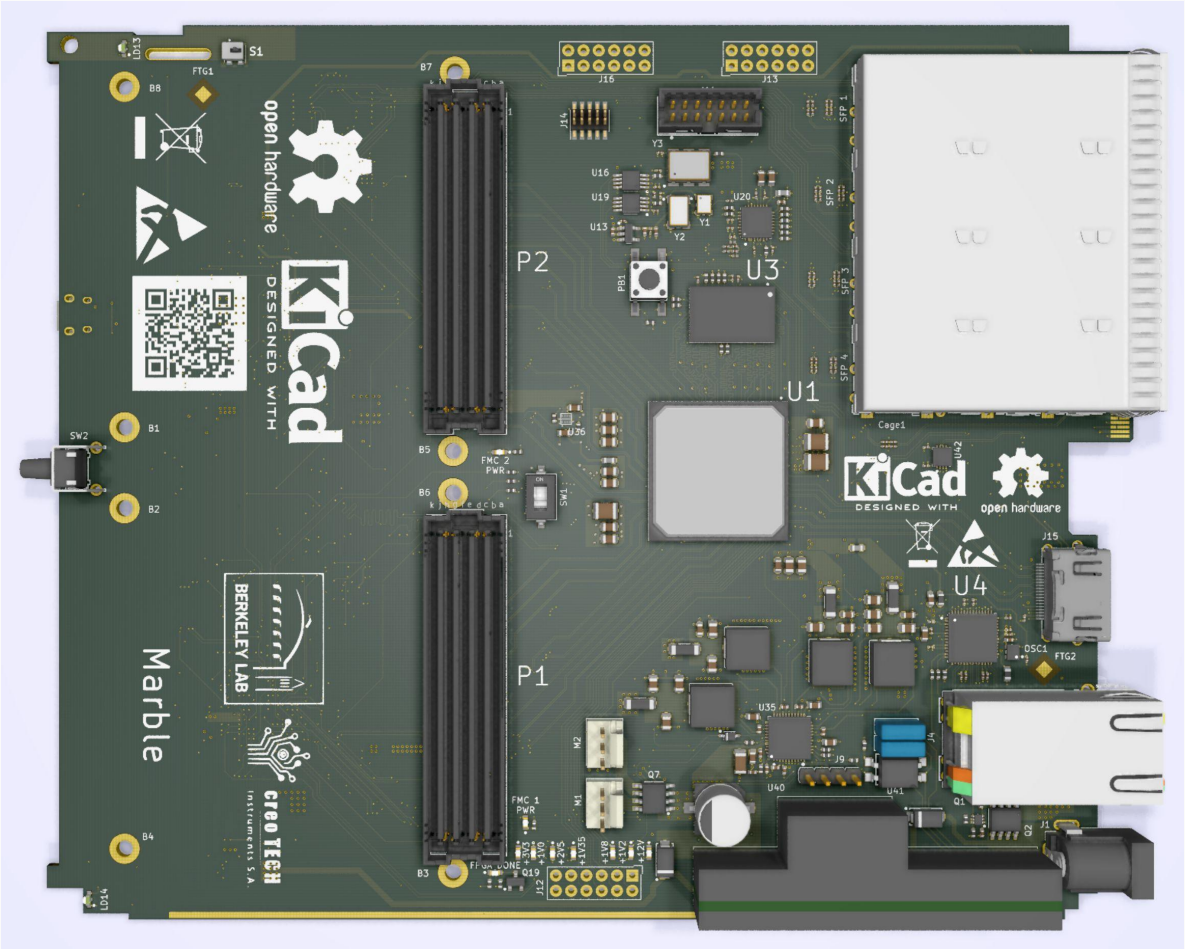
New LLRF for Accumulator Ring

Distributed LLRF system

- Agile phase-continuous RF distribution; [5]
- Bucket alignment control;

Tuesday Poster Session: *Low phase noise master oscillator generation and distribution for ALS and ALS-U*

Look Ahead: ALS-U LLRF FPGA Carrier



LBNL Dual FMC NAD/AMC Carrier [6, 7]

Wednesday talk: *Open Source LLRF stack*

Questions?

References i

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