LLRF Status & Development Activities at the Spallation Neutron Source

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2019 LLRF Workshop

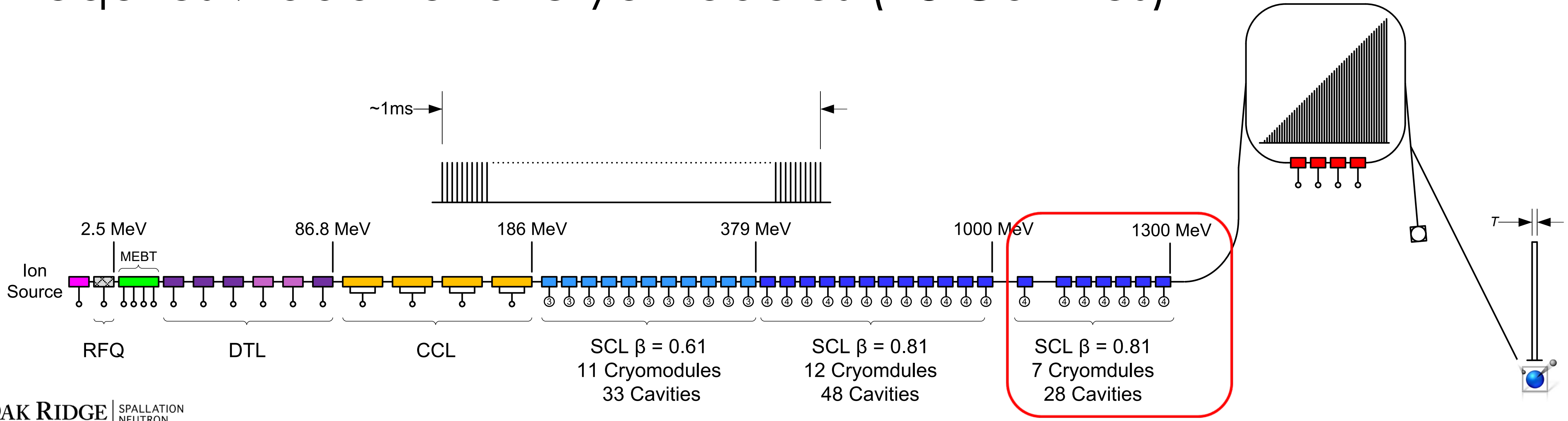
Chicago, IL

Since LLRF Workshop 2017…

- Business as usual → support accelerator operations
  - Provide neutrons for user community
- Replaced the Radio Frequency Quadrupole (RFQ)
  - Improved beam transmission
  - Developed a Field Flatness Measurement System to monitor RFQ health
- Completed the Ring LLRF upgrade
  - 4 replacement LLRF systems developed and installed
  - First μTCA.4 LLRF systems at SNS
- Proton Power Upgrade and Second Target Station become approved projects

Proton Power Upgrade (PPU) Project

- Increases power capabilities of existing 60 Hz accelerator from 1.4 MW to 2.8 MW
  - Increases power delivered to first target station (FTS) to 2 MW
  - Increases neutron flux on existing beam lines
  - Provides platform for construction of second target station (STS)
- Requires 7 additional cryomodules (28 Cavities)

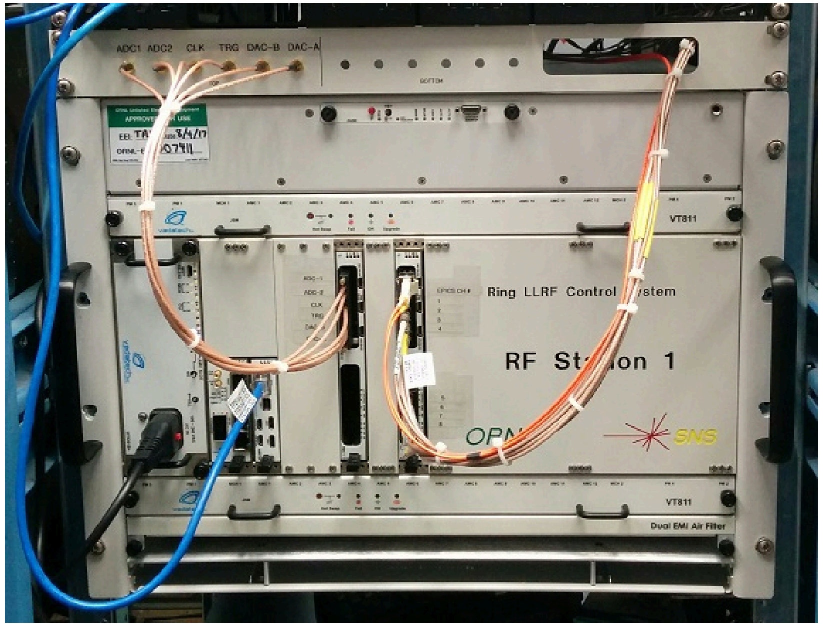


LLRF Design Considerations

- The existing LLRF systems are capable of meeting PPU requirements
  - Parts obsolescence does not allow for fabrication of additional systems
- For Second Target Station, the system cannot meet requirements
  - No support for more than one style of beam
  - No pulse-to-pulse AFF correction
  - Current system is bus bandwidth limited to 20 Hz
- Collaborative approach chosen for new design
  - LBNL LLRF Team
  - ORNL SNS Controls Group

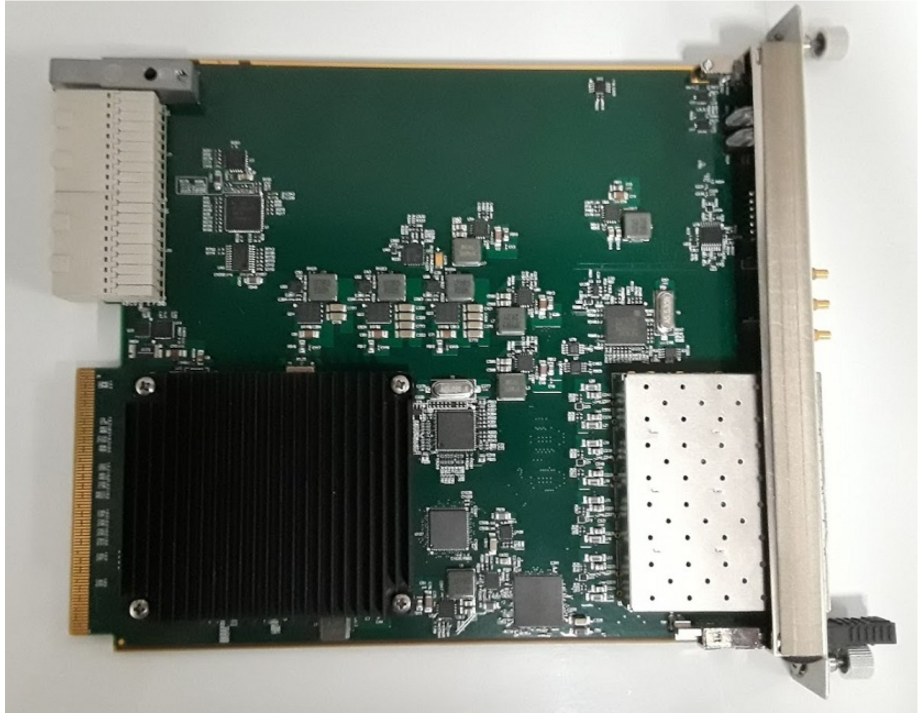
LLRF Platform Evaluation

- Investigated possible platforms
  - µTCA.4
  - VPX
  - Network attached device
  - VME/VXI
- µTCA.4 is our planned baseline
  - Controls Group is utilizing for their high-speed platform for replacement systems (MPS, timing FMC on carrier card, etc.)
  - Driver/software support for integration into EPICS completed
  - The replacement Ring LLRF was developed with this platform
    - All 4 Ring LLRF stations have been upgraded
    - Supporting 1.4 MW beam for over 1 year
  - Reasonable COTS support – multiple vendors
  - Utilized at several European labs for LLRF applications



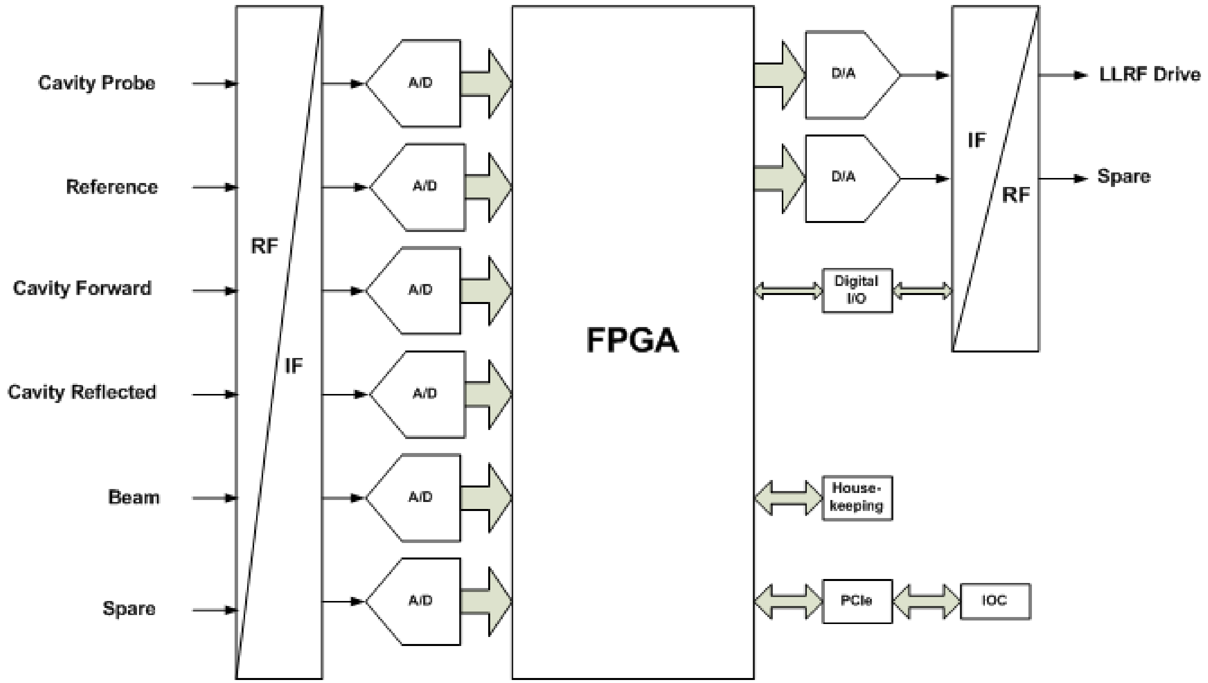
Make vs. Buy Decisions

- Use common carrier card to minimize hardware design
  - VadaTech AMC523
    - Kintex 7 410T (XC7K410T) FPGA
      - LUTS: ~400,000
      - MULTs: 1540
      - BRAM: 28 Mb
      - IO Count: 500
    - Maxim MAX5878 dual 16-bit, 250 MSPS DAC
    - Silicon Labs Si5345 DSPLL jitter attenuator, cleaner
      - Additive jitter ~330 fs measured
- Fabricate custom rear transition modules



Field Control

- Digital control system that fundamentally realizes a proportional-integral (PI) feedback controller along with adaptive feed-forward (AFF) to support cavity filling and beam loading
- Based on the existing SNS physics specifications
  - 1% amplitude, 1 degree phase
- IF frequency will remain at 50 MHz due to installed reference system
- Sampling scheme changed to Non-I/Q (12/5*IF)



Improvements Over Existing FCM

- Higher bandwidth data acquisition
  - Report data for all RF pulses at 60 Hz versus 20 Hz
  - Improved learning speed for Adaptive Feedforward
  - Better diagnostics for troubleshooting
- Greater FPGA resources
  - Creates possibility to expand upon current FCM algorithms.
- Higher resolution ADC (16 bits versus 14 bits)
- Higher sample rate (120 MSPS versus 40 MSPS)
  - Lower latency for multiplication and addition
  - Improved measurement precision by avoiding spectral aliasing

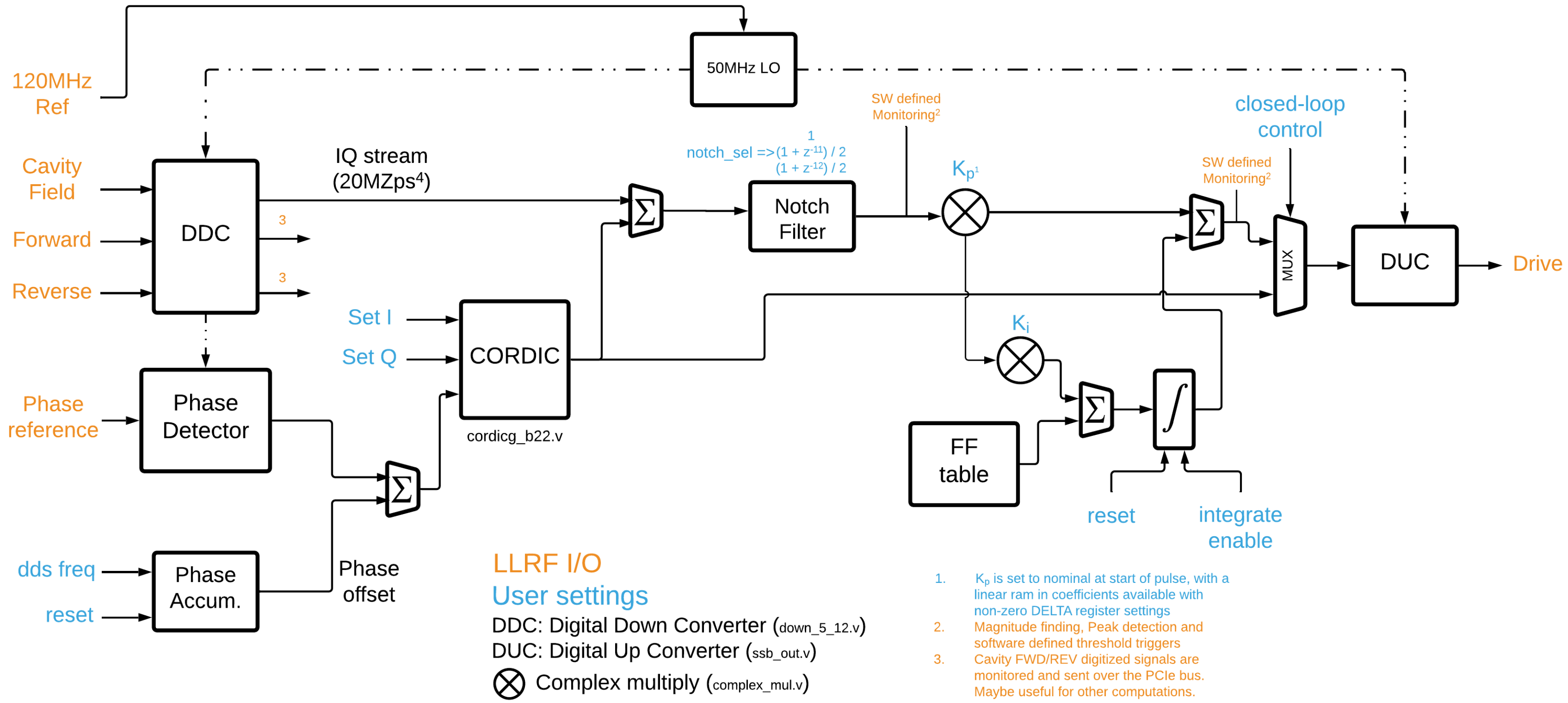
Field Control Module Hardware

- Collaboration with VadaTech
  - 8 ADC channels – AD9653
    - Six 50 MHz AC coupled input channels
    - Two baseband DC coupled channels
  - DAC buffer to support 50 MHz IF output
  - Digital IO for communications with HPM-II and Frequency Conversion Chassis

SNS PPU Field Control Module – Sorrell
(Poster session)

Firmware

- Field control firmware is based on the original SNS code
  - Core DSP is well tested
- New design requires digital up and down conversion
- Provide hooks for on-chip AFF
- First bench tests planned for late October 2019



High Power Protection & Interlocks

- The high-power protection systems are responsible for the fast shutdown of the output signal
  - Detected overpower
  - Quench detection
  - Arcs in the RF distribution system and cavity
  - Poor vacuum
  - "Soft" interlocks – cryo, coupler cooling, and HPRF permits
- Retain the AFT Arc-4 arc detector system
  - Interface with protection module for EPICS interface
- Four history buffers for improved troubleshooting
  - 400 ns resolution

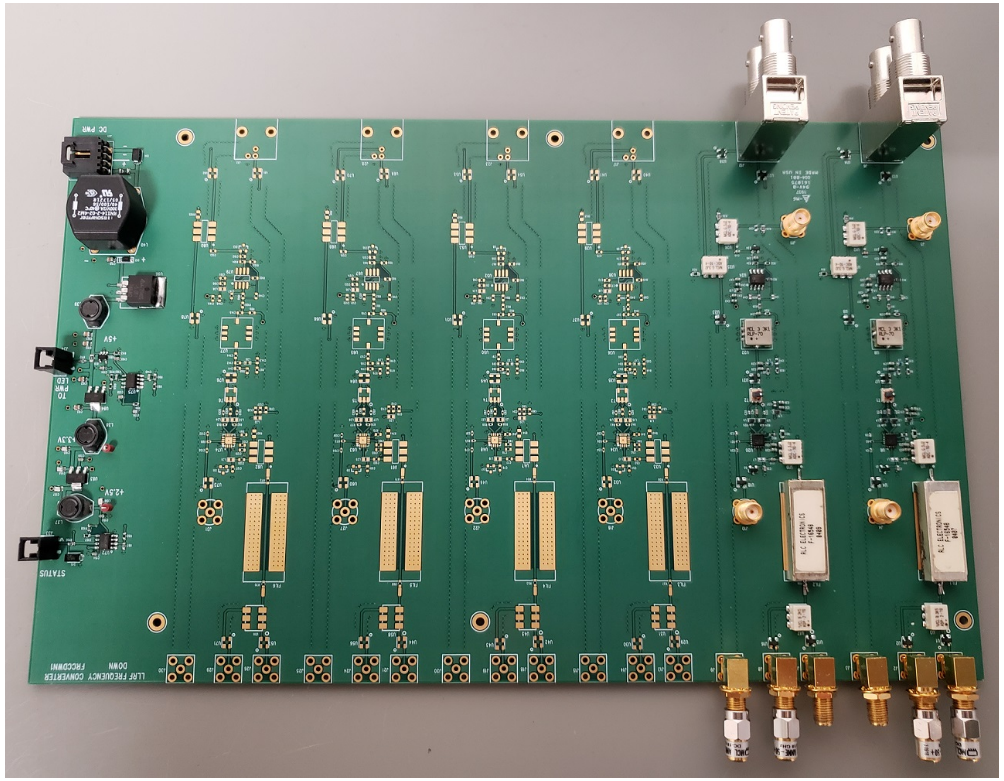
High-power Protection Module (HPM-II)

- RF front-end utilizes eight ADL5513 log detectors
  - 80 dB dynamic range
  - ADCs are 16-bit vs. 10-bit in original system
  - I2C programmable DAC & pot for automated calibration
- Eight arc detector interfaces
  - Provides test pulse for fiber verification
- Digital IO
- Initial firmware and EPICS screens are in test

SNS PPU High-Power Protection Module - Sorrell (Poster session)

Frequency Conversion Chassis

- All RF functions are contained in a temperature-controlled chassis
- Six active down conversion channels
  - LTC5567 active mixers
- Single active up conversion channel
- 50 MHz clock reference created for digital electronics
- Monitors provided for reporting health of the chassis



SNS Frequency Conversion Chassis Upgrade for PPU - Musrock (Poster session)

Summary

- Proton Power Upgrade project has necessitated the redesign of the Linac LLRF systems
  - Great collaborative effort
- Use of COTS hardware has shortened development time
- Custom rear transition modules for field control and protection functions are complete and tested
- Firmware development has leveraged the original SNS code and will be ready for bench testing in October 2019
- Design of the Frequency Conversion Chassis is underway and initial testing started

Acknowledgement

- Thanks to the SNS LLRF Team, Controls Group, and LBNL LLRF Team for their dedication and hard work. None of this would be possible without the help of everyone involved.

SNS LLRF Team
- Jeff Ball
- Taylor Davidson
- Mark Musrock
- Chip Piller
- Zach Sorrell
- Stacey Whaley

SNS Controls Group
- Eric Breeding
- Doug Curry
- Craig Deibele
- Marnelli Martinez
- Chuck Roberts
- John Sinclair

LBNL LLRF Team
- Larry Doolittle
- Carlos Serrano
- Vamsi Vytla

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