LLRF life cycle @ LBNL

Gang Huang on behalf of the team

LLRF 2019, Chicago

Life cycle

Seeds — Open source environment, hardware, firmware and software (BIDS)

Germination — R&D on hardware development, firmware modules, control algorithm

Growth — In lab project, ALS, ALS-U, HiRES
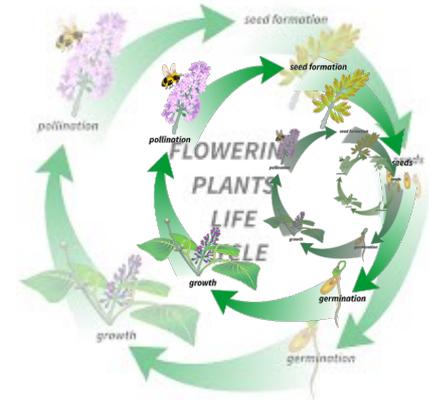
Collaboration projects, LCLS-II, SNS, PIP-II, Tsinghua

Pollination — Cross disciplinary: Laser stacking, Quantum bit control

Seed formation — Contribute to or forking open source projects
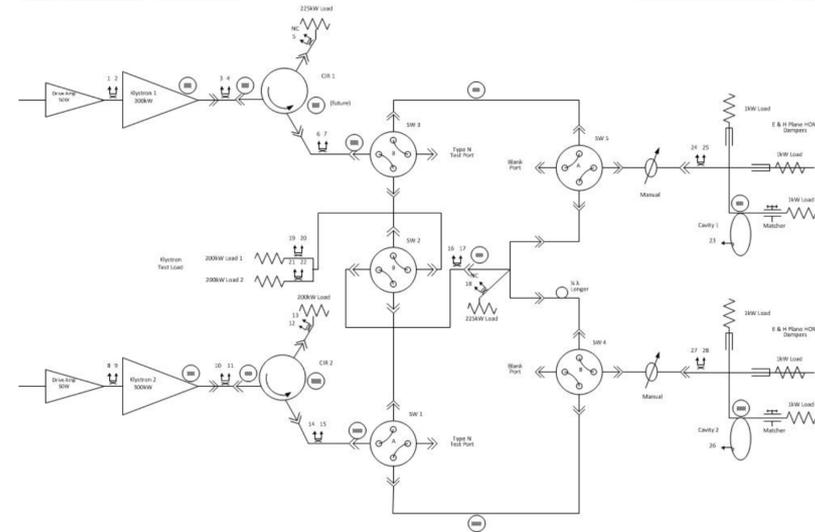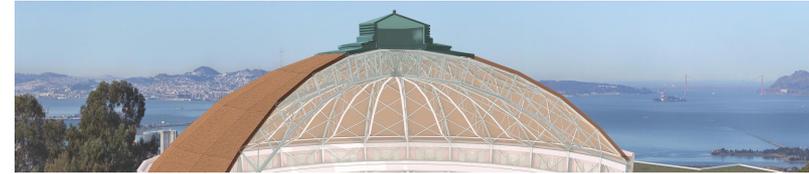
Advanced Light Source Digital LLRF

- ALS is the 3rd generation light source at LBNL which was in operation since 1993
- Few years ago, the decision was made to upgrade the LLRF system from analog to digital to improve flexibility and reliability
- Support configurable waveguide mode to drive two cavities
- Operational since March 2017
- Emphasis open source hardware, firmware and software design under BSD license

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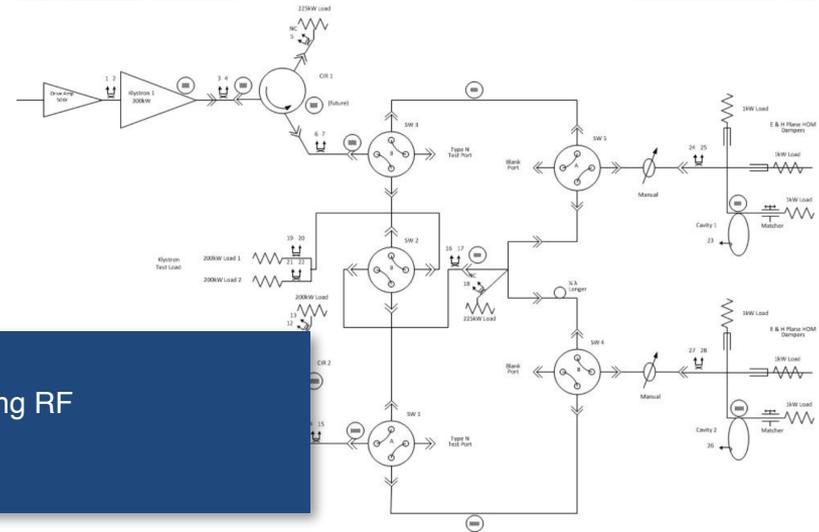
Tuesday 9:10-9:40
Digital LLRF system for Advanced Light Source Storage Ring RF
Qiang Du
LBNL

- Upgrade ALS to a diffraction limited storage ring based on the multibend achromat lattice
- Additional accumulator ring swapping beam
- LLRF
  - Current ALS LLRF system design is capable to meet the requirements
- Master Oscillator upgrade
  - Low phase noise
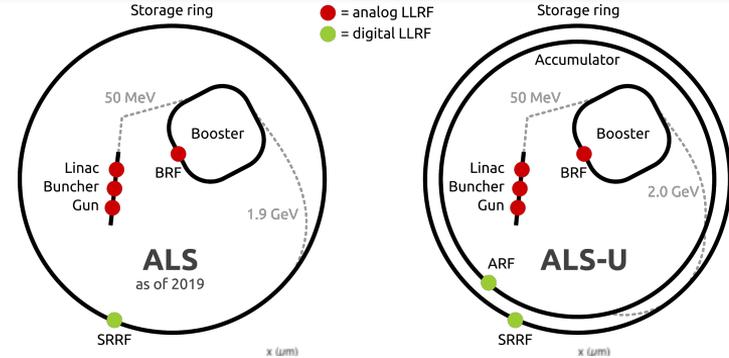 - Frequency fine adjustable
  - Continuous phase
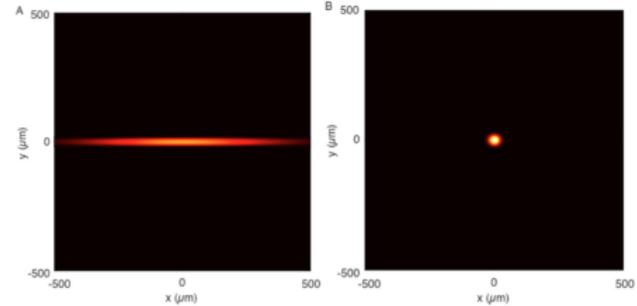
From ALS to ALS-U

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- LLRF
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  - Continuous phase

RF System Requirements

	ALS SR – 1.9 GeV	ALS-U AR – 2.0 GeV	ALS-U SR – 2.0 GeV
Cavity RF Frequency	499.645 MHz	500.405 MHz	500.405 MHz
# of Cavities	2	2	2
R_s (ea)	4.9 MΩ	4.9 MΩ	4.9 MΩ
Cav Voltage (kV)	649	649	300
β (max = 3.15)	2.93	1.13	10.07
Energy loss per turn (keV)	326.5	247	329
BM Beam Pwr (kW)	112.6	12.35	125
ID Beam Pwr (min gap) (kW)	44	0	35
3HC Beam Pwr (kW)	6.6	0	4.4
Parasitic Beam Pwr (kW)	2.5	0.25	2.5
Total Beam Pwr (kW)	165.7	12.54	166.9
Cavity Pwr (no beam) (kW)	43	43	9.2
Cavity Pwr (beam) (kW)	125.8	49.3	127.6
Waveguide Losses (kW)	3.5	1.4	2.6
High Power Amplifier (kW)	255.2	100	257.8

From ALS to ALS-U

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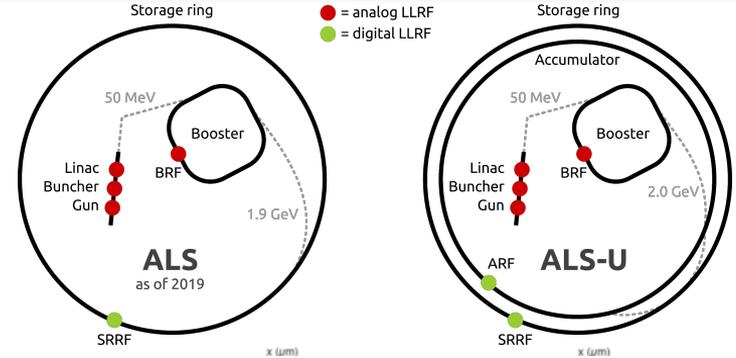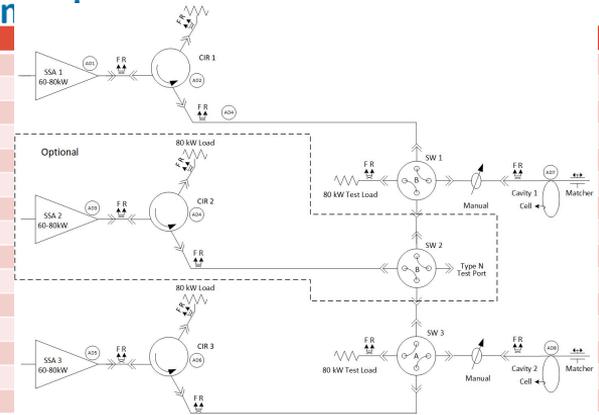 - Continuous phase

RF System Requirements

Cavity RF Frequency
# of Cavities
R_s (ea)
Cav Voltage (kV)
β (max = 3.15)
Energy loss per turn (keV)
BM Beam Pwr (kW)
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Waveguide Losses (kW)
High Power Amplifier (kW)

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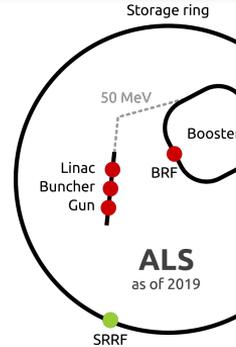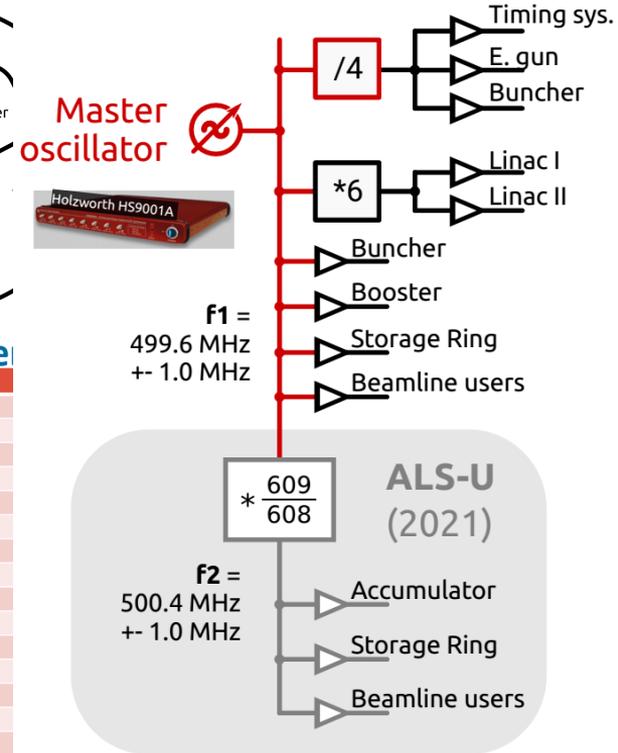 - Frequency fine adjustable
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RF System Requirements

Cavity RF Frequency	
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Cav Voltage (kV)	
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3HC Beam Pwr (kW)	
Parasitic Beam Pwr (kW)	
Total Beam Pwr (kW)	
Cavity Pwr (no beam) (kW)	
Cavity Pwr (beam) (kW)	
Waveguide Losses (kW)	
High Power Amplifier (kW) 500 mA	

From ALS to ALS-U

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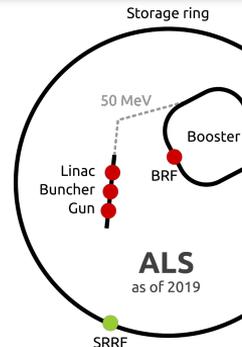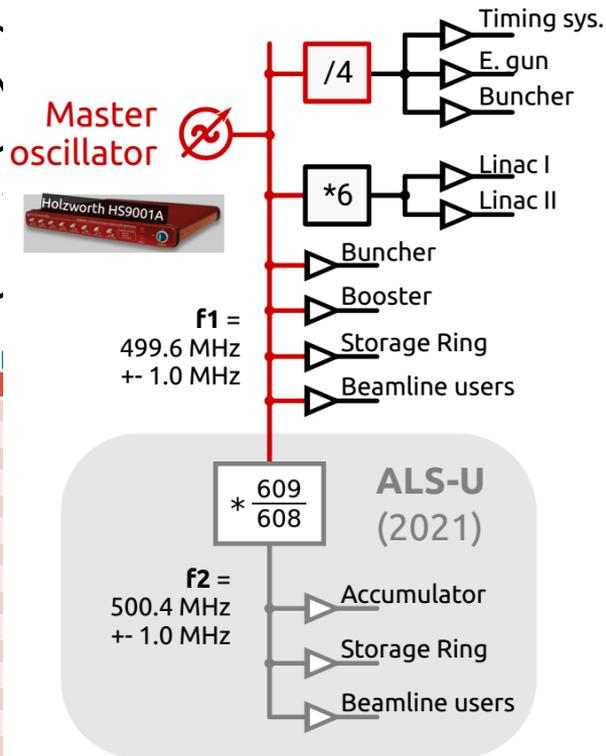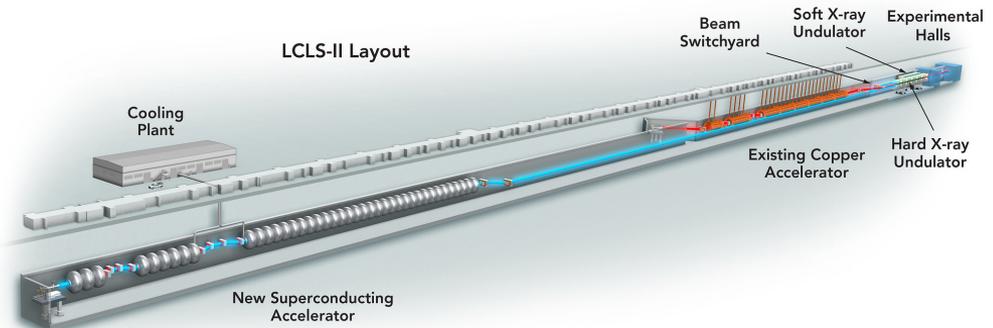 - Frequency fine adjustable
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Tuesday 14:00-15:50
Low phase noise master oscillator generation and distribution for ALS and ALS-U
Michael Betz
LBNL

LCLS-II LLRF

- SRF LLRF development and test @ JLab LERF (Low Energy Recirculator Facility)
  - Operational experience
    - screens, operating mode
  - RF / SRF calibration
  - Interlocks
  - Waveform capture
    - Cavity quench events
    - Microphonics environment
- Early injector commissioning (EIC)
  - LLRF system successfully commissioned
    - Full power CW operation
    - Transfer to operation
  - First photo emission on May 29, 2019
  - Transition to operation on Sept. 17, 2019

LCLS-II Layout

Cooling Plant

New Superconducting Accelerator

Existing Copper Accelerator

Beam Switchyard

Soft X-ray Undulator

Hard X-ray Undulator
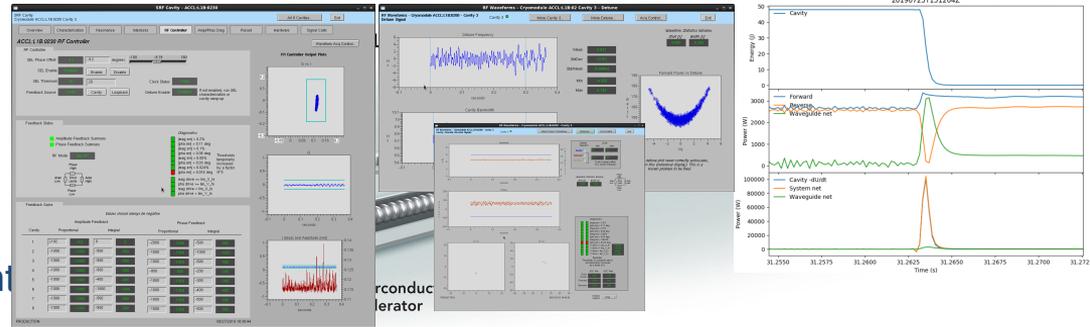
Experimental Halls

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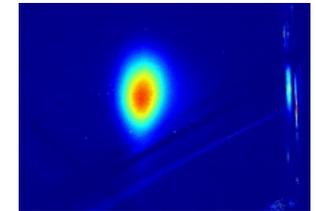 - Transition to operation on Sept. 17, 2019
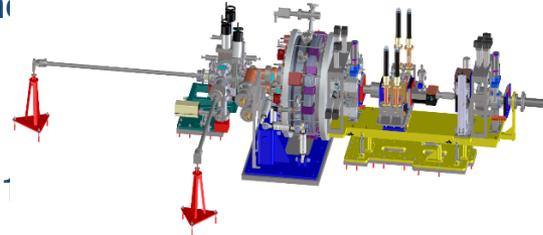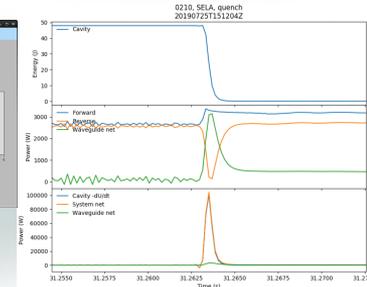
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LCLS-II LLRF

LCLS-II

SLAC NATIONAL ACCELERATOR LABORATORY
BERKELEY LAB
Argonne NATIONAL LABORATORY
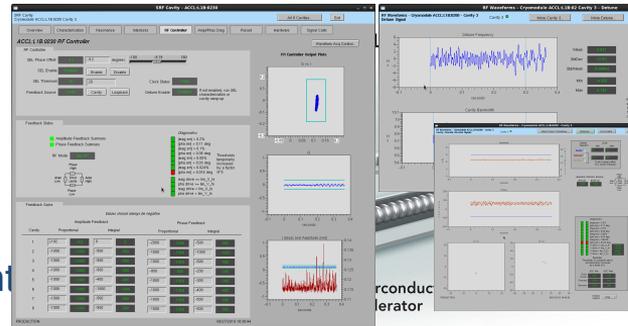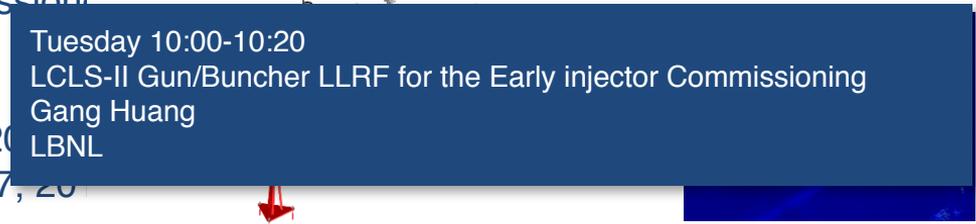CORNELL UNIVERSITY
Fermilab
Jefferson Lab

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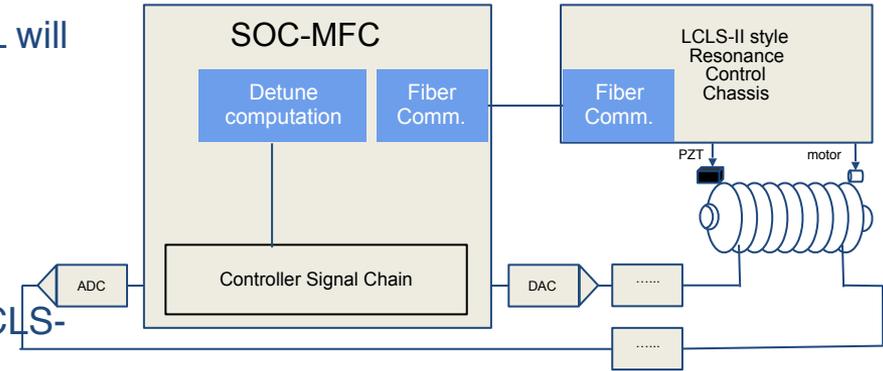Thursday 9:55-10:15
LCLS-II LLRF - Design, production and early test results
Andy Benwell
SLAC

Tuesday 10:00-10:20
LCLS-II Gun/Buncher LLRF for the Early injector Commissioning
Gang Huang
LBNL

PIP-II LLRF collaboration

- Proton Improvement Plan II (PIP-II) project at FNAL will upgrade the accelerators to 800MeV SC linac with warm frontend.

- Altera-powered SOC Multi-cavity Field Controller (SOC-MFC)
  - Detune calculation in firmware
  - Fiber based communication (chitchat) with LCLS-II style resonance control chassis over fiber
- Testing rack setup
  - FNAL chassis and Labview GUI
  - LCLS-II style cavity emulator
  - Chitchat tested between Altera and Xilinx FPGA
  - Detune calculation validating by offline waveform extraction

SOC-MFC

Detune computation | Fiber Comm.

Fiber Comm.

LCLS-II style Resonance Control Chassis

PZT | motor

Controller Signal Chain

ADC | DAC | ...... | ......

Wednesday 12:10-12:30
Resonance Control System for PIP-II 650 MHz STC at Fermilab
Philip Varghese
FNAL

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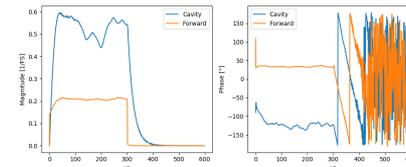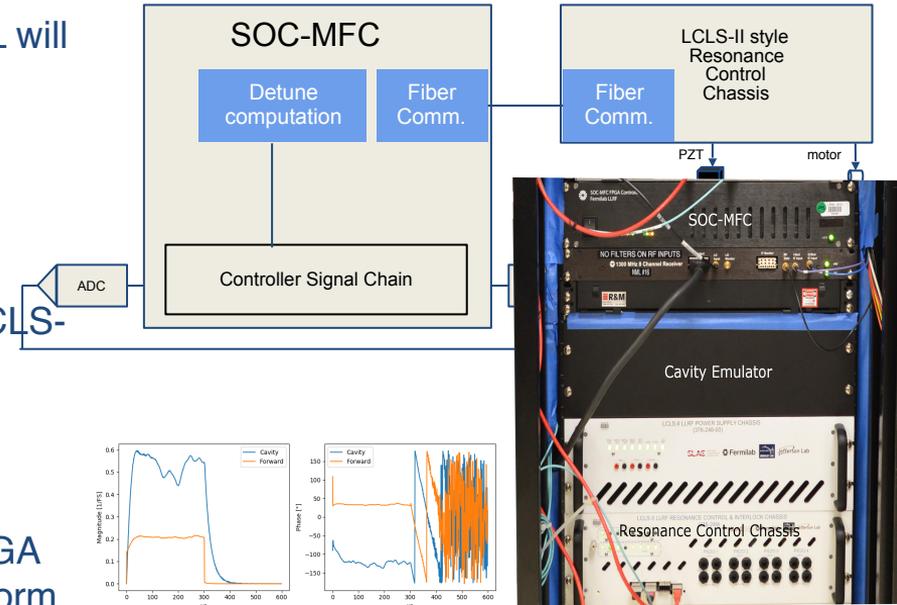 - Detune calculation validating by offline waveform extraction

Wednesday 12:10-12:30
Resonance Control System for PIP-II 650 MHz STC at Fermilab
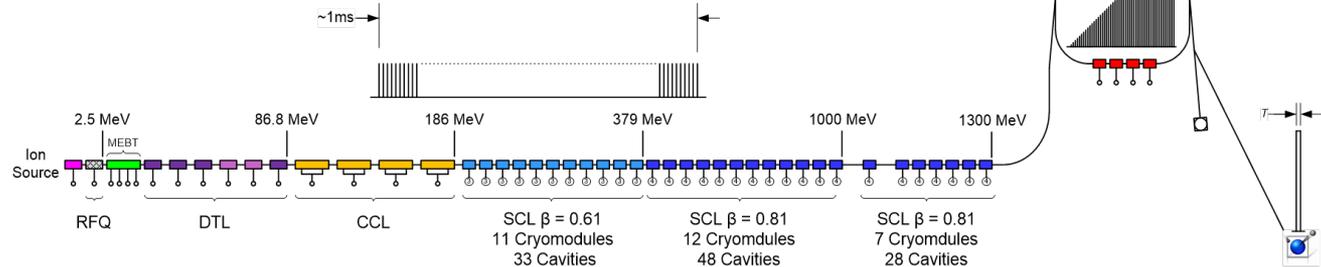Philip Varghese
FNAL

PPU@ORNL

- Proton Power Upgrade
  - 2.8 MW proton beam power
  - Install new LLRF systems to control 7 cryomodules, 28 new superconducting cavities

Monday 9:20-9:30
LLRF Status & Development Activities at the SNS
Mark Crofford
ORNL

- LBNL role
  - Implemented FPGA controls firmware for PPU
  - To be tested on cold cavities over the next year

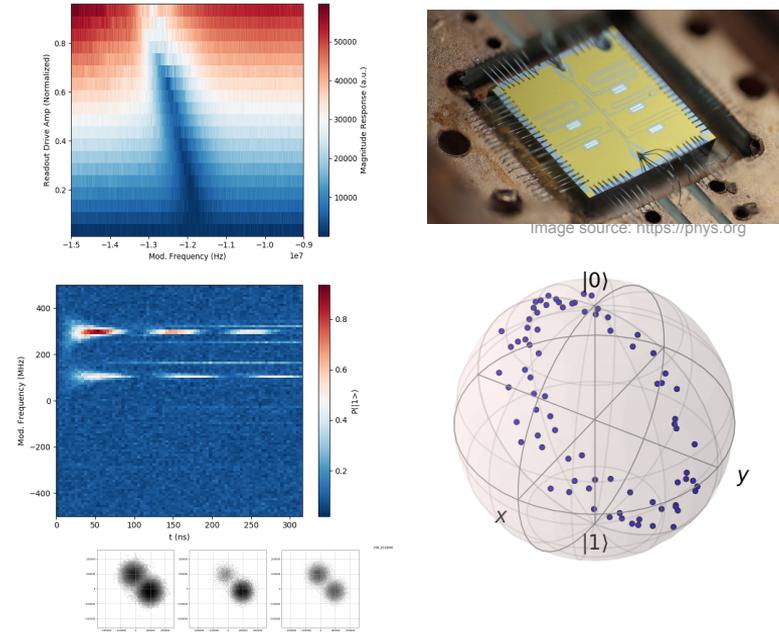| ~1ms						
2.5 MeV	86.8 MeV	186 MeV	379 MeV	1000 MeV	1300 MeV	

Ion Source

RFQ · DTL · CCL · SCL β = 0.61 11 Cryomodules 33 Cavities · SCL β = 0.81 12 Cryomdules 48 Cavities · SCL β = 0.81 7 Cryomdules 28 Cavities

Coherent laser combination

spectral splitter
spatial splitters
λ_1
front end
λ_2
fiber amplifiers (~300)
λ_3
spatial combiners (~100x)
λ_{16}
spectral combiner (~3x)
temporal combiner (~100x)
pulse compressor (1ns -100fs)
output
compressor

1Gsps 8-in 8-out chassis   200ksps 8-in 8-out chassis

25-pulse stacking result

Opt. Lett. 42, 4422 (2017)
JOSA B. 35 2081 (2018)
 IEEE J. QE 54, 1 (2018)
Opt. Lett. 43, 3269 (2018)
Opt. Lett. 44, 4554 (2019)

Quantum bit control

Image source: https://phys.org
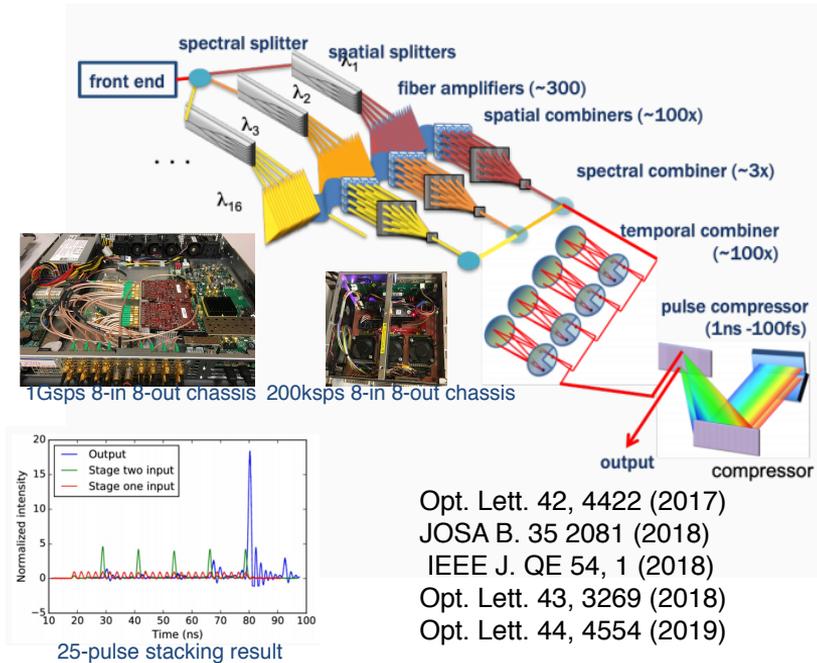
Full stack Open source

Firmware

Hardware

Software

Simulation

Beam Instrument Development System

Bedrock

Marble

Zest

FEED

CMOC

$$z = e^{st}$$

BSD licensed

OHWL licensed

License work in progress

Software Accelerator System simulation engine

Full stack Open source

Firmware

Beam Instrument Development Syste...

Bedrock

Marb...

BSD licensed

OHWL licensed

License work in progress

Firmware, software and hardware base used in our projects is Open Source

- Bedrock
  - FPGA DSP and communication code base
  - https://github.com/BerkeleyLab/Bedrock
- BIDS
  - Multiple repos for building blocks from firmware to hardware
  - https://github.com/LBL-BIDS
- Cryomodule-On-Chip FPGA simulation engine (CMOC)
  - SRF plant model running live in FPGA
  - https://github.com/BerkeleyLab/CMOC
- Software Accelerator System simulation engine
  - Integration of RF and electron tracking code for beam-RF simulations
  - https://github.com/BerkeleyLab/Global-Feedback-Simulator
- FPGA carrier board: Marble
  - Double FMC FPGA carrier board
  - https://github.com/BerkeleyLab/Marble
- ADC/DAC board: Zest
  - 6 ADC, 2 DAC FMC mezzanine
  - https://github.com/BerkeleyLab/Zest
- Used in
  - LCLS-II (SLAC), SNS/PPU (ORNL), PIP-II (FNAL), ALS/ALS-U (LBNL)

Full stack Open source

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Firmware

Beam Instrument Development Syste

Bedrock   Mar

BSD licensed

OHWL licensed

License work in progress

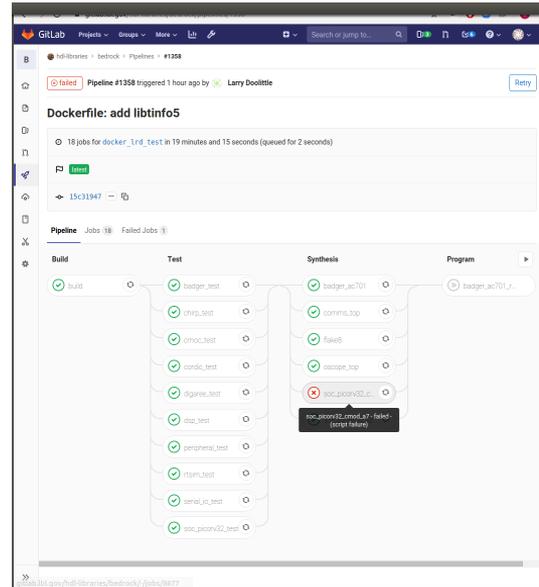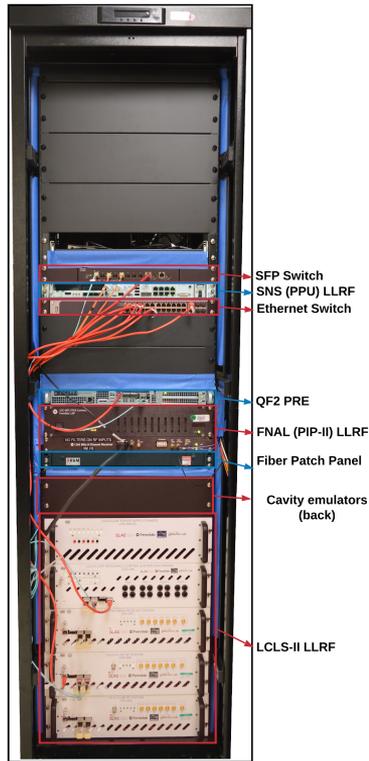Wednesday 14:00-14:30
Open Source LLRF stack
Carlos Serrano
LBNL

Continuous integration

SFP Switch
SNS (PPU) LLRF
Ethernet Switch

QF2 PRE
FNAL (PIP-II) LLRF
Fiber Patch Panel
Cavity emulators
(back)

LCLS-II LLRF

Continuous integration

Tuesday 14:00-15:50
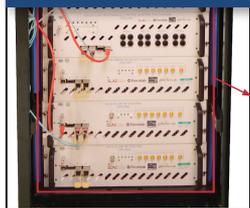S1-30 Hardware-in-the-Loop testing of accelerator firmware
Carlos Serrano
LBNL

ICALEPCS 2019
LBNL FPGA development flow, Vamsi Vytla, LBNL
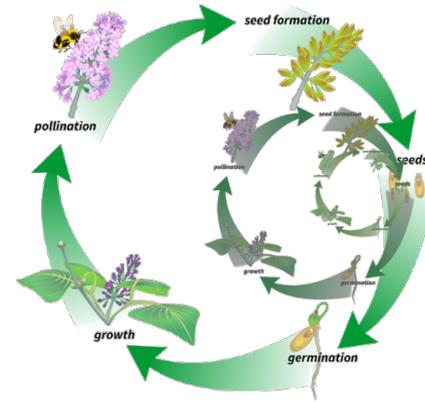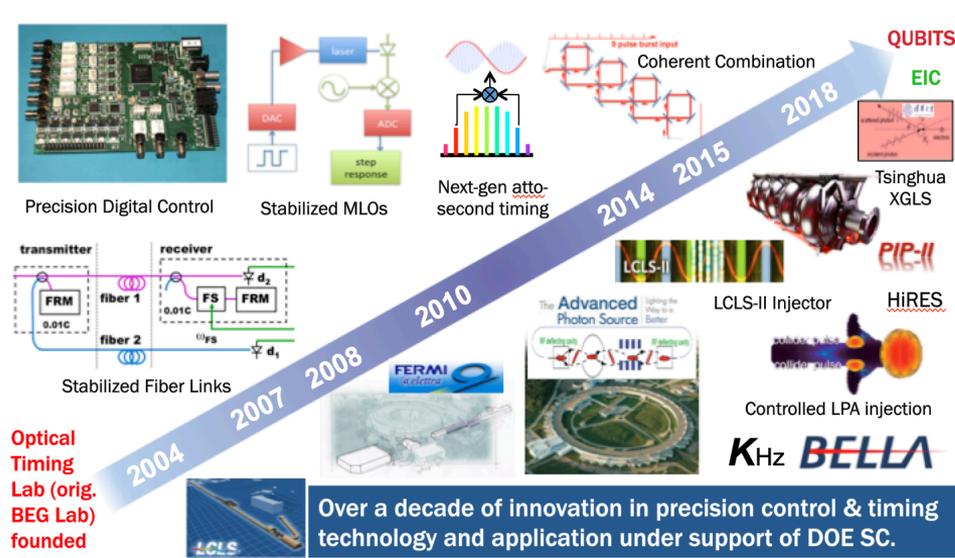Hardware in the loop testing of accelerator firmware, Carlos Serrano,
LBNL

LCLS-II LLRF

Summary

- Open to collaboration
- Opening for postdoc and engineer positions

Summary

Oct. 1, 2019 Tuesday

    09:10-09:40 Digital LLRF system for Advanced Light Source Storage Ring RF, Q.Du, LBNL, USA

    10:00-10:20 LCLS-II Gun/Buncher LLRF for the Early Injector Commissioning, G. Huang, LBNL, USA

    Poster Session I

        Low phase noise master oscillator generation and distribution for ALS and ALS-U, M. Betz, LBNL, USA

        Hardware-in-the-loop Testing of Accelerator Firmware

Oct. 2, 2019 Wednesday

    14:00-14:30 Open Source LLRF stack, C. Serrano, LBNL, USA

Oct. 5, 2019 Saturday

LBNL FPGA development flow, V. Vytla, LBNL, USA

Oct. 8, 2019 Tuesday

Hardware In Loop testing of accelerator firmware, C. Serrano, LBNL, USA