LUCRECE DLLRF Status

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INTRODUCTION

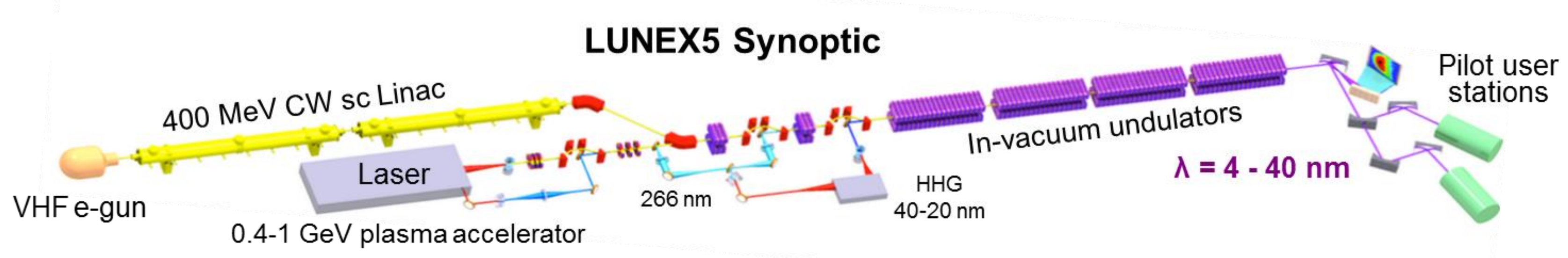
The LUCRECE project aims at developing an elementary RF system (cavity, power source, LLRF and controls) suitable for continuous (CW) operation at 1.3 GHz in Energy Recovery Linacs (ERL) and VUV-X-ray femtosecond free electron laser (FEL) based light sources at high repetition rate. It takes place in the context of the LUNEX5 (free electron Laser Using a New accelerator for the Exploitation of X-ray radiation of 5th generation) advanced and compact FEL demonstrator, using superconducting linac technology for high repetition rate and multi-user operation.

A 1.3 GHz superconducting accelerating structure and its related components (tuner, fundamental and HOM couplers, Helium manifold, etc.) will be designed for CW operation.

A 20 kW 1.3 GHz solid state amplifier (SSA) will be developed and constructed, based on the SOLEIL technology already in use at lower frequencies (352 MHz and 500 MHz), but relying on the emerging Gallium Nitride (GaN) transistor technology.

The 20 kW CW operation of the complete RF assembly will be validated in the CEA CryHoLab test station. The SOLEIL LLRF team is in charge of developing a µTCA based digital LLRF prototype, which status is reported in the present poster.

LUCRECE : RF R&D program for LUNEX5



Phase 1 : based on a 400 MeV CW sc Linac → explore advanced FEL techniques and applications

Phase 2 : laser wakefield (or plasma) accelerator will be assessed in view of FEL applications

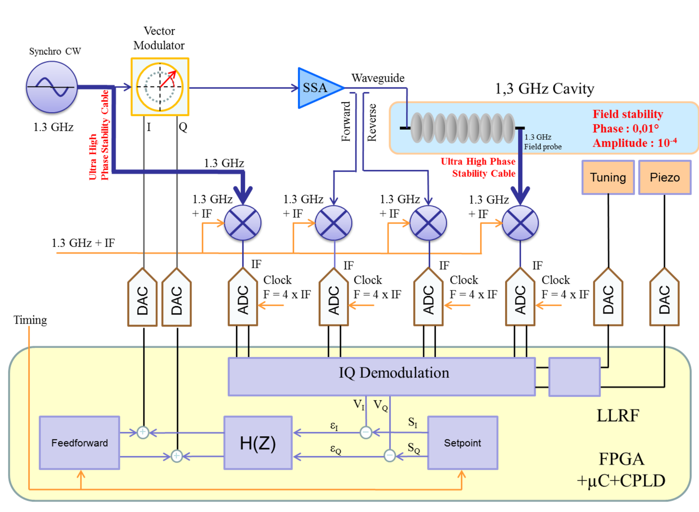
- **Collaboration between SOLEIL and CEA-DACM for the 400 MeV conventional LINAC (phase 1)**
  - ***2 x 200 MeV LCLS-II type cryomodules of 12 m (CW operation)***
  - ***One RF power amplifier for each cavity 16 x 16 kW @ 1.3 GHz (not the most economical but the best way for achieving the required cavity field stability)***
  - ***LLRF system (0.01° in phase and 10^{-4} in amplitude) with its associated synchronization part***

LUCRECE LLRF basic design

First step in the RF R&D for LUNEX5 project, LUCRECE aims at developing a complete RF elementary cell (cavity, power source, LLRF and control) adapted to CW operation to be used for ERLs or femtosecond multi-user FEL at high repetition rate.

LUCRECE tasks:

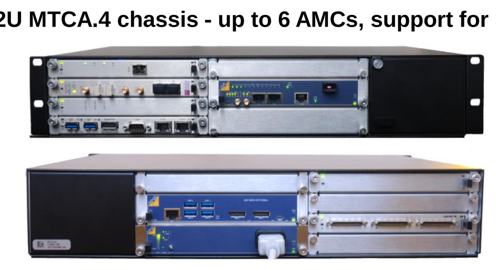
- *A 1.3 GHz CW TESLA-shaped cavity [CEA, SOLEIL]*
- *A 20 kW CW input power coupler [CNRS-LAL, THALES, SOLEIL]*
- *A digital LLRF system (10^{-4}, 0.01°), based on FPGA + CPLD + µController [SOLEIL, CNRS-LAL]*
- *Cryomodule mechanical studies [CEA, ALSYOM, SOLEIL]*

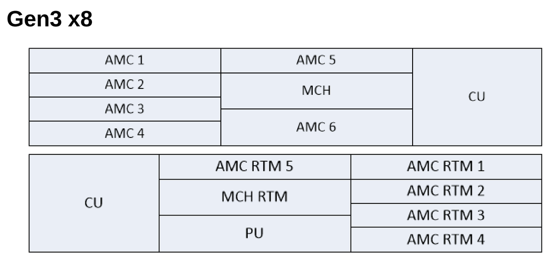


Upcoming tasks

Native-R2 µTCA platform

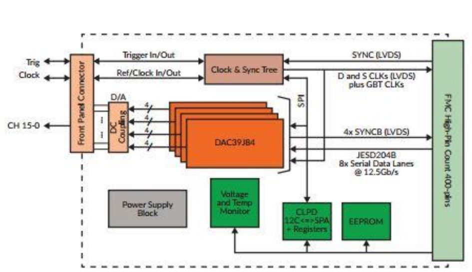
2U MTCA.4 chassis - up to 6 AMCs, support for PCIe Gen3 x8





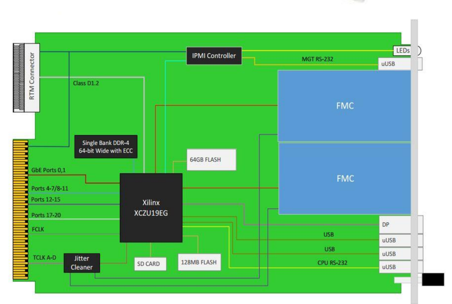
AMC580 board from Vadatech

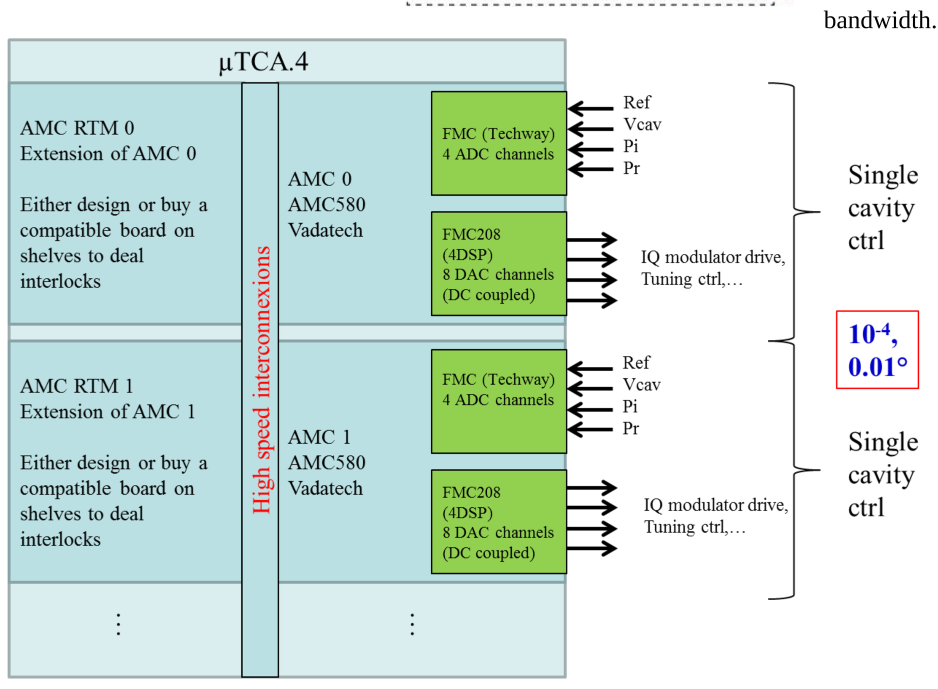
FMC208 DAC board from 4DSP



4 (CH0-CH7 for FMC204)
Channel resolution: 16-bit
Output voltage range: 2.0Vpp

Sampling Frequency Range: up to 312.5Msps → This may be further limited by JESD204B channel bandwidth.





Unfortunately, µTCA.4 standard specifications are not fully respected by all manufacturers.

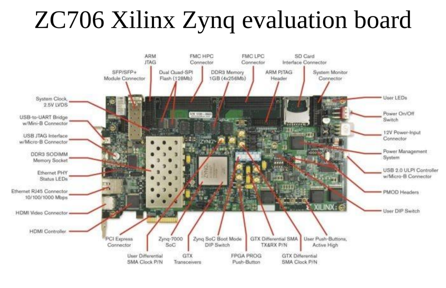
We are still trying to operate the Vadatech AMC580 in the Native µTCA chassis.

Once controlling the AMC, we will migrate all implementation done on ZC706 in the AMC580.

Then the DAC board will be integrated.

What is already achieved

ZC706 Xilinx Zynq evaluation board

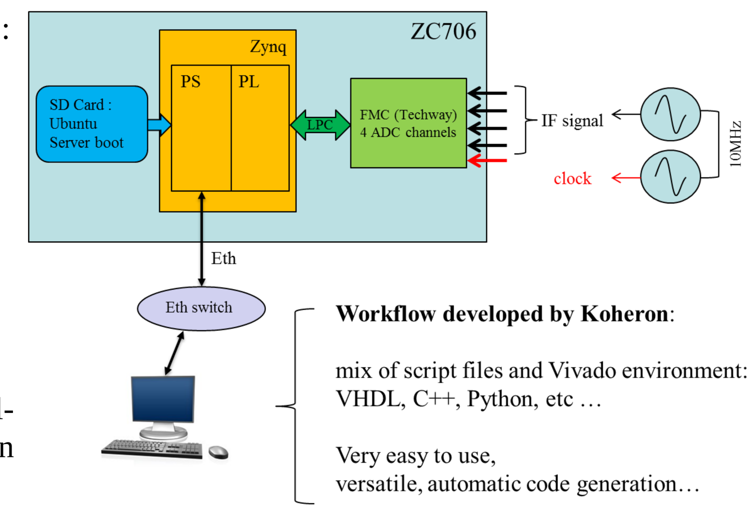


4 channel ADC FMC board (TECHWAY)

RF cavity field stability requirements are : 0.01° in phase and 10^{-4} in amplitude
1 LLRF + 1 SSA per cavity.

Digital LLRF based on IQ (or non-IQ) demodulation will give all the flexibility to implement different operating modes (CW or pulsed).

The main characteristic of ADCs and DACs are high bit resolution, good signal-to-noise ratio, low jitter and low latency in order to meet the required stability performance.



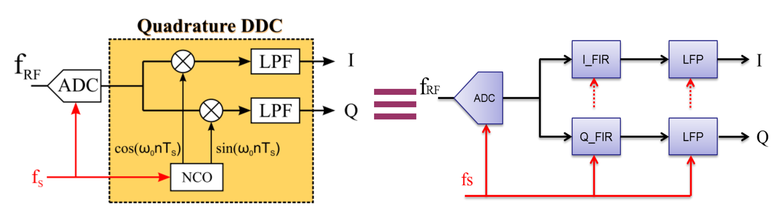
Workflow developed by Koheron:

mix of script files and Vivado environment: VHDL, C++, Python, etc …

Very easy to use, versatile, automatic code generation…

Complete LLRF design in collaboration with LAL (Orsay)

- R&D, component choice
- Component performance test
- Production of the complete system
- Test with the cavity

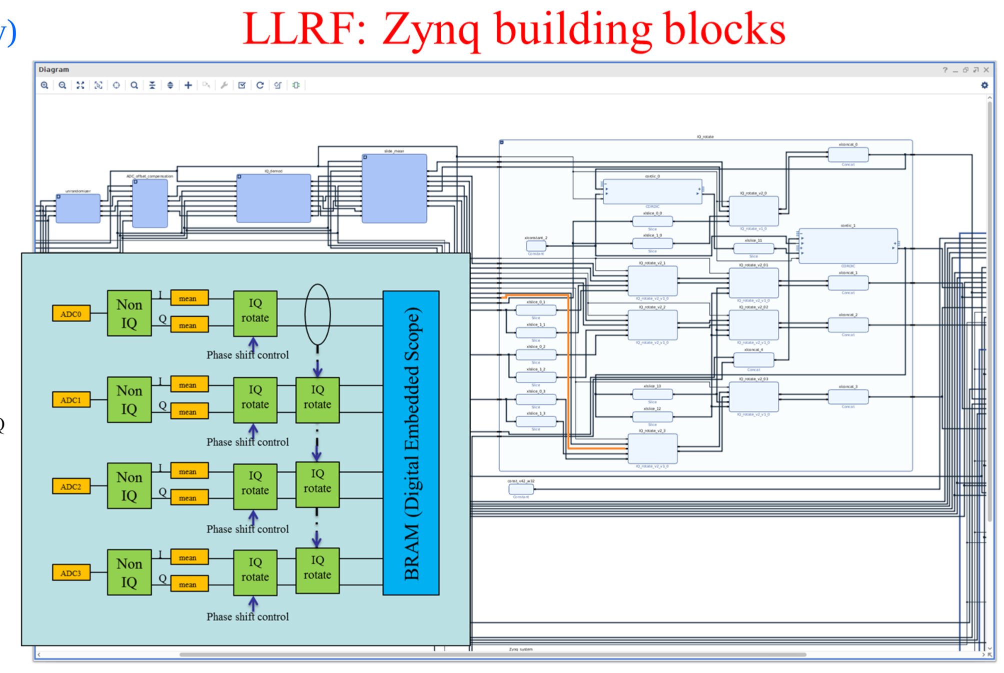


M . f$_{RF}$ = N. fs Δφ = 2Π. N/M

$$I = 2/M \sum_{i=0}^{M} y_i \cdot \cos(i.\Delta\varphi) \quad \text{Coef\_FIR\_I}(i) = \cos(i.\Delta\varphi)$$

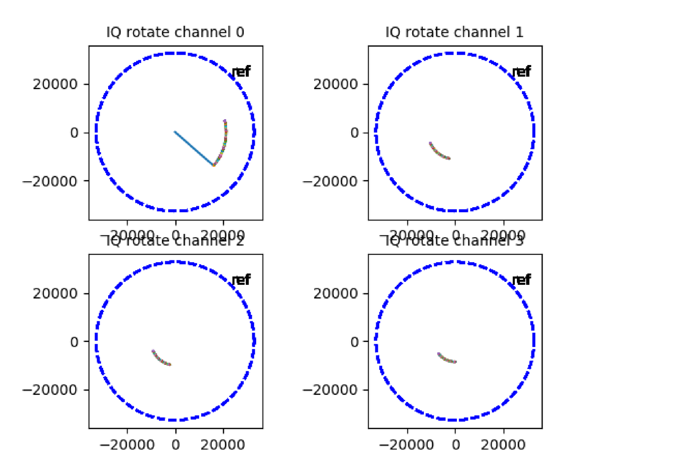
$$Q = 2/M \sum_{i=0}^{M} y_i \cdot \sin(i.\Delta\varphi) \quad \text{Coef\_FIR\_Q}(i) = \sin(i.\Delta\varphi)$$

LLRF: Zynq building blocks



$\frac{f_{RF}}{f_s} = \frac{N}{M} = \frac{4}{9}$ ⇨ With this ratio and 64 values of sliding mean, real measurements give 0.02° rms. We have to improve it and test other ratios.

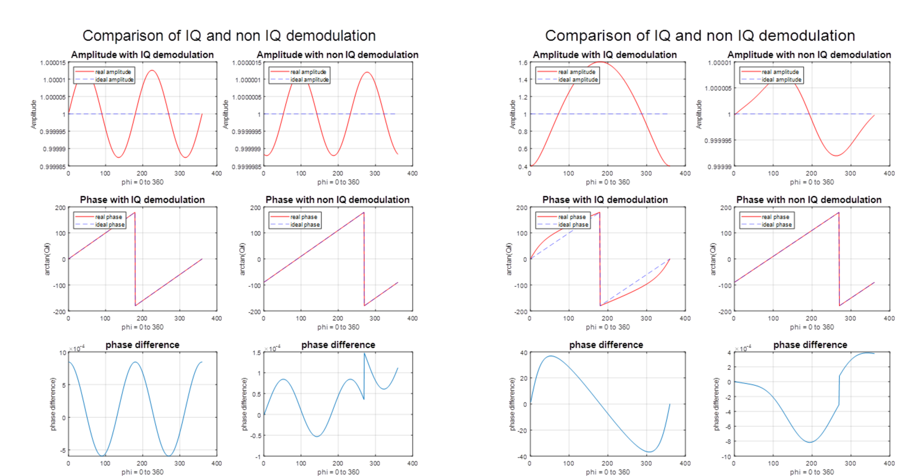
Measured rotated IQ values



Non-IQ method is suitable for IF signal with harmonics from mixer stage. Classical IQ method is more sensitive to harmonics and produces phase and amplitude errors.

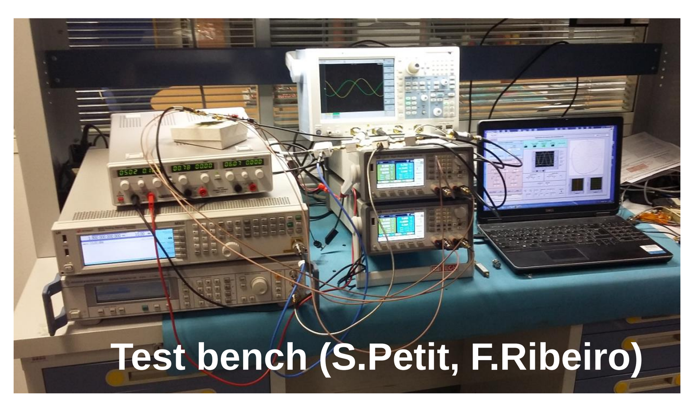
Digital non-IQ demodulation method

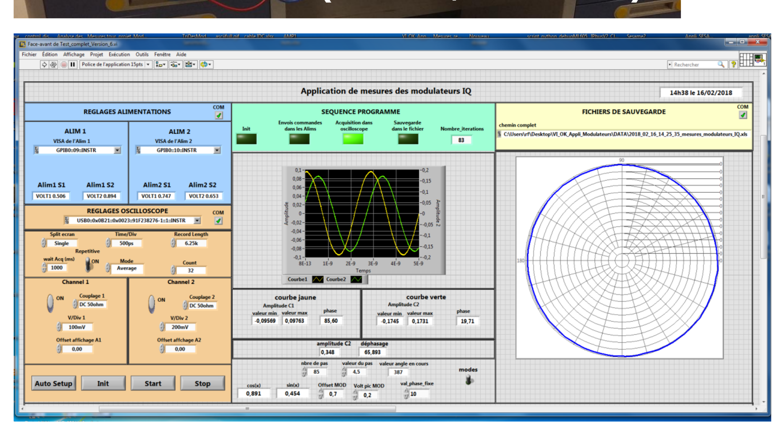
Matlab simulation:
Comparison IQ vs non-IQ with some harmonics introduction on the IF signal

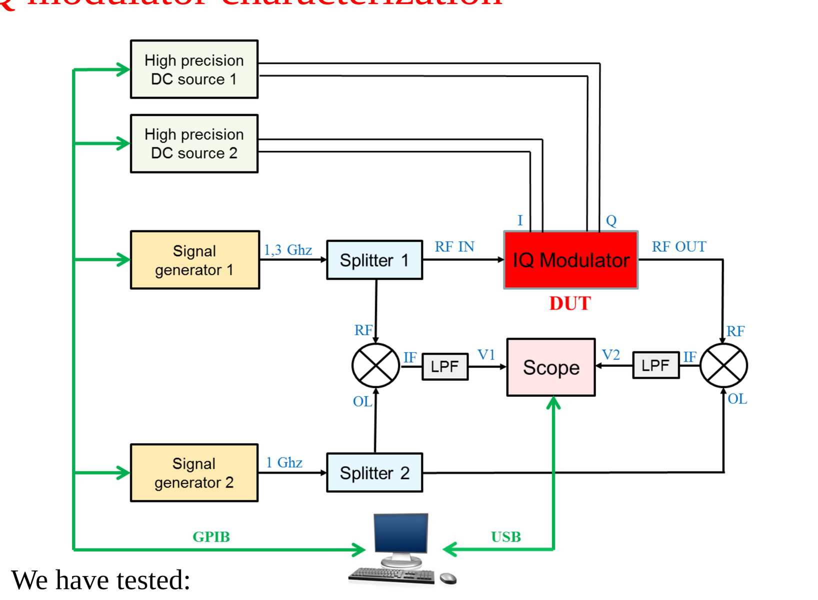


With jitter and without harmonics   With jitter and harmonics

Automatic benchmark for analog IQ modulator characterization







We have tested:

LTC5598

AD8345

TRF370333, …

We have selected LTC5598 for its good linearity.

LUCRECE DLLRF status

SOLEIL has selected the Zynq technology for the LLRF digital processing system of LUCRECE project. Preliminary tests were performed using ZC706 Zynq board, interfaced with a four channel ADC FMC board from Techway. All basic signal processing modules relying on Non-IQ demodulation technic were successfully implemented and tested. The presence of an ARM processor with a classical FPGA on the same chip makes the communication part very easy. The FPGA is working with IQ and the ARM transforms IQ in amplitude and phase.

All the developed modules have now to be migrated on the Zynq based AMC580 board which is integrated in a µTCA platform. Unfortunately, it turned out that the Vadatech AMC580 board was not compatible with the Native µTCA, an issue which is under investigation.

Then SOLEIL Tango control system will be embedded on the Zynq part and the DAC board will be interfaced in order to complete the system. We expect that it will meet the very tight precision (0,01°) , required for LUCRECE LLRF.