LLRF system used for testing the RFQ prototype o MYRRHA

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Injector's facility at LLN

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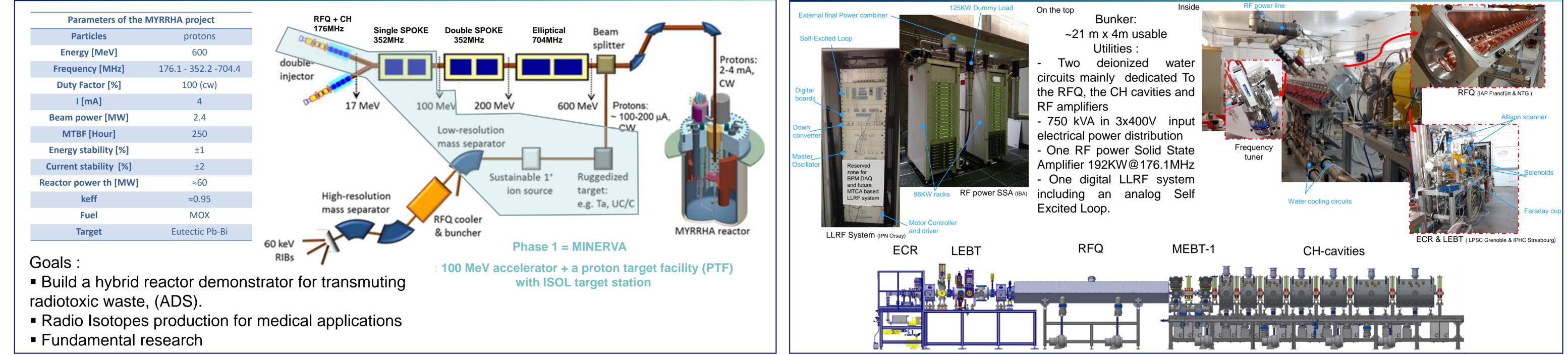




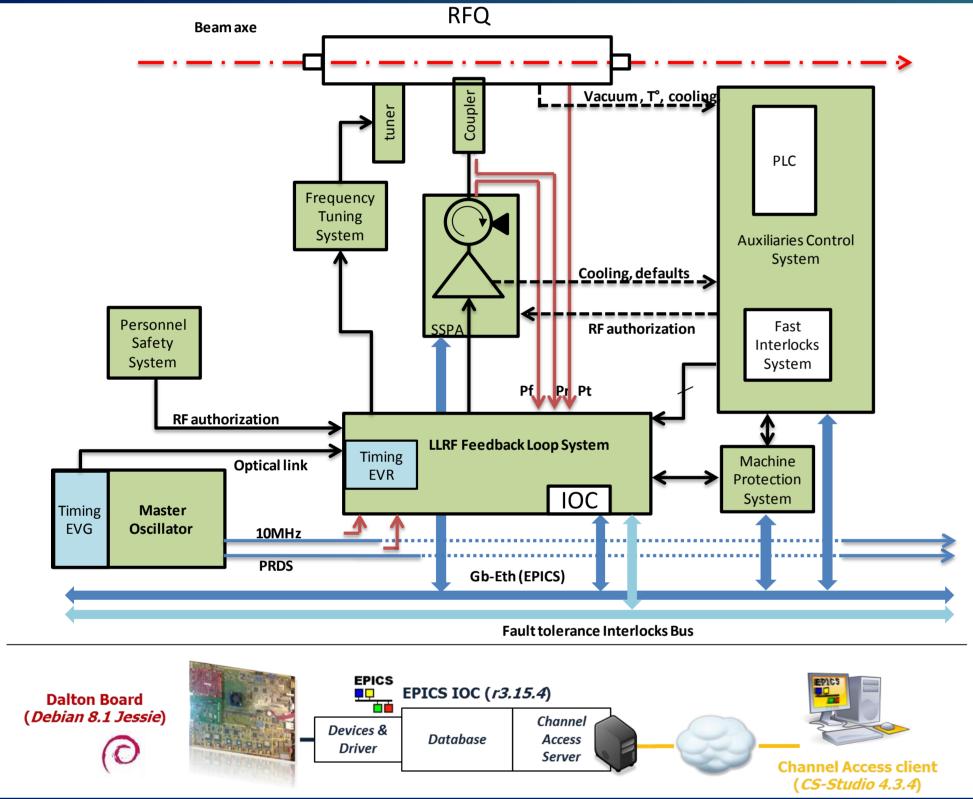
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Within the framework of the European project MYRTE (MYRRHA Research and Transmutation Endeavour) of the H2020 program, a 4-Rods RFQ (Radio Frequency Quadrupole) has been designed at 176.1 MHz RFQ for accelerating up to 4 mA protons in CW operation from 30 keV up to 1.5 MeV. A LLRF prototype has been developed to regulate the amplitude and the phase of the accelerator field into the RFQ and the frequency of the RFQ controlling the motor of the RFQ frequency tuner. Here, we present the facility at Louvain-la-Neuve, with a focus on its LLRF, as well as some preliminary results.

Conceptual layout of the MYRRHA Facility



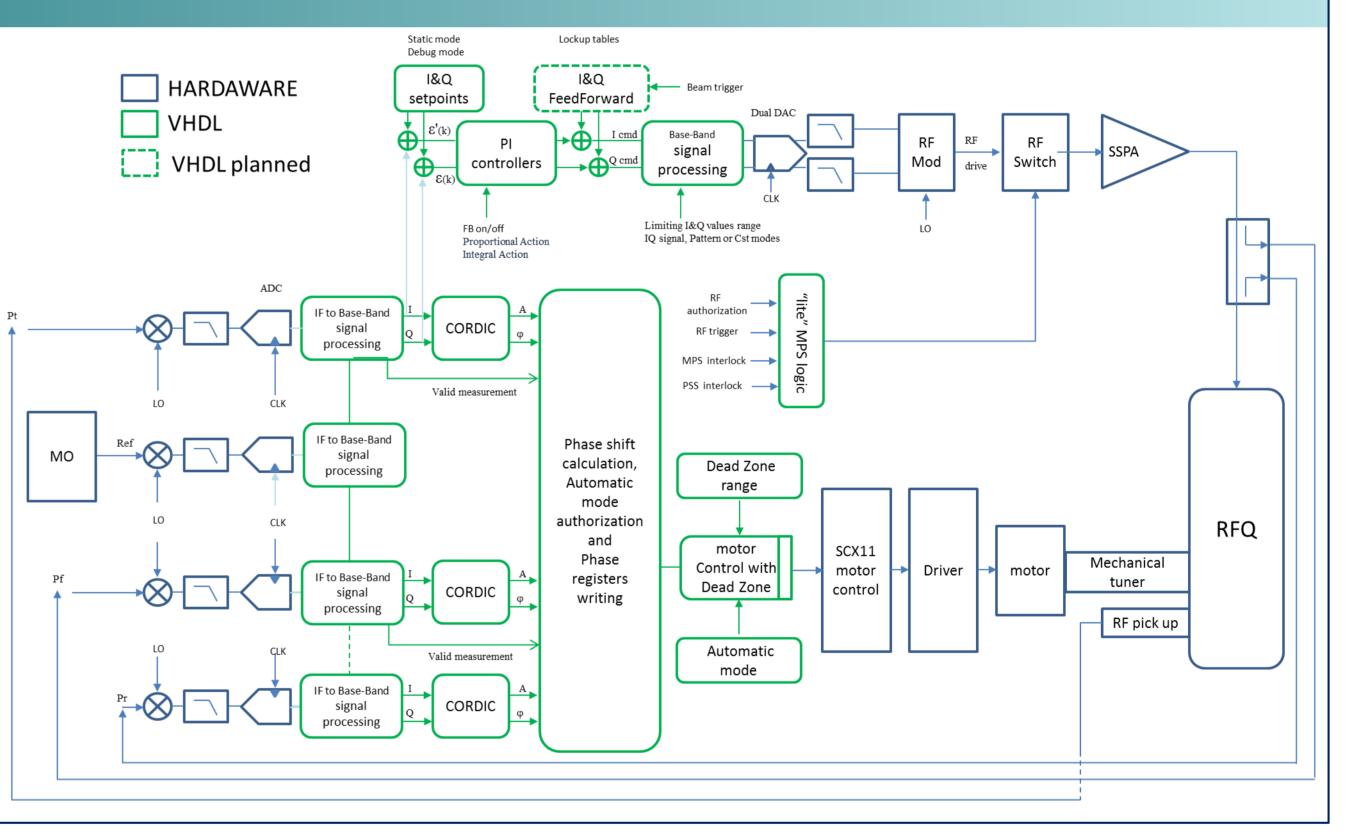
LLRF system



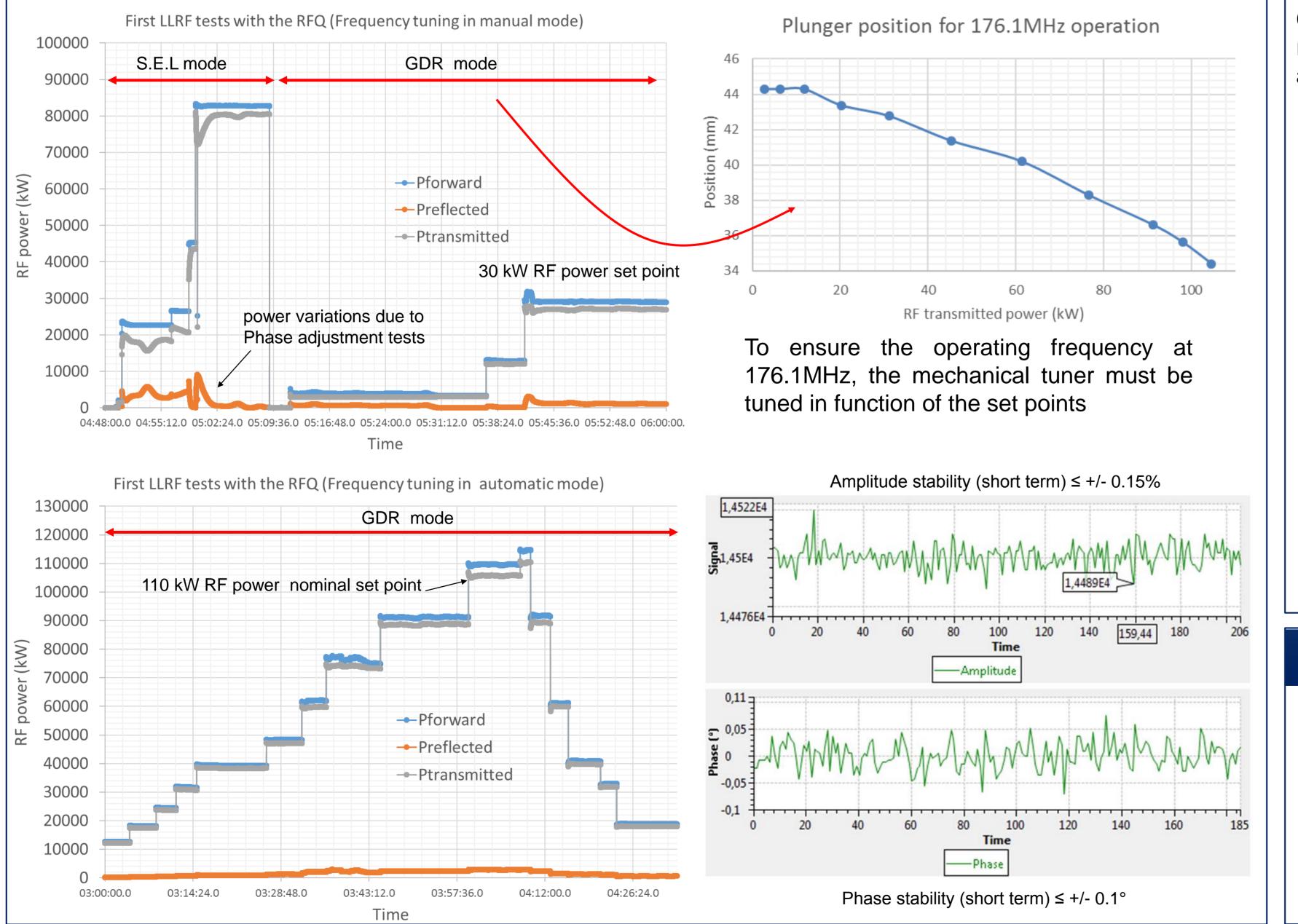
The LLRF prototype system for the RFQ is based on a in-house digital motherboard called DALTON using a FPGA linked to a processor ARM by PCIe, with two FMC slots.

For HW and SW details, see "EPICS and VHDL developments in the LLRF for MYRRHA Project's RFQ prototype" poster,LLRF17.

FPGA's signal processing provides the IQ inputs signals for two main loops. The first one is the RFQ's cavity field amplitude and phase regulation using Proportional and integral corrections. The second loop maintains the RFQ's frequency with a phase shift measurement between incident and transmitted signals which drives the motorized tuner. Future additions to the hardware architecture include a feed forward functionality for reducing the beam loading. EPICS IOC implemented into the embedded processor distributes and receives the PV to/from the CSS supervision (GUI) developed by IPNO team allow the global LLRF system to be controlled and commanded.



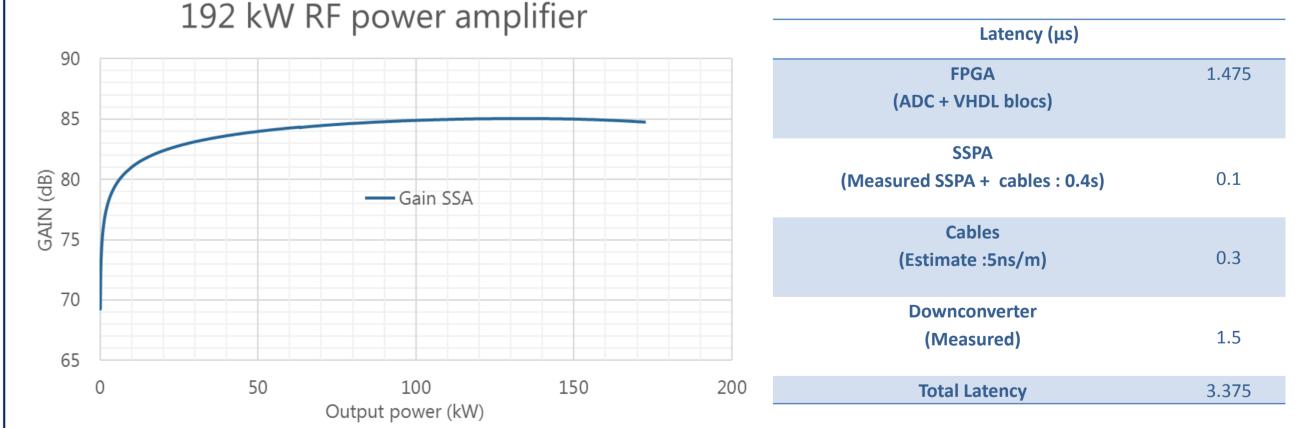
Tests results without beam



Improvements

Concerning the amplitude and phase, the stability values have been greatly improved with respect to the gain augmentation of the RF power amplifier with values better than 0.1% and 0.1°.

In return, associated to the global latency, the gain and phase margins are limited.



To increase the gain keeping typical margins, the latency must be reduced. It was decided to change the Intermediate Frequency, from 10MHz to 20MHz, which allows the FPGA signal processing clock to be multiplied by a factor of two compatible with the maximum clock rating with few VHDL modifications and new IF filters with low group delay to be used. The objective is a latency value around 1.3 μ s.

Acknowledgements

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Conclusion

The in-house LLRF system designed by IPNO is validated with the RFQ (without beam) at the nominal RF power (110KW). However, some improvements are in progress for increasing margins stabilities and facilitating the operator's job. The validation with the beam is planned for next year. In parallel, a LLRF MTCA based development is on-going within a collaboration contract between SCK•CEN and IN2P3, benefiting from MYRTE developments and tests - see Article and Poster "A µTCA-based Low Level RF System prototype for MYRTHA 100 MeV project", LLRF2019.