A µTCA-based Low Level RF System prototype for MYRRHA 100 MeV project

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Abstract

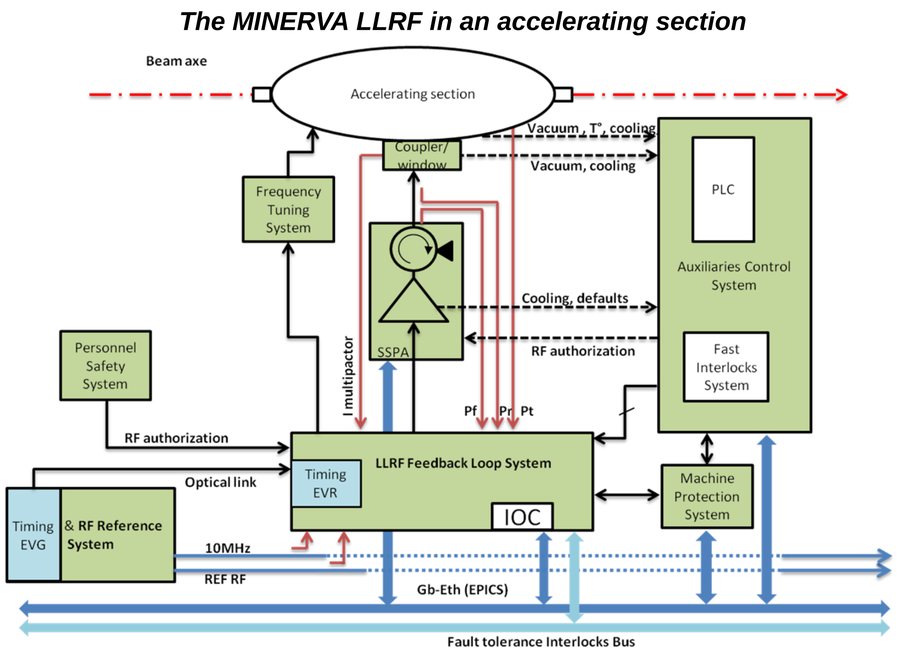
MYRRHA (Multi-purpose hYbrid Research Reactor for High-tech Applications) is a European project, whose aim is to demonstrate radiotoxic waste transmutation through the design of an ADS (Accelerator Driven System) : a hybrid reactor, driven by a superconducting proton LINAC operating at 600 MeV. From the beginning of 2016, the SCK•CEN is in charge of MINERVA (MYRRHA Isotopes productioN coupling the linEar acceleRator to the Versatile proton target fAcility) project : building the first section of the accelerator, up to 100 MeV. Through collaboration with SCK•CEN, IPNO takes in charge the developments of several parts of the accelerator, including a fully equipped Spoke cryomodule prototype and a cold valves box. This cryomodule will integrate two superconducting single spoke cavities operating at 2K, the RF power couplers and the cold tuning systems associated.

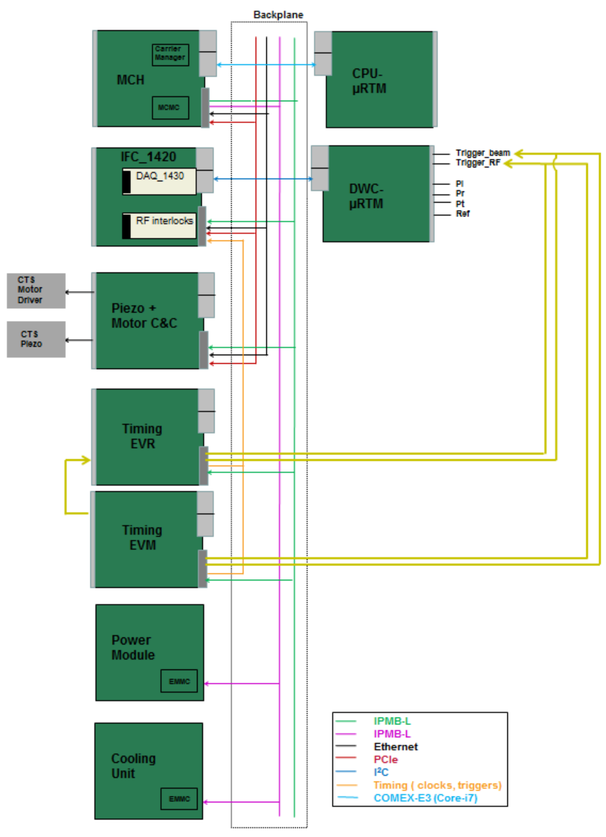
For cavity field control and regulation purpose, a µTCA LLRF system prototype is being implemented. It strongly benefits from the return on experience from MYRTE (MYRRHA Research and Transmutation Endeavour, design of an injector prototype) project (design of the prototype of MYRRHA's injector), where IPNO was also in charge of the LLRF (see poster "***LLRF system used for testing the RFQ prototype of MYRRHA***"). This µTCA-based LLRF will be presented here alongside with the hardware, VHDL and EPICS associated developments that aim to fulfil MYRRHA's ambitious requirements.

The MINERVA µTCA version of the LLRF

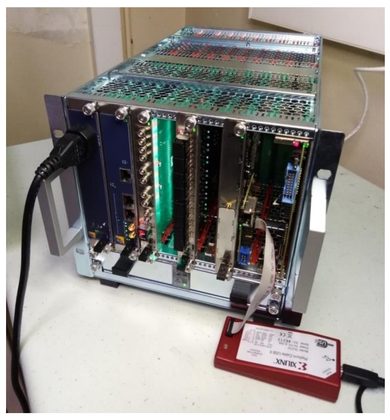
For the LLRF under development at IPNO, a special focus was given on reliability and mass production : the µTCA standard indeed provides systems with a high availability and reliability (99.9% without redundancy, 99.999% else), and on-the-shell industrial solutions for the different components of the LLRF were also maximized to design a uniform, modular and rugged system. The RF front end (downconverter) is realized through a collaboration between IPNO and IOxOS Technologies, and the RF interlocks (FMC board embedded with the digital LLRF) is an in-house development.

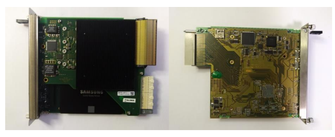
The MINERVA LLRF in an accelerating section





Currently, all the hardware, except the downconverter µRTM module and the RF interlocks (embedded in the IFC_1420), has been acquired and assembled in a **Native-R5** chassis from N.A.T.





- MCH (µTCA Carrier Hub): **NAT-MCH-PHYS**, from N.A.T, equipped with a **NAT-MCH-RTM-COMex-i7** µRTM CPU module.
- **IFC_1420**: from IOxOS Technologies, dedicated to the digital part of the LLRF, equipped with two FMC slots: one DAQ_1430 (16-bit ADC channels at 250 Msps and four 16-bit DAC channels at 2.5 Gsps for data acquisition), and one RF Interlocks (multipacting and arc detection board, dedicated to the RF couplers). These FMCs are controlled by a Xilinx Kintex UltraScale FPGA KU040. The board embeds a PowerPC (NXP QorIQ T2081 processor @ 1.8 GHz)..
- **Piezo + Motor C&C**: AMC associated to an external linear power rack allowing the frequency tuning of the cavity using piezoelectric and motor controllers. A first prototype including only the piezoelectric controller was developed and validated through collaboration between IPNO and LPSC (Laboratoire de Physique Subatomique et de Cosmologie).

- Power module: **NAT-PM-AC600D** from N.A.T (110-240VAC, 600W output)

- Timing EVM (EVent Master): **mTCA-EVM-300** board from MRF (Micro Research Finland).

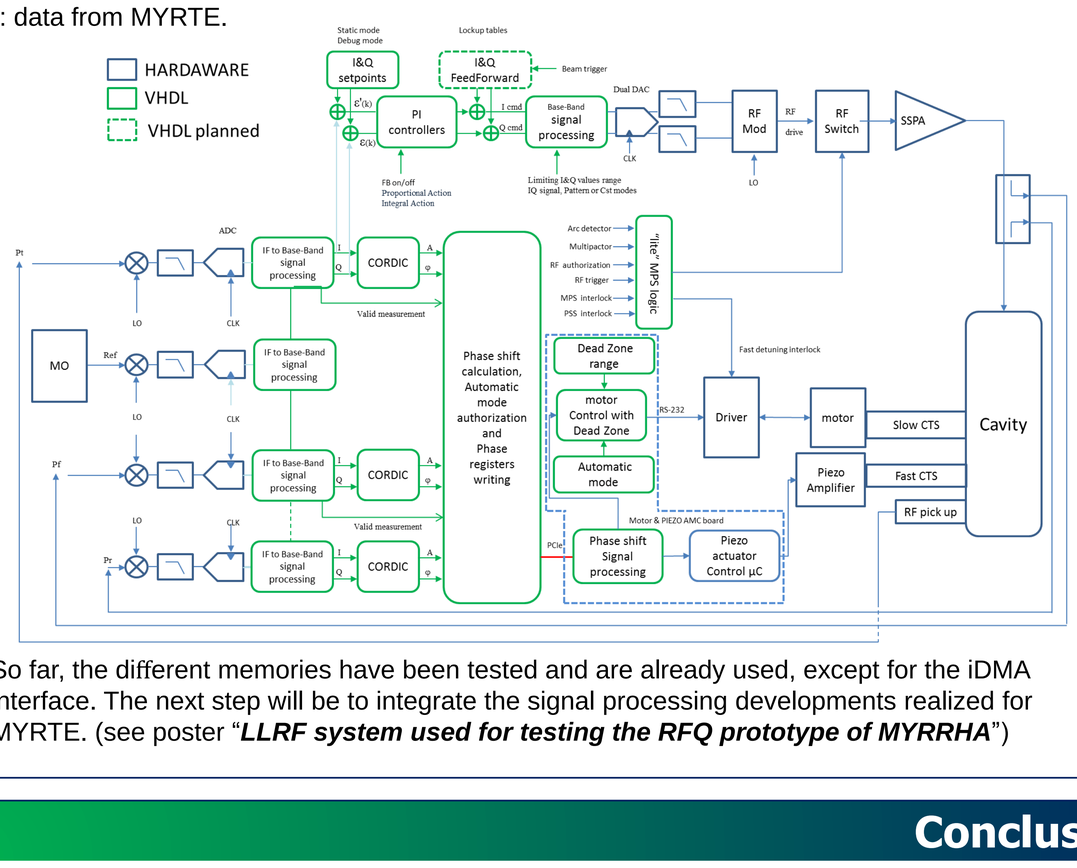
- Timing EVR (EVent Receiver): **mTCAEVR-300U** board, also from MRF.

VHDL programming using TOSCA IIB

Function	FPGA Location	TOSCA Interface	Data Size	Number of Elements
Set-points, Boolean indicators	Registers	TCSR	32 bits	~ 40 *
Medium-Sized Frame	FIFOs	TMEM	64 bits	10 *
Patterns	FIFOs	TMEM/ SMEM	64 bits	2*
Monitoring Frame	DMA	iDMA	64 bits	1*
Circular Buffer (Simple/Double)	DMA	iDMA	64 bits	1-2

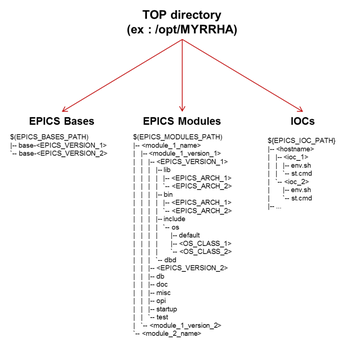
*: data from MYRTE.

In the IFC-1420 digitizer's FPGA is powered by IOxOS Technologies proprietary TOSCA FPGA Design Kit (TOSCA IIb), a design environment for custom VHDL application. It allowed to select different kind of memories associated to each communication functionality (Set-Points, acquisition FIFOs, history).



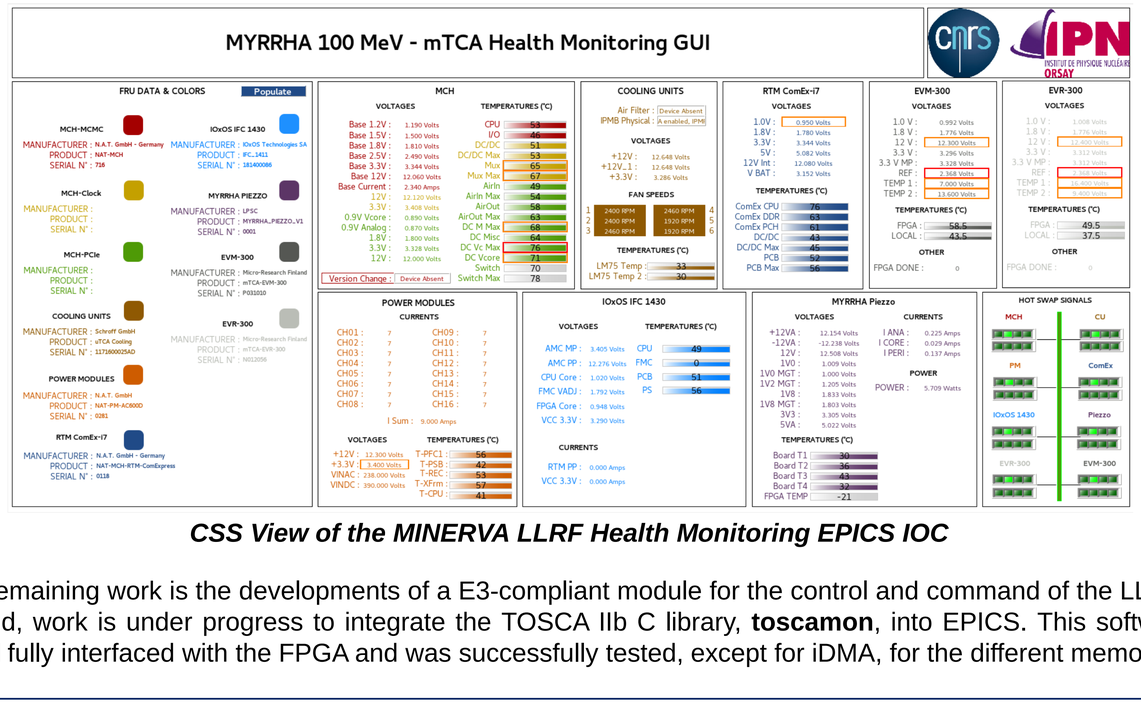
So far, the different memories have been tested and are already used, except for the iDMA interface. The next step will be to integrate the signal processing developments realized for MYRTE. (see poster "***LLRF system used for testing the RFQ prototype of MYRRHA***")

EPICS Developments



For MYRRHA, EPICS was chosen to perform the accelerator's control and command. Developments made so far at IPNO followed the model of E3 (ESS EPICS Environment), the control architecture used by ESS (European Spallation Source).

A E3-compliant modules has been designed for the general supervision of the crate (based on E3 **ipmi-epics** module), able to scan the system using IPMI (Intelligent Platform Management Interface) requests, and generate a complete sensor's database describing the system (i.e. for temperature, voltage sensors). The module can also relate one PV to its physical hardware, and thus ensure PV's name unicity as well as ease maintenance operations.



CSS View of the MINERVA LLRF Health Monitoring EPICS IOC

Main remaining work is the developments of a E3-compliant module for the control and command of the LLRF. To this end, work is under progress to integrate the TOSCA IIb C library, **toscamon**, into EPICS. This software is indeed fully interfaced with the FPGA and was successfully tested, except for iDMA, for the different memories.

Conclusion and Perspectives

The µTCA-based LLRF prototype under development at IPNO benefits from MYRTE feedback as well as the possibilities given by the µTCA standard. The first step of the development, the selection of the different hardware components and the assembly of a complete µTCA crate, was finished by the end of 2018. The following phase consisted of the deployment of E3, the design of the µTCA health monitoring IOC, and the mastering of the TOSCA IIb environment provided by IOxOS Technologies. Remaining work consists of both the integration of MYRTE VHDL developments for the signal processing into the TOSCA environment, and the design of an EPICS wrapper module to handle communications with the IFC_1420 board directly in the E3 architecture. The design of this µTCA version of the MINERVA LLRF is under progress, and a first prototype is planned for 2020, so that it could be validated through on-site tests, before the RF tests taking place during the second semester of 2021.