SPS 200 MHz MicroTCA Cavity Controller

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SPS Upgrade
LIU Project

SPS 200MHz Cavity controller [3]

The SPS Low Level RF undergoes a complete upgrade during the CERN-wide machine stop 2019-2020. The Cavity controllers (one system per cavity) regulate the accelerating voltage in the cavities. They compensate the beam loading, including the transients caused by the beam gaps, thereby suppressing the Coupled-Bunch instability. The previous system relied on a beam synchronous clocking scheme while the new system uses a fixed 125 MHz clock. To keep the six cavities in phase during the ramp, the instantaneous frequency is transmitted through a deterministic serial data link, the White Rabbit that is also used to reconstruct the fixed-frequency sampling clock (125MHz).The system is implemented on a MicroTCA platform, using commercial off-the-shelf (COTS) modules wherever possible. Communication with the Beam control is done through a 8 Gbps serial link.
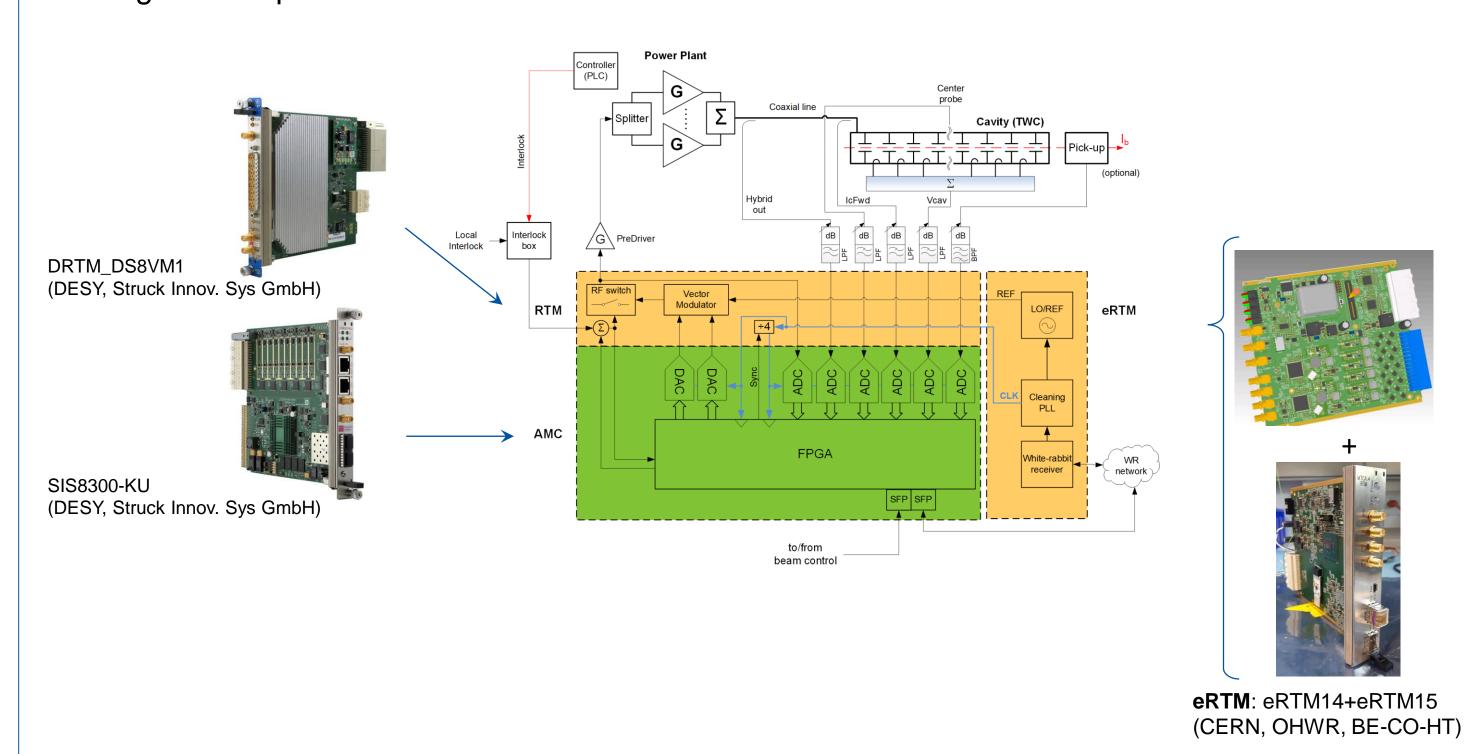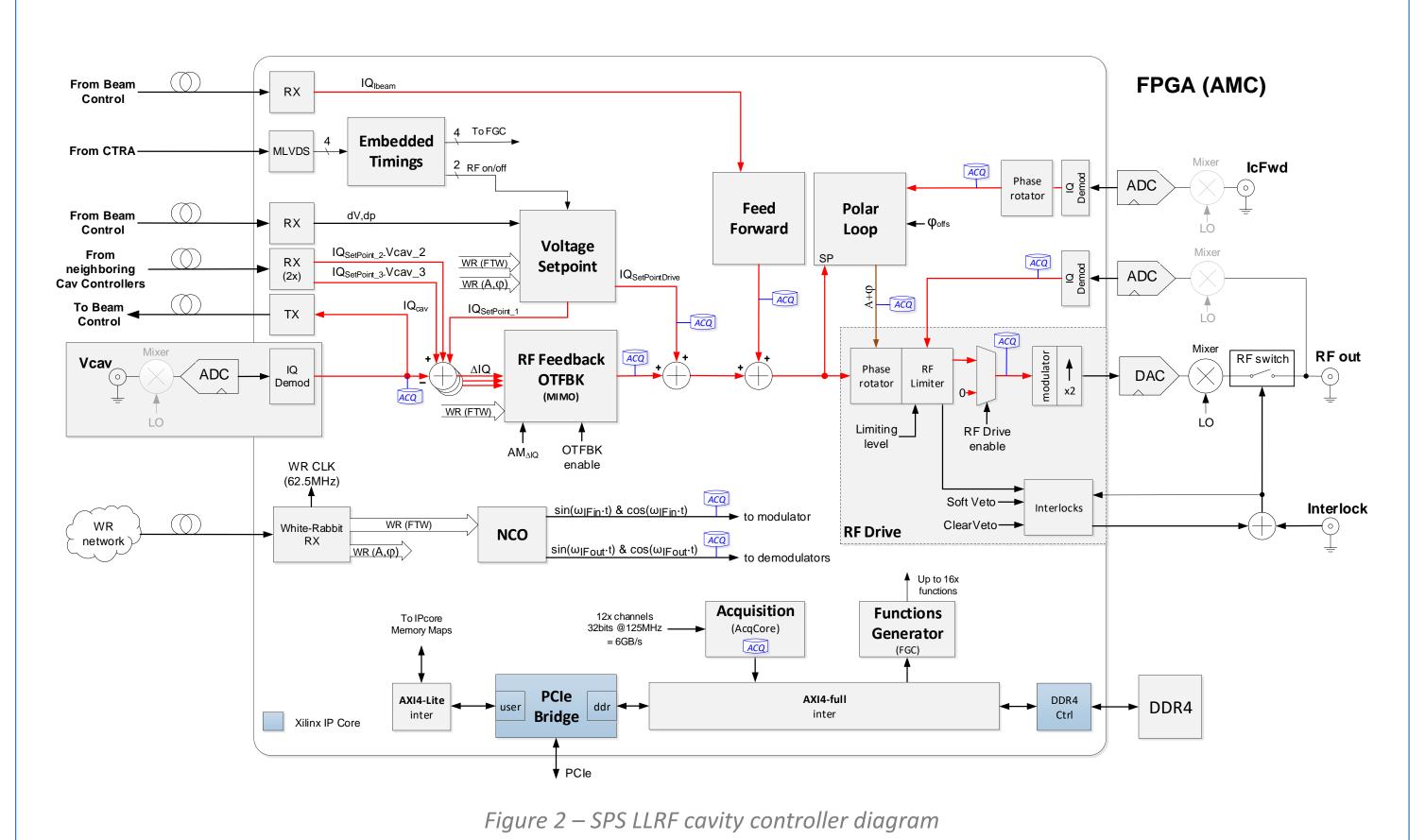

DRTM_DS8VM1
(DESY, Struck Innov. Sys GmbH)

SIS8300-KU
(DESY, Struck Innov. Sys GmbH)

eRTM : eRTM14+eRTM15
(CERN, OHWR, BE-CO-HT)

Figure 1 – SPS 200MHz Cavity controller

The architecture of the FPGA firmware is based on *Intellectual Property* (IP) cores approach. The usage of IP cores ease the way to add features to the firmware or use them for others projects, like the Beam control of the SPS. Furthermore, the *Advanced eXtensible Interface* (AXI) protocol is used to easily interconnect the IP cores together.

The firmware in the Kintex Ultrascale FPGA includes the following IP cores:
- The One Turn delay FeedBack (OTFB) compensating the transient beam loading
- The Numerically Controlled Oscillator (NCO) generating the reference revolution frequency keeping all cavities in synchronism during the acceleration ramp
- The Function Generator (FGC) for settings that vary during the ramp
- The Acquisition (acqCore) for built-in data observation and signal analysis
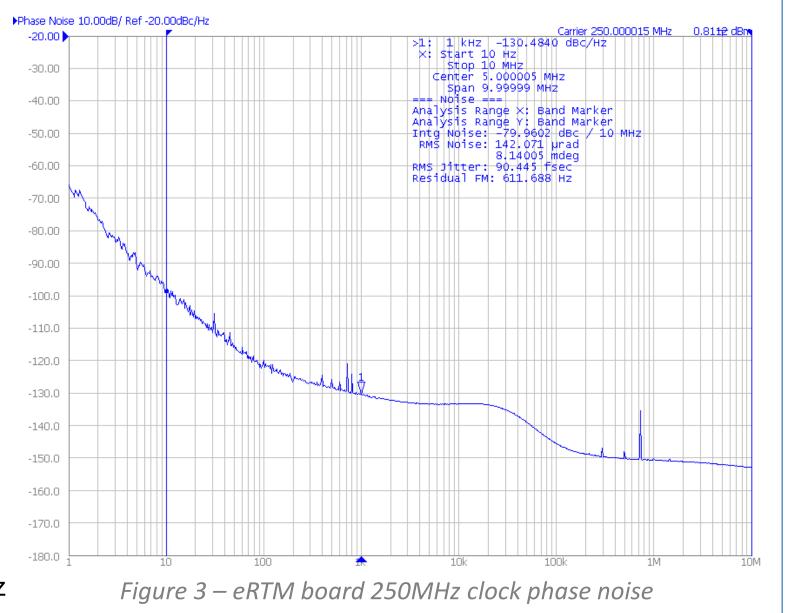- The PCIe Bridge for fast data transfer through MicroTCA backplane.

Figure 2 – SPS LLRF cavity controller diagram

eRTM – Clock distribution

The fixed-frequency sampling clock used in the new system is reconstructed from the White Rabbit on the custom eRTM board developed at CERN. This specific board was designed to reconstruct and distribute a local clock with low jitter and low phase noise to the rest of the boards through the so-called RF backplane of the MicroTCA standard.

The eRTM board must respect the stringent phase noise requirements imposed by the beam quality required for the HL-LHC:

125MHz clock phase noise: < -130dBc/Hz @ 1kHz

Figure 3 – eRTM board 250MHz clock phase noise

MicroTCA Backplane

During the SPS RF Upgrade, the new system is migrated on a MicroTCA platform. The six 200MHZ travelling wave cavities (TWC) of the SPS have their dedicated hardware. Each cavity has a Cavity controller board (SIS8300-KU AMC board) implementing the OTFB.
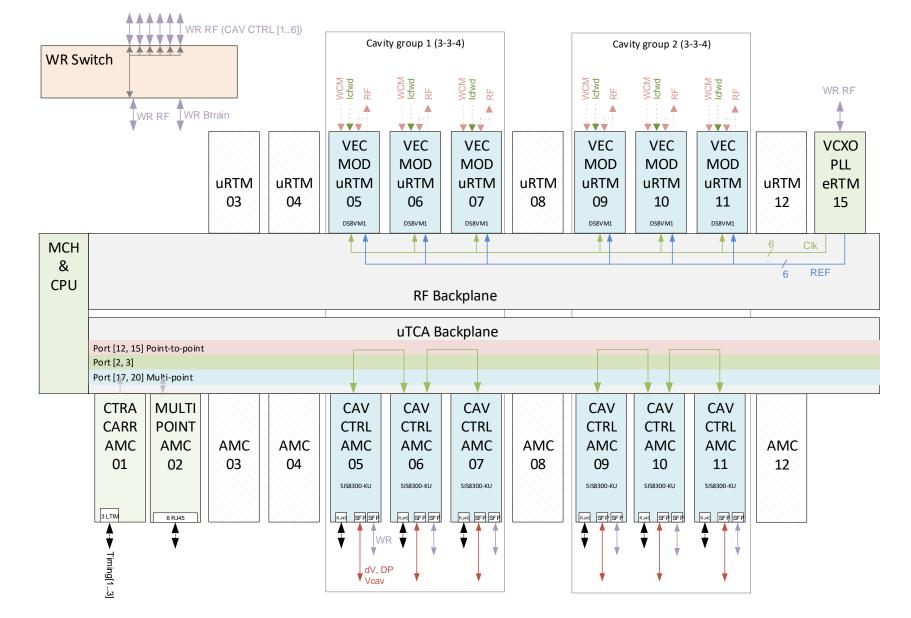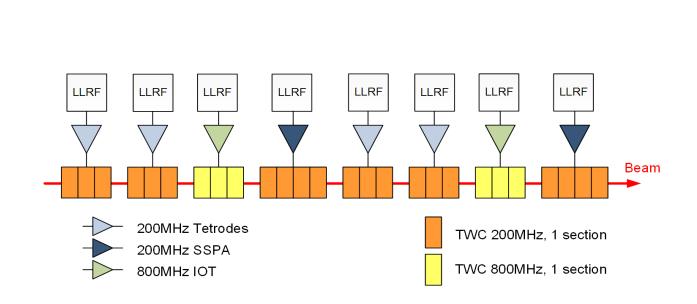

Figure 4 – TWC200 crate structure

For some frequencies, the accelerating voltage created by the power amplifier is zero while the voltage induced by the beam is non zero (Fig. 6). Therefore, the beam loading in the cavity cannot be compensated by its amplifier. As the 3 and 4 sections cavities have zeros at different frequencies, a cross-feedback can be used to overcome this problem: The 4-sections cavity would compensate for the beam induced voltage at the zero of the 3-sections cavity and vice versa. The Cavity controllers are split in two 3-3-4 sections group in the MicroTCA crate. Point-to-point GB serial links on the backplane will be used to exchange the feedback data required for this cross-feedback scheme. Figure 6 shows the layout of the Cavity Controllers in the MicroTCA crate (slots 5,6,7 and 9,10,11).

200MHz Tetrodes
200MHz SSPA
800MHz IOT
TWC 200MHz, 1 section
TWC 800MHz, 1 section

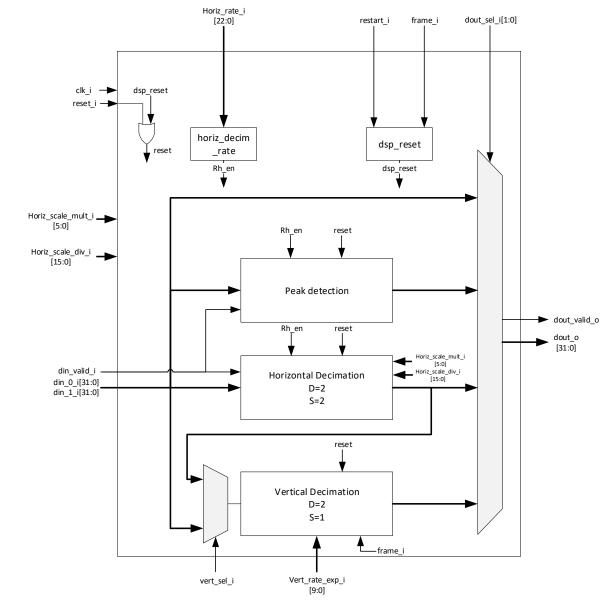*Figure 5 – the SPS acceleration system*

Figure 6 – 3 and 4 sections cavities. Ratio of accelerating voltage to generator current (top) and beam current (bottom)

Diagnostic tool

The SIS8300-KU AMC board provides a high-performance DDR4 memory (12.8GBps bandwidth). Combining this high-speed memory, an efficient AXI4-full scheme and the PCIe Gen 3.0 interface, this hardware allows for a powerful diagnostic tool.

The new FPGA firmware integrates the acqCore IP. This module provides up to twelve 32-bits acquisition channels and can reach a 500Msps acquisition rate simultaneously on all channels. This feature is essential for machine debugging and diagnostics. Moreover, this IP core has pre-processing features (acqDSP module):

- Peak detection: detect the minimum/maximum of a decimation period. This can be useful to detect voltage and power peak transients.
- Horizontal decimation: reduce the sampling rate using a CIC filter. Useful to monitor slow trends and drifts.
- Vertical decimation: turn-by-turn decimation for bunch-by-bunch diagnostics. This can be useful for tracking features such as the individual stable phase (monitoring of the e-cloud via power loss).
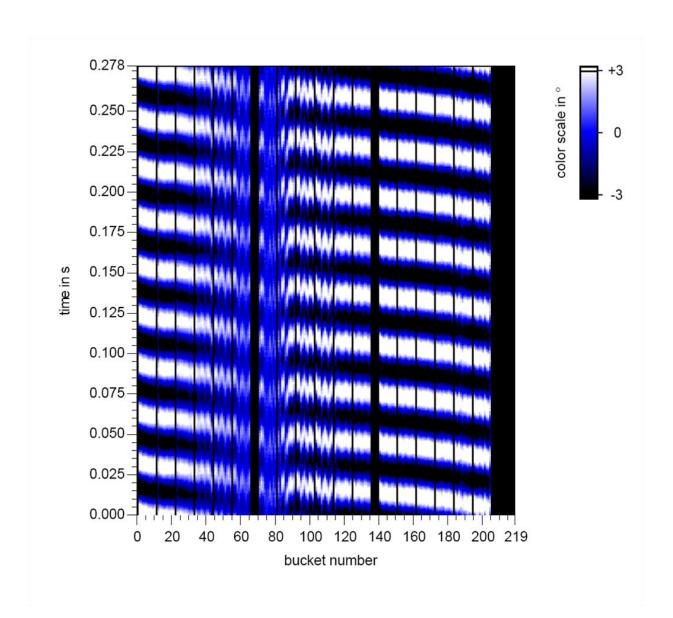

Figure 7 – acqDSP module in acqCore

Figure 8 – Measurement of the synchrotron oscillation bunch per bunch and turn-per-turn (courtesy of Hera).

To reach the system requirements, the AXI-full interconnection was optimized using a complete simulation of the architecture involving all IP cores accessing the DDR memory. The worst use-case was tested to validate DDR performances.

References
[1]   J. Coupard et al., "LHC Injector Upgrade - Technical Design Report - Vol. I: Protons", CERN-ACC-2014-0337 (CERN, Geneva, 2017)
[2] A. Spierer et al., "Upgrade of the SPS LLRF beam-based loops on the MicroTCA platform", Poster, LLRF2019, Chicago
[3] G. Hagmann et al., "The CERN SPS Low Level RF upgrade Project", in Proc. 10th Int. Particle Accelerator Conf. (IPAC'19), Melbourne, Australia, May 2019, pp. 4005-4008. doi:10.18429/JACoW-IPAC2019-THPRB082