Upgrade of the SPS LLRF beam-based loops on the MicroTCA platform

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SPS Upgrade LIU Project

SPS RF Upgrade as HL-LHC injector [1]

Beam performance requirements of the High Luminosity LHC (HL-LHC) project translate into a set of requirements for the SPS as injector.

- **Protons**: Doubling beam intensity (25ns bunch spacing, 2.3×10^{11} p+/bunch at extraction, 2.5×10^{11} p+/bunch injected, up to 4 batches of 72 bunches/batch)
- **Lead ions**: Slip-stacking for 50ns bunch spacing, low RF noise due to long injection plateau of ~39.6s (2.1×10^{8} ions/bunch extracted)

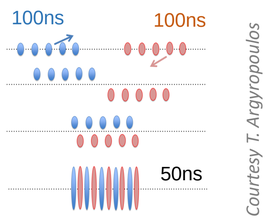

Figure 1 – Ions Slip-stacking

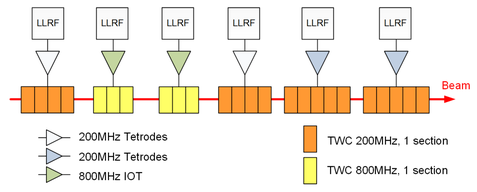

Figure 2 – SPS RF systems before LS2

- Main limitations come from:
  - Beam-loading at very high beam intensity for protons (V_{RF}=1MV, ~2MV beam induced)
  - Longitudinal instabilities linked to longitudinal impedance

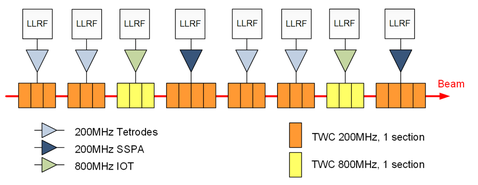

Figure 3 – SPS RF systems after LS2

The SPS LLRF is divided in 5 distinct modules [3]:

- ***Beam phase measurement*** (bunch per bunch) from resonant pick-up or wall current monitor
- ***Beam radial position measurement*** (bunch per bunch) from strip-line pick-up
- ***Cavity controller*** to regulate the cavity voltage and ***RF-Synchro*** to generate and distribute beam synchronous signals or triggers
- ***Beam control*** system which implements the beam-based loops (synchro, phase and radial loops) and generates the frequency program from the B-field.

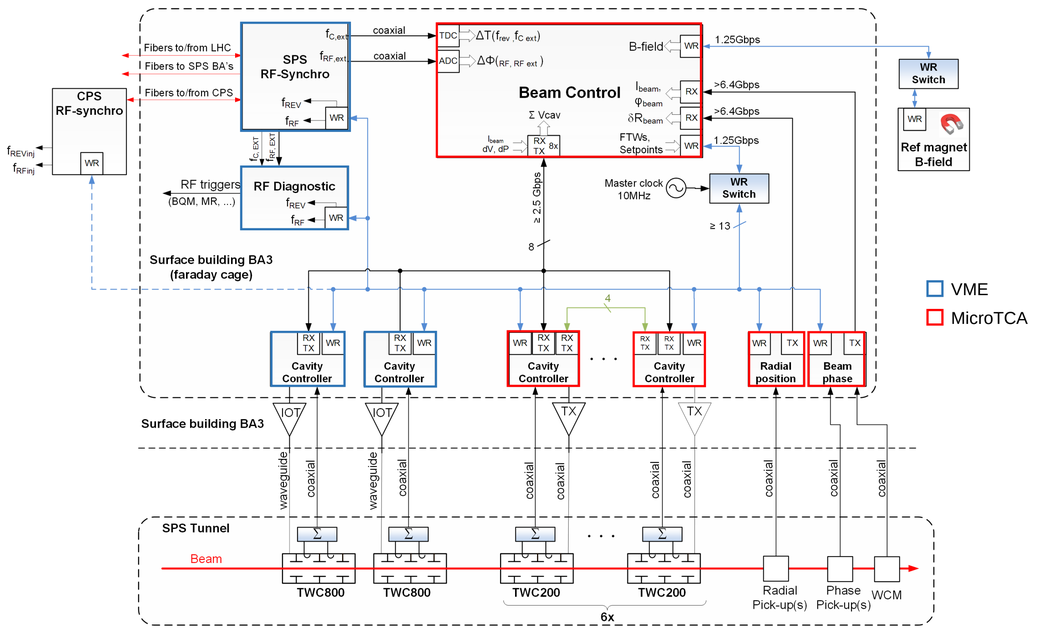

Figure 4 – SPS LLRF architecture

Beam control architecture

The Beam control receives bunch by bunch beam phase and radial position measurements over multi-gigabit serial links and processes one averaging per turn over the full beam or a region of interest. The control loops are applied using biquadratic filters implemented in the ARM CPU. The resulting Frequency Tuning Words (FTW) are sent at every turn over White Rabbit to the other devices on the network. During Ions Slip-Stacking two groups of three cavities can be controlled independently (RF frequency, phase and amplitude).

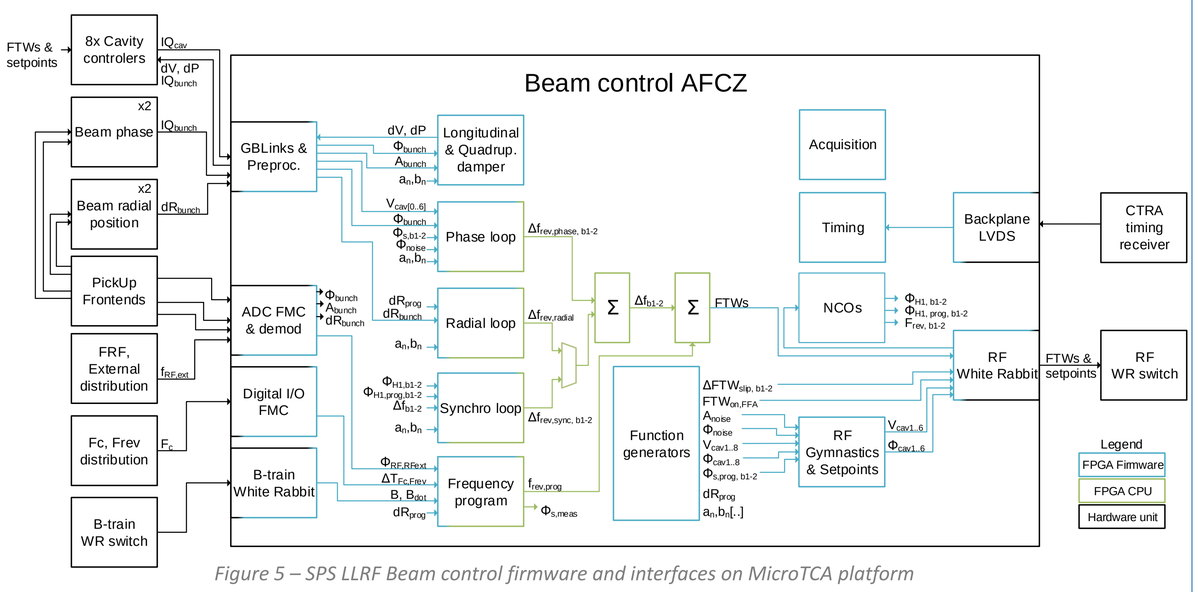

Figure 5 – SPS LLRF Beam control firmware and interfaces on MicroTCA platform

- The cavities RF amplitude and phase setpoints can be updated once per turn by the Beam control to perform precisely timed non-adiabatic manipulations such as bunch rotation and longitudinal blow-up.
- Two higher bandwidth loops (~5 MHz) are used to damp longitudinal oscillations (dipolar and quadrupolar) within the particle batches.
- Synchronization signal from the LHC and other target machines are sampled to align the beam longitudinally before extraction.

RF Synchronization over White Rabbit network

Every module is equipped with a White Rabbit [2] receiver which synchronizes the FPGA fixed clocks (Beam control, Cavity controllers, LO generators, …). A local NCO (Numerically Controlled Oscillator) is then used to generate the RF signals in the FPGA. Along with the clock synchronization, an *RF data frame* is sent at every machine turn with Frequency Tuning Words for the NCOs. We can set a fixed latency to the frame transmission so that each device receives and updates its frequency simultaneously with a clock cycle precision. To ensure a deterministic phase between all the devices at every machine cycle, we also send a NCO reset signal through the same RF frame. This method removes the need for analog distribution lines for RF and synchronization signals within the machine.

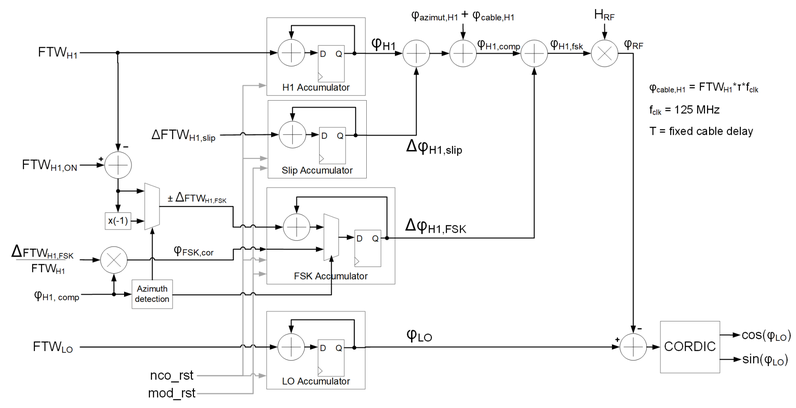

Figure 6 – NCO for up/down modulation in fixed frequency clock

- The NCO has additional functionalities such as modulation for fixed frequency acceleration and an accumulator dedicated to slip-stacking. It also includes a compensation of cable delay depending on frequency and an azimuthal position offset.
- By using the revolution frequency as a reference oscillator, all the nodes can retrieve the same revolution marker and use it for data synchronization and tagging.

Beam synchronous data flow

A custom *GBLink* protocol is used to transmit 200 Msps bunch synchronous or 125 Msps fixed sampling clock data with a fixed latency. Both the MicroTCA backplane links and SFP optical links are used as multi-gigabit serial lanes.

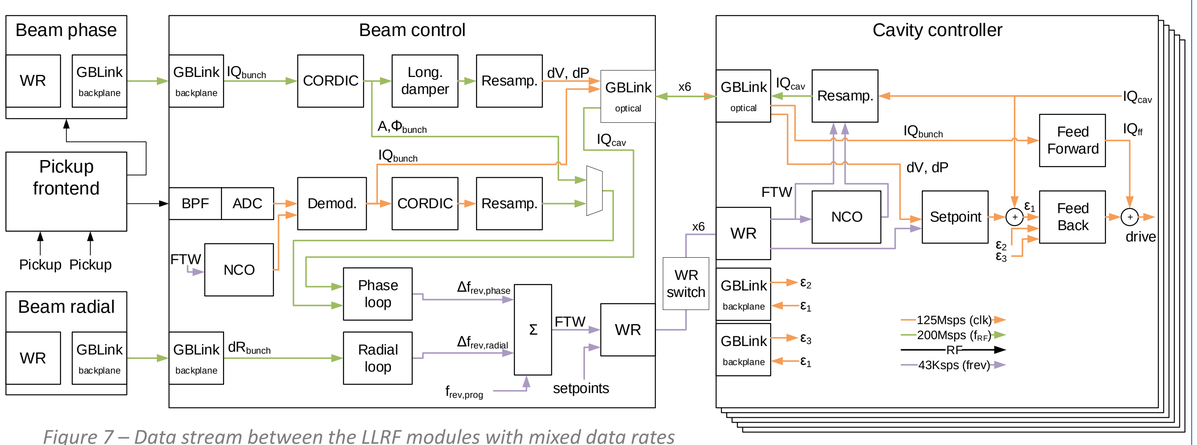

Figure 7 – Data stream between the LLRF modules with mixed data rates

- Bunch synchronous and clock synchronous data are compared using resamplers. The resamplers are disciplined by the NCO and the Frequency Tuning Words.

Beam control Hardware

The beam control is based on MicroTCA and open hardware modules (OHWR). The carrier (AFCZ) is equipped with a Zynq Ultrascale+ SoC FPGA and two White Rabbit receivers. The modular system allows to route the 16 FPGA gigabit transceivers towards the FMCs or the RTM.

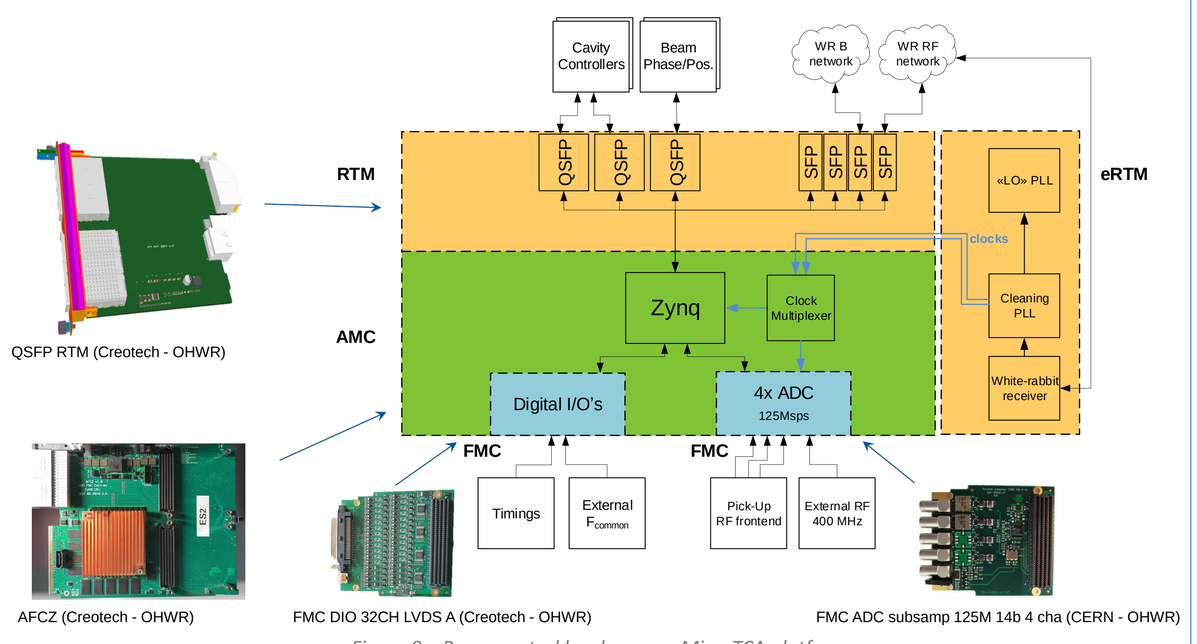

Figure 8 – Beam control hardware on MicroTCA platform

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