The CEBAF Third Generation LLRF system, LLRF 3.0

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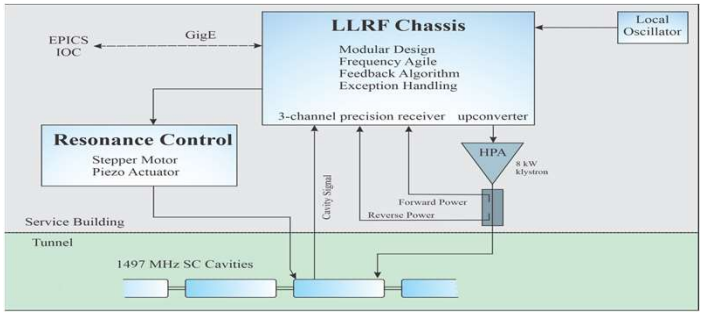
Abstract

The CEBAF accelerator is a 12 GeV recirculating electron linac consisting of approximately 500 SRF cavities. Each cavity is individually controlled by a single LLRF system. The facility has been operating since 1995, and presently three types of LLRF systems have been installed. The original analog system, a VME based digital LLRF system and a PC/104 based NAD (Network Attached Device) digital LLRF system. With the introduction of high loaded Q and high gradient cavities eight years ago, the LLRF team had to develop new control algorithms and hardware, including, at the time, an innovative digital Self Excited Loop. As CEBAF approaches 25 years in operation the older 320 cavity LLRF systems are becoming problematic to maintain and repair due to obsolesce of components. The decision was made to develop a new generation of LLRF system (LLRF 3.0) to begin "back populating" the older RF systems with new LLRF. The new design benefits from our recent collaboration and experience with the LCLSII LLRF program. The design follows the LCLSII design to a certain extent, but instead of having a dedicated cavity receiver chassis and separate transmitter chassis, we combine the two into one chassis, like the LCLSII RF station chassis. Given the accelerator requirements, specifications and existing footprint, the single LLRF chassis/cavity is a better fit for CEBAF. The chassis functionality is divided into four different boards, RF receiver, RF transmitter, Digitizer (ADC/DAC) and FPGA carrier card. The FPGA carrier retains the LCLSII feature by communicating with a local EPICS IOC using a User Datagram Protocol (UDP). This is an improvement over our existing digital LLRF system by eliminating the need for an IOC in the chassis (PC/104). In this poster we will discuss the architecture, design methodology/performance of RF receiver, RF transmitter, Digitizer and the communication between FPGA and EPICS.

ARCHITECTURE

1. One 8kW Klystron per cavity
2. One field control system per cavity
3. One ioc per 8 cavities (cryomodule)
4. Udp over Ethernet and EPICS

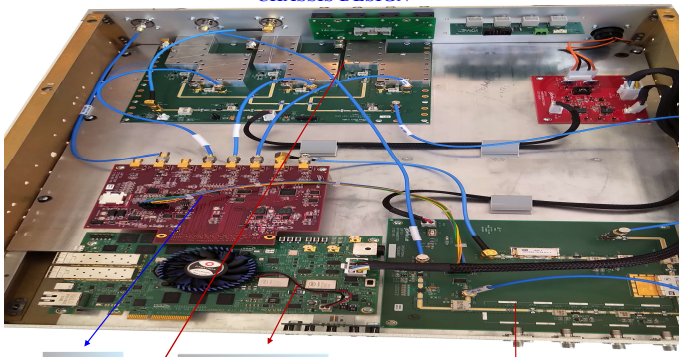


Single source, single cavity and single controller architecture

DESIGN PHILOSOPHY

Design philosophy of the chassis is modularity. Digitizer has ADC,DAC and the Clock circuitry. Upconverter and Downconverter have been designed as separate boards to increase isolation and decrease the crosstalk between Probe and Forward channels. An evaluation FPGA board (Cyclone 10 GX) is being used for testing with the prototype chassis. Once the FPGA design is complete and tested, it will be replaced. All the boards are mounted on a cooling plate for efficient heat dissipation

CHASSIS DESIGN

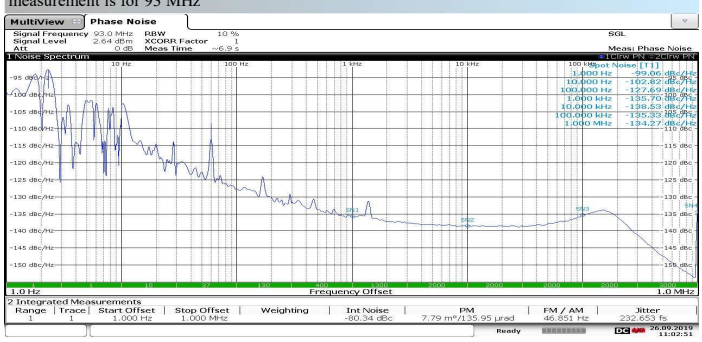


Downconverter has three receiver channels, down converting the 1497 MHz to 70 MHz using the1427 MHz LO, and these signals are fed to the Digitizer

Upconverter receives the 70 MHz IF signal from Digitizer, and generates 1497 MHz to drive the amplifier using 1427 MHz LO

CLOCK PERFORMANCE

jitter performance of LMK03328 225 fs for 93 MHz output and 230 fs for 186 MHz output .Shown measurement is for 93 MHz



Integrated phase noise of the ADC clock

DIGITIZER and SIGNAL PROCESSING

Clock chip on the Digitizer takes 70 MHz MO as input reference and generates the 93 MHz and 186 MHz sampling clocks needed for ADC and DAC respectively.

Digitzer receives the 70 MHz IF signals from the downconverter. These signals are sampled with 93 MHz using nonIQ sampling to generate I and Q components.

DAC generates the 70 MHz IF signal using 186 MHz sampling clock and the I and Q Information. This generated signal is fed to the upconverter

I and Q samples are generated using the following equation

$$\begin{pmatrix} I \\ Q \end{pmatrix} = \frac{1}{\sin\theta}\begin{pmatrix} \sin(n+1)\theta & -\sin n\theta \\ -\cos(n+1)\theta & \cos n\theta \end{pmatrix}\begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix}$$

Where y_n and y_{n+1} are two successive samples of the IF and θ is f_{if}/f_s *360. Sine and Cosine

LUT consists of 93 values for sampling 70 MHz with 93 MHz clock

DAC signal is generated from I and Q values using the equation

$$\begin{pmatrix} y_n \\ y_{n+1} \end{pmatrix} = \begin{pmatrix} \cos n\theta & \sin n\theta \\ \cos(n+1)\theta & \sin(n+1)\theta \end{pmatrix}\begin{pmatrix} I \\ Q \end{pmatrix}$$

Where y_n and y_{n+1} are the successive samples sent to the DAC and θ is is f_{if}/f_s *360. Sine and Cosine

LUT consists of 186 values for generating 70 MHz wutg 186 MHz sampling clock. Firmware development

For field control algorithm is in progress. It will be based on the existing implementation and also from

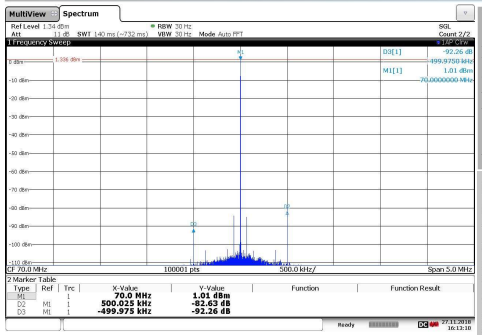
LCLS-II implementation

Digitizer ADC Linearity

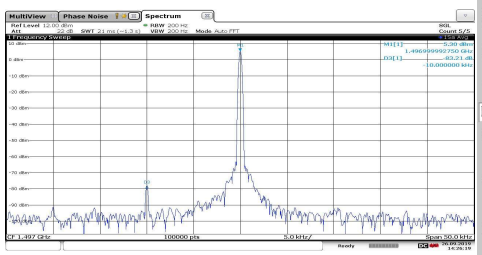
Power	M(Expected)	I	Q	M(measured)	Error %	dB
6 dBm	116322	7654	-116076	116328.077	0.005224	5.929947
0 dBm	58776	-9330	-58029	58774.26087	-0.00296	6.199784
-6 dBm	28788	-5651	-28227	28787.10354	-0.00311	6.01504
-12 dBm	14403	-3328	-14013	14402.76894	-0.0016	6.022317
-18 dBm	7206	-549	-7179	7199.96125	-0.08387	6.007013
-24 dBm	3610	-412	-3582	3605.616175	-0.12158	5.98228
-30 dBm	1810	-280	-1789	1810.779114	0.043026	6.010346
-36 dBm	913	-182	-888	906.4590449	-0.72159	

ISOLATION MEASUREMENTS

Preliminary isolation measurements when two channels are driven. ~84 dB. Probe has 1497 MHz 0 dBm, Forward has 1496.99 MHz 0 dBm and the Probe output is sent to the DAC and then upconverted. This shows isolation of the whole system. 1497 MHz input on the receiver channels to 1497 MHz output on the amplifier drive. Isolation measurements on the downconverter board are also shown here. These values are 83 dB and 92 dB when all three channels are driven



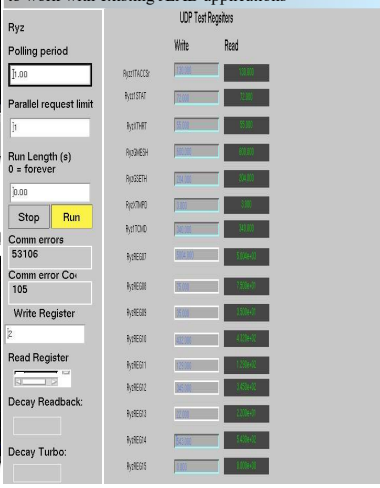
Isolation measured on the downconverter



S21 measurement, Isolation measured from input to output

UDP and EPICS

Basic EPICS screens are under development. This application polls and scans all the registers and writes to the registers only by request. This is based on Verilog code from Berkeley and the UDP driver from SLAC. We are making modifications to these drivers to work with existing JLAB applications



References

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2. The LCLS-II LLRF System. C.Hovater et al, IPAC2015, Richmond VA USA