Development of a Zynq-based Laser Timing System for LEReC

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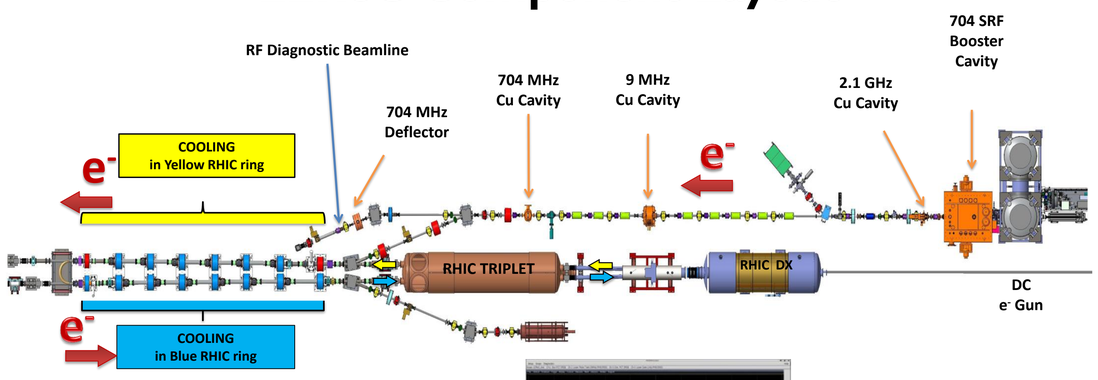
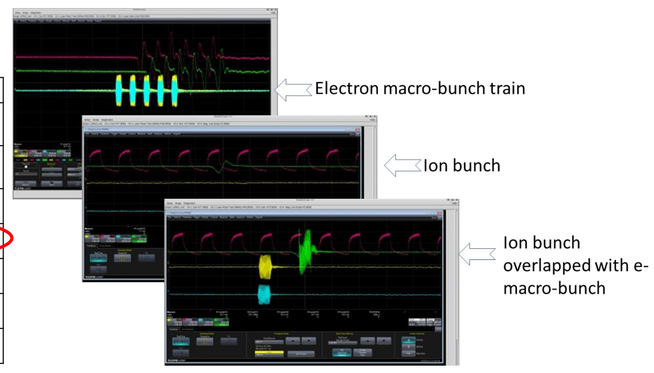
The Low Energy RHIC electron Cooler (LEReC) is presently being commissioned at BNL to improve the luminosity of the Relativistic Heavy Ion Collider (RHIC) at low energies. LEReC is the first RF linac-based electron cooler with bunched beam cooling. To support LEReC beam operation with different energies and bunch patterns, a Xilinx ZC706 Zynq evaluation board is configured to function as a daughter card to a LLRF Controller. The LLRF Controller platform is based on a Xilinx Virtex5 FPGA and consists of a Carrier Board for Control system interface and a Daughter DAC module to provide RF synchronous reference and triggers. The 'Update Link' provides a deterministic 2 Gb/s serial link distributing encoded timing and data for system integration and synchronization. A custom FMC daughtercard provides the interface between the ZC706 and the LLRF Controller, as well as the hardware interface to the laser system. The Xilinx Aurora protocol is used for the high-speed signal transfer with multi-gigabit serial I/O.

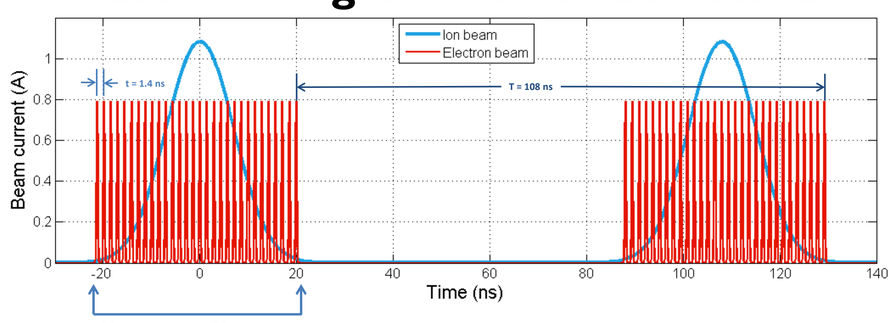
LEReC Component Layout



LEReC Laser Requirements	
Transverse profile	Truncated Gaussian (3mm sigma)
Longitudinal profile	Stacking with < 40% peak-to-peak modulation
Pulse length after stacking, ps	40-80
Time jitter rms, ps	< 1
Intensity rms, shot-to-shot, %	< 2
Spatial stability C.O.M. on iris rms, um	50 (<10um on cathode)
Extinction ratio (power leakage, pulsed mode)	10^6:1

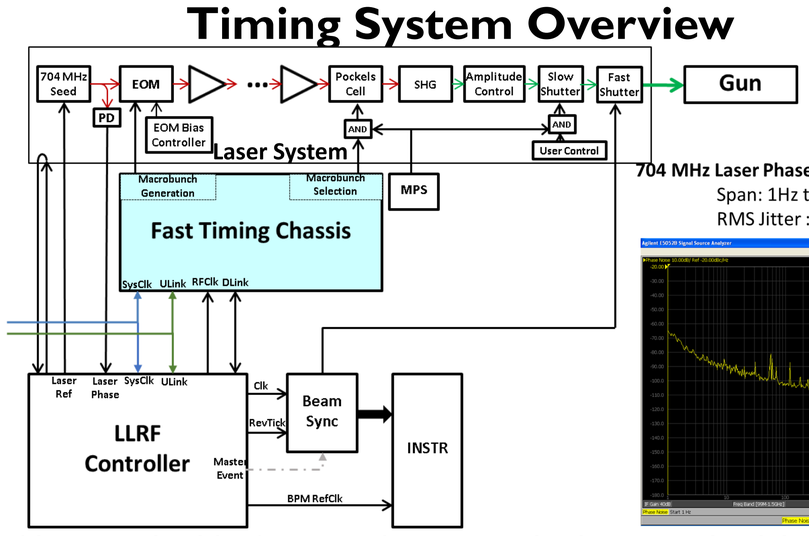


Laser Timing and Bunch Structure

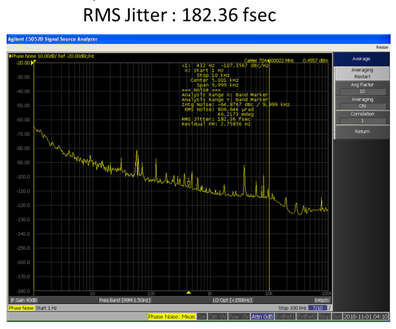


- Electron bunches are generated in the DC gun with a repetition rate of 704MHz. Macro-bunches (consisting of ~30 bunches) repeat at the 9 MHz ion bunching frequency. These frequencies are both harmonics of the RHIC ion revolution frequency, but the 704 MHz harmonic is not an integer multiple of the 9 MHz harmonic.
- A Mach-Zehnder electro-optical modulator (EOM) creates the macro-bunch structure on the drive laser. This EOM is driven with new hardware that consists of a Xilinx Zynq evaluation board with a custom FMC daughtercard and Picosecond Pulse Labs driver amplifier. The transmitter section of a Zynq GTX gigabit transceiver is used to generate a serial data stream which corresponds to the on-off pattern of the laser.
- Modes of Beam Operation:
  - 1 Hz
  - CW (Continuous train of 9 MHz macro-bunches)
  - 76 kHz (1 to 6 macro-bunches, repeated at Revolution Frequency)

Timing System Overview

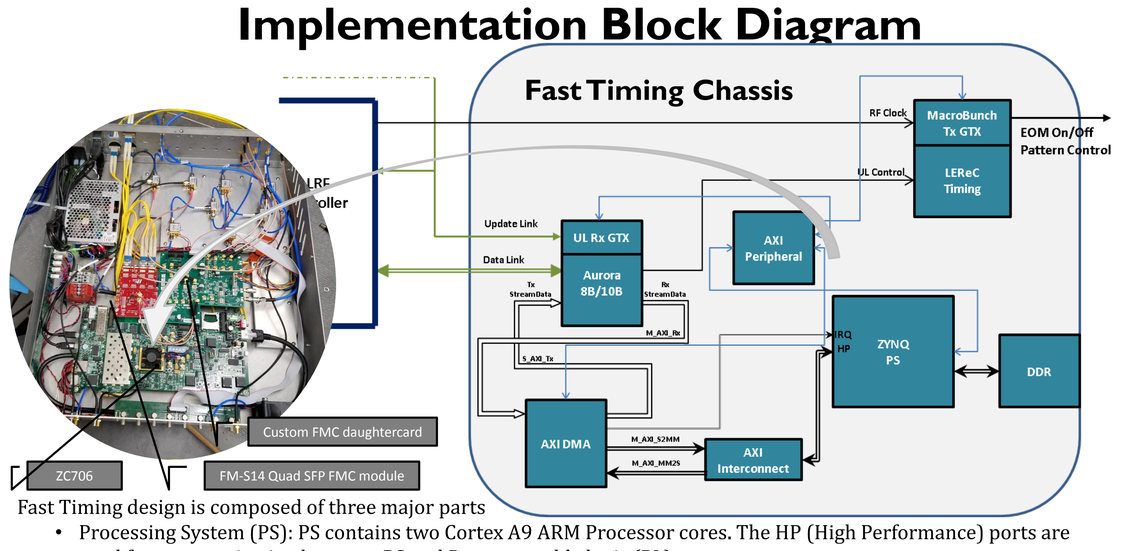


704 MHz Laser Phase from Photodiode before EOM
Span: 1Hz to 10 kHz
RMS Jitter : 182.36 fsec



- EOM (Electro-Optical Modulator) : Generates the 9 MHz macro-bunch structure and needs fast control synchronized with 704 MHz laser oscillator
- PSPL5865 Driver: Generates the control voltage for the EOM with fast response. Amplitude and bias is controlled to optimize EOM On/Off contrast
- Pockels Cell: Generates the gated macro-bunch train

Implementation Block Diagram

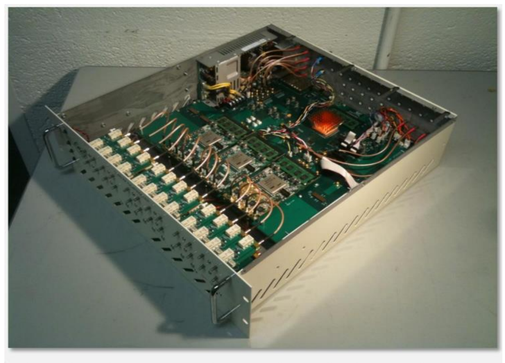


Fast Timing design is composed of three major parts

- Processing System (PS): PS contains two Cortex A9 ARM Processor cores. The HP (High Performance) ports are used for communication between PS and Programmable logic (PL).
- Interconnects: AXI Interconnect and AXI Peripheral take care of the data transmission between PS and PL.
- Programmable Logic (PL): Aurora channel partner to pass data across the DataLink with 8B/10B protocol using the high-speed serial transceivers. AXI DMA engine to transfer data between Aurora IP and DDR memory with AXI_MM2S and AXI_S2MM AXI4-streaming buses. LEReC timing IP for RF clock synchronous pattern generation.

LLRF Controller

- LLRF Controller is a stand-alone configurable, modular, hardware / software platform
  - Carrier Board: Control system interface, daughter host platform, communication hub, timing, data acquisition management, power monitor.
  - Daughter Module: Provide system specific functionality (ADCs, DACs, DSP, Motor Controller).
- 'Update Link'
  - Downstream deterministic (i.e. fixed latency) 2 Gb/s serial link distributing encoded timing and data.
  - Key to ease of system integration, flexibility, scaling and synchronization.
- Clocking/Sampling
  - RF asynchronous fixed-frequency is used as the primary system clock and signal processing.
  - RF synchronous clocking used for specific applications (e.g. trigger generation for e-gun lasers).


Platform Chassis showing Carrier Board, 2 DAC Daughter Boards and 1 ADC Daughter Board.

Design Parameters

	Electron KE (MeV)	Ion Total Energy (GeV/n)	RHIC Ions f_rev(Hz)	RHIC Ion bunch Freq(Hz) h_120	LEReC e-bunch harmonic h_704	Ratio of e-/Ion h_704/120	LEReC e-bunch Freq (Hz)
Au inj		9.7960	77842.23	9.341E+6	9044	75.37	7.04E+08
	1.600	3.8467	75870.80	9.104E+6	9279	77.33	7.04E+08
	2.003	4.5810	76563.91	9.188E+6	9195	76.63	7.04E+08
	2.651	5.7610	77168.16	9.260E+6	9123	76.03	7.04E+08
	2.600	5.6692	77134.34	9.256E+6	9127	76.06	7.04E+08

- For cooling, the electron bunch repetition rate must be a harmonic of the RHIC revolution frequency. The macro-bunch repetition rate must match the RHIC bunch spacing. It is also limited by the tuning range of the laser and RF cavities. Therefore a fixed Laser reference frequency is adopted.
- Each off time must be an integer number of periods of the laser oscillator (i.e. the control signal needs to be synchronous with the oscillator frequency). Duty cycle variation from pulse to pulse complicates the logic of the timing controller.
- A Xilinx ZC706 Zynq evaluation board is configured to function as a daughter card to LLRF Controller. It is located near the Laser system and is connected to a remote LLRF controller through high-speed fiber link.
- A multi-gigabit transceiver (GTX) in ZC706 generates the EOM gate signal. GTX has a PLL that generates a serial bit clock synchronous with the RF clock. Logic runs on a subharmonic, and loads the pattern piece-wise into the GTX output shift register. Frequency is locked to RF and phase can be adjusted by shifting the reference clock.

Conclusion

- RF reference signal to Laser meets LEReC Laser requirement specification for RMS jitter < 1ps.
- Beam commissioning with different modes of operation and bunch patterns was completed.
- Design and evaluation of the Xilinx Virtex5 Master- Zynq Daughter platform system provides an upgrade strategy for the future when next generation LLRF controllers are deployed.

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