Waveform Feature Implementation for FRIB LLRF Controllers

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	Introduction						Memory Controller Interface
The low level radio			Tab	ole 1: FRIB Ca		pes	 Native port interface (NPI) Notice port interface (NPI)
(LLRF) controller f project is designed		System	Area	Frequency (MHz)	Туре	Tuner	Write fast data into memory p0_wr_count[6:0] p0_wr_full p0_wr_data[31:0] 000000,00(255418 AE82E,D5 (62F5AEC5))
accommodate var		MHB F1	FE	40.25	RT	N/A	• Advanced extensible interface (AXI)
		MHB F2	FE	80.5	RT	N/A	to asserting write enable.
and tuner types (S	ee lable 1).	MHB F3	FE	120.75	RT	N/A	Read/Write data in software on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data written into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where write enable present. Data writen into FIFO on positive edge of wr_clk where writen into
		RFQ	FE	80.5	RT	temperature	Figure 4-8: Loading the Write Data FIFO
RF Board		MEBT	FE	80.5	RT	2-phase stepper	Memory chip 1: 830ns 840ns 850ns 860ns 870ns
 Direct sampling Under sampling 	•	QWR	LS1 FS1	80.5	SC	2-phase stepper	 Single 32-bit bi-directional AXI port For running Microblaze software

- Under sampling (38.99 MHz) • Non-IQ sampling (31 points)
- Direct synthesis: use band pass filters to pickup fundamental or higher harmonics
- Three variants: supports two frequencies per variant
- Spare analog/digital I/Os: 4 AI, 4 AO, 5 DI and 5 DO

Tuner Board

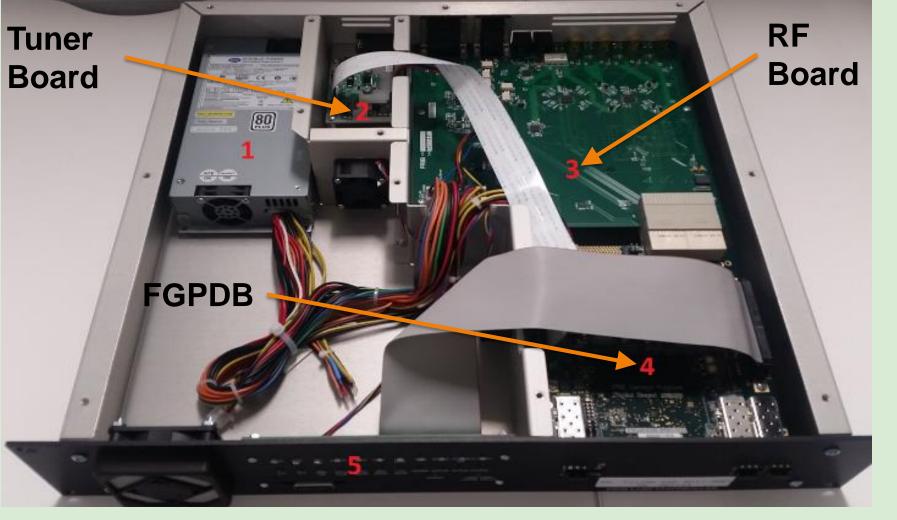
• Stepper Tuner: 2-phase with micro-stepping; RS-485 interface to 5-phase driver.

Analog Tuner: pneumatic valves for HWR; error signal to RFQ.

FRIB General Purpose Digital Board (FGPDB)

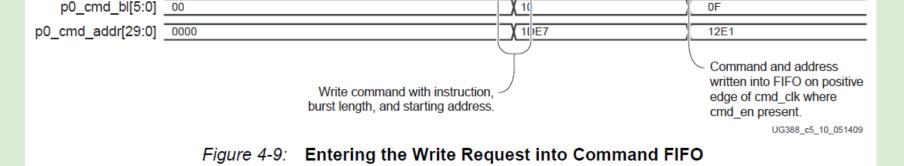
- A common digital front-end intended to support multiple systems:
- Low Level Radio Frequency (LLRF, Qty: 372)
- Machine Protection System (MPS, Qty: 80)
- Beam Position Monitor (BPM, Qty: 120)
- Xilinx Spartan-6 XC6SLX150T-FGG900 FPGA, dual 256 MB DDR memory,

MGB	FS1	161	RT	5-phase stepper
HWR	LS2/3 FS2	322	SC	pneumatic



Memory chip 2:

- One 32-bit NPI bi-directional port For writing fast data
- One 32-bit AXI bi-directional port Read only in practice
- Dedicate to circular buffer



JG388_c5_09_05140

Data can be copied through software from chip 1 to chip 2 while the circular buffer is still running to fulfil the second use case.

Data Organization

Data structure:

- 16 32-bit registers per sample
- 64 bytes block size
- 4 M samples (256 MB / 64 B)
- ~ 3.3 seconds (2²² / 1.25 MHz)

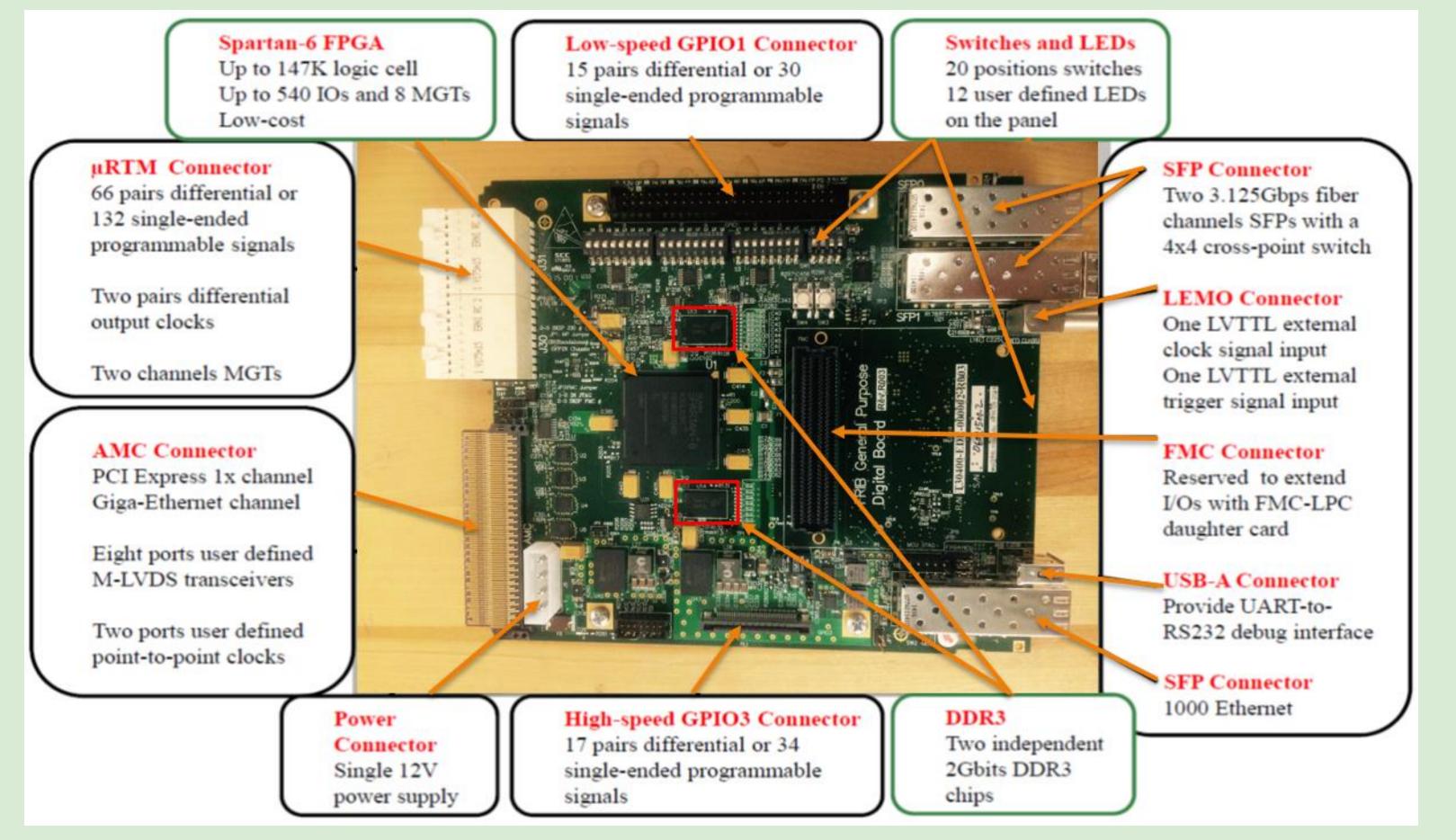
Pointers:

- *pStart* marks the starting address
- *pCurrent* tracks current sample address
- *pTrig* marks the trigger point

Flag:

																		-				
Address	0	1	2	3	4	5	6	7	8	9	А	в	с	D	E	F	Sample	flagFull				
(Hex)	-	inter Ch		, i a h	T1.						A			E.u.d.						Waveform Variab		_
00000000	- 1	ime St		<u> </u>			Stamp				Ampl				Phase		-		Ľ		le	_
00000010			Ampl				v Phase v Phase	-			Ampl		DI	nase S	hase		0			Fwd Ampl Fwd Phase		
			Ampl		l m				A	mpl S		nt	PI			nι						
00000030	-		r Erro				ock Sta				: bits				rved					Rev Ampl		
00000040	- 1	ime St		~	Tir		Stamp				Ampl			Fwd			-			Rev Phase		
00000050			Ampl				v Phase				Ampl				hase		1			Cav Ampl		
00000060			Ampl				v Phase		A	mpl S		nt	Pł	hase S		int	-			Cav Phase		
0000070			r Erro				ock Sta				: bits				rved					Drv Ampl		
00000080	Т	ime St		-	Tir		Stamp				Ampl			Fwd I			_	pStart		Drv Phase		
00000090			Ampl				v Phase	-			Ampl				hase		2	(oldest data, if		Ampl Setpoint		
000000A0			Ampl				v Phase		A	mpl S		int	Pł	nase S		int		flagFull is not		Phase Setpoint		
00000B0			r Erro				ock Sta			Miso	c bits			rese				set)		Tuner Error		
000000C0	T	ime St	amp ł	nigh	Tir	me S	Stamp	ow		Fwd	Ampl			Fwd	Phase					Interlock Status		
00000D0		Rev	Ampl			Re	v Phase			Cav	Ampl			Cav F	hase		3			Misc bits		
00000E0		Drv	Ampl			Dr	v Phase		A	mpl S	etpoi	int	Pł	nase S	ietpoi	int	5			reserved		
00000F0		Tune	r Erro	r	In	terl	ock Sta	tus		Miso	c bits			rese	rved							
00000100	Т	ime St	amp ł	nigh	Tir	me S	Stamp	ow		Fwd	Ampl			Fwd I	Phase					Waveform Exar	nple	S
00000110		Rev	Ampl			Re	v Phase	2		Cav	Ampl			Cav F	hase			pTrig		Time Stamp hi	gh 0	
00000120		Drv	Ampl			Dr	v Phase	:	A	mpl S	etpoi	int	Pł	nase S	ietpoi	int	4	(trigger point)		Time Stamp lo	0 w	
00000130		Tune	r Erro	r	In	terl	ock Sta	tus		Mise	bits			rese	rved					Fwd Ampl (D	
00000140	Т	ime St	amp ł	nigh	Tir	me :	Stamp	low		Fwd	Ampl			Fwd I	Phase					Fwd Ampl 1	1	
00000150		Rev	Ampl			Rev	v Phase	2		Cav	Ampl			Cav F	hase		_			Fwd Ampl 2	2	
00000160		Drv	Ampl			Dry	v Phase		A	mpl S	etpoi	int	Pł	nase S	etpoi	int	5			Fwd Ampl 3	3	_
00000170		Tune	r Erro	r	In	terl	ock Sta	tus		Mise	bits			rese	rved					Fwd Ampl 4	4	_
00000180	Т	ime St	amp ł	nigh	Tir	me :	Stamp	ow		Fwd	Ampl			Fwd I	Phase					Fwd Ampl 5	5	
00000190		Rev	Ampl	Ŭ			v Phase			Cav	Ampl			Cav F	hase			pCurrent				_
000001A0		Drv	Ampl			Dr	v Phase		A	mpl S	etpoi	int	Pł	nase S	ietpoi	int	6	(newest data)		Fwd Ampl 25	50	_
000001B0		Tune	r Erro	r	In	terl	ock Sta	tus		Misc	bits			rese	rved					Fwd Ampl 25	51	_
000001C0	Т	ime St	amp h	nigh	Tir	me :	Stamp	ow			Ampl				Phase					Fwd Ampl 25		
000001D0			Ampl	<u> </u>			v Phase				Ampl				hase		_	(oldest data, if		Fwd Ampl 25		
000001E0			Ampl				v Phase		А	mpl S			Pł	nase S		int	7	flagFull is set)		Fwd Ampl 25		
000001F0			r Erro		In		ock Sta				bits			rese						Fwd Ampl 25		
																					_	
																	· ·			Time Stamp bi	σh 5	

16 MB flash, MicroTCA compatible



Waveform Requirements

• Save important internal data (e.g. the amplitude and phase information of forward/reverse/cavity signals, interlock status, etc.)

- *flagFull* will be set once the circular buffer is filled;
- *flagFull* resets when buffer starts running for the next time.

					•	Time Stamp low 5
					•	Cav Phase 5
	Time Stamp high	Time Stamp low	Fwd Ampl	Fwd Phase		Cav Phase 8
	Rev Ampl	Rev Phase	Cav Ampl	Cav Phase	N	Cav Phase 11
	Drv Ampl	Drv Phase	Ampl Setpoint	Phase Setpoint		Cav Phase 14
	Tuner Error	Interlock Status	Misc bits	reserved		Cav Phase 17
						Cav Phase 20
					•	
					•	Cav Phase 755 (5+250*3
					•	Cav Phase 758 (5+251*3
0FFFFFC0	Time Stamp high	Time Stamp low	Fwd Ampl	Fwd Phase		Cav Phase 761 (5+252*3
0FFFFFD0	Rev Ampl	Rev Phase	Cav Ampl	Cav Phase	End	Cav Phase 764 (5+253*3
OFFFFFEO	Drv Ampl	Drv Phase	Ampl Setpoint	Phase Setpoint	Ena	Cav Phase 767 (5+254*3
OFFFFF	Tuner Error	Interlock Status	Misc bits	reserved		Cav Phase 770 (5+255*3

Trigger position is a user settable parameter that determines how many more samples to acquire after the trigger condition is met before circular buffer freezes.

Data Retrieving

For the first use case, the circular buffer is already frozen when user tries to retrieve the data. So the time is not a concern.

- Whole memory dump
- Selective read
 - Similar to second use case

For the second use case, the circular buffer is still running. So how to read the data out before it is over written needs to be addressed.

Commands:

Request Waveform Data

REQ_WF_DATA Cmd Request						
Offset (Byte)	Length (Byte)	Field	Definition			
0	4	Packet ID	> = 1 (incremented for each packet sent)			
4	4	Command	8			
8	4	Length	Total number of samples required. Must match Waveform NELM field			
12	4	Decimation Factor	Number of samples to be read. DF=1 (all data read), DF=2 (one out of two)			

REQ_WF_DATA Cmd Response

Offset (Byte)	Length (Byte)	Field	Definition
0	4	Packet ID	> = 1 (incremented for each packet sent)
4	4	Command	8
8	2	Session ID	The session ID assigned to the connection by the IOC
10	2	Status	Status 0 if success; !=0 if error (see LCP status codes)
12	4	Length	Total number of samples available to be read
16	4	Decimation Factor	Number of samples to be read. DF=1 (all data read), DF=2 (one out of two)
20	4	Sequence Number	Sequence Number of the package requested. Increased by 1 on each request

READ_WAVE	ORM Cmd Re	equest	
Offset (Byte)	Length (Byte)	Field	Det

et e)	Length (Byte)	Field	Definition
	4	Packet ID	> = 1 (incremented for each packet sent)
	4	Command	3
	4	Waveform ID	ID of the waveform to be read
	4	Offset	First value to be read from the waveform. Increased on each read by Count to read total length
	4	Count	The number of values to return from the waveform on each read

- Holds at least one second of fast data at the RF feedback control loop rate (~1.25 MHz, 80.5 MHz / 64)
- Freeze buffer when MPS triggers or internal interlock detected
- Flexibility

Use cases:

- Freeze the circular buffer when an interlock event happens and read out the fast data to diagnose the problem
- Monitor one or a set of signals at a decimated rate (user settable) while the circular buffer is still running

- > Length (8 K max)
- > Decimation Factor
- Base on the user's choice, fast data will be copied from circular buffer to waveform buffer (512 KB max) in Microblaze memory space.
- Read Waveform
- \succ Waveform ID (1 ~ 14) > Offset (in waveform buffer)
- > Count (256 max, limited by MTU)

Offset (Byte)	Length (Byte)	Field	Definition
0	4	Packet ID	> = 1 (incremented for each packet sent)
4	4	Command	3
8	2	Session ID	The session ID assigned to the connection by the IOC
10	2	Status	Status 0 if success; !=0 if error (see LCP status codes)
12	4	Waveform ID	ID of the waveform actually read from (0xFFFFFFFF if req ID invalid)
16	4	Offset	The offset of the first value actually returned (0xFFFFFFFF if none)
20	4	Count	The number n of values returned (0 if none)
24	4	Sequence Number	Sequence Number of the package this data belongs to.
28	8	TimeStamp	Value from GTS (0 if no data returned) of first value acquired [63:32]-Date/Time part of the timestamp [31:0]-Sub-second part of the timestamp
36	4*n	Waveform Values	n 32-bit values from the requested waveform



Facility for Rare Isotope Beams

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