Fermilab PIP-II Era Booster LLRF Upgrade

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LLRF 2019 Workshop

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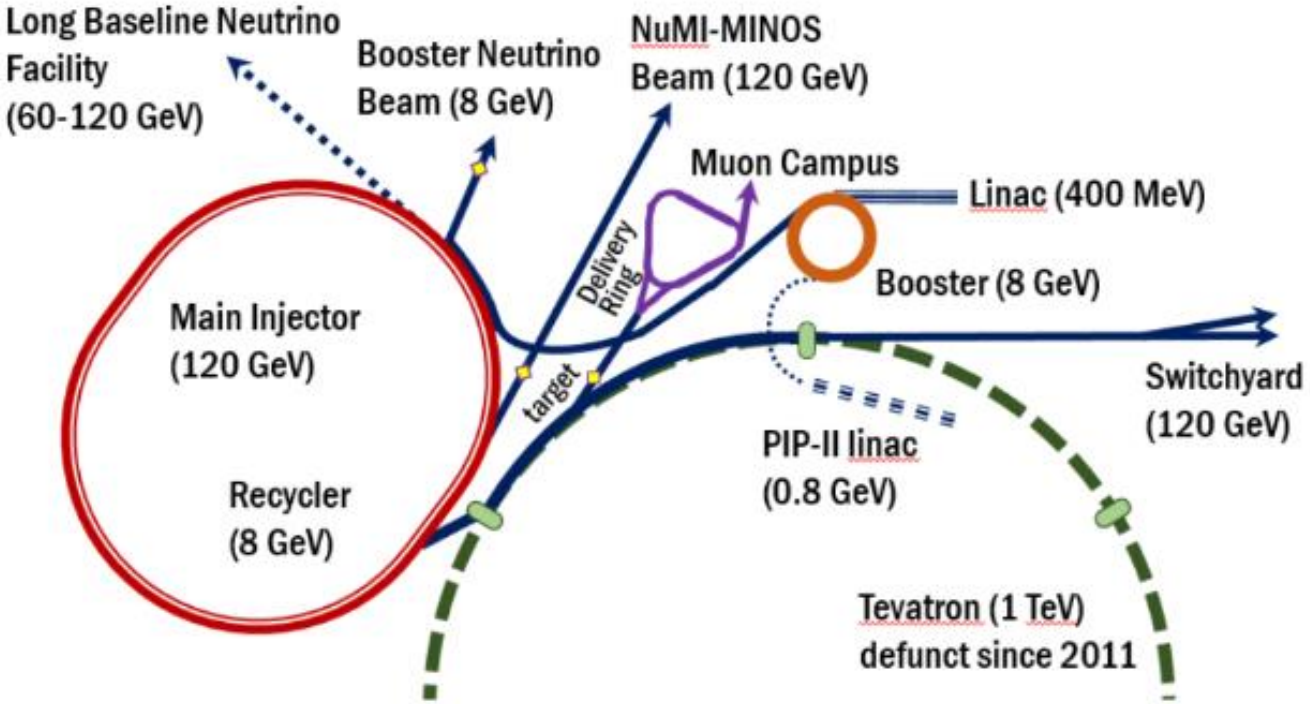
Fermilab PIP-II

Planned PIP-II 800 MeV Linac to replace the current 400 MeV Linac

Fermilab Booster



Fermilab Accelerator Complex

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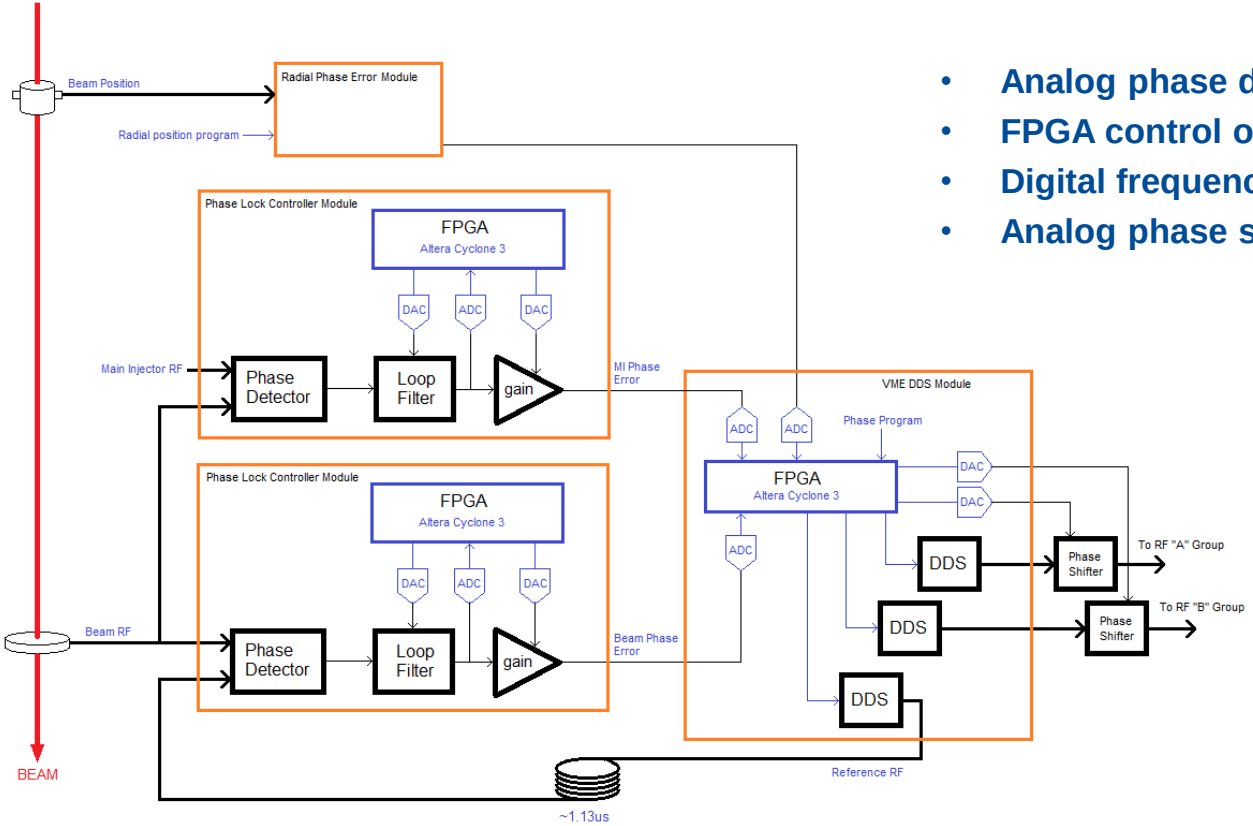
Fermilab Booster PIP-II Requirements

Performance Parameter	Present	PIP II Requirement	Units
Input (H^{-}) Beam Energy (Kinetic)	400	800	MeV
Output Beam Energy (Kinetic)	8.0	8.0	GeV
Protons per Pulse (injected)	5.0×10^{12}	7.0×10^{12}	
Protons per Pulse (extracted)	4.75×10^{12}	6.4×10^{12}	
Beam Pulse Repetition Rate	15	20	Hz
RF Frequency (injection)	37.9	44.7	MHz
RF Frequency (extraction)	52.8	52.8	MHz
Injection Time	.04	0.6	msec
Injection Turns	18	315	Turns
Beam Emittance (6σ, normalized; $\varepsilon_x=\varepsilon_y$)	<18	<18	π mm-mrad
RF Volts (Max)	1100	1200	V
Delivered Longitudinal Emittance (97%)	.08	0.08	eV-sec
Booster RF Stations	22	22	Count (A&B)

LLRF System must be capable of the following:

- Rep rate increased from 15 Hz to 20 Hz.
- Injection time lengthened from 40 us to 600 us.
- RF frequency sweep changed from 37.9-52.8 MHz to 44.7-52.8 MHz.

Current Booster LLRF System



- Analog phase detectors and feedback gain
- FPGA control of analog feedback
- Digital frequency control and synthesis
- Analog phase shifters for radial position control

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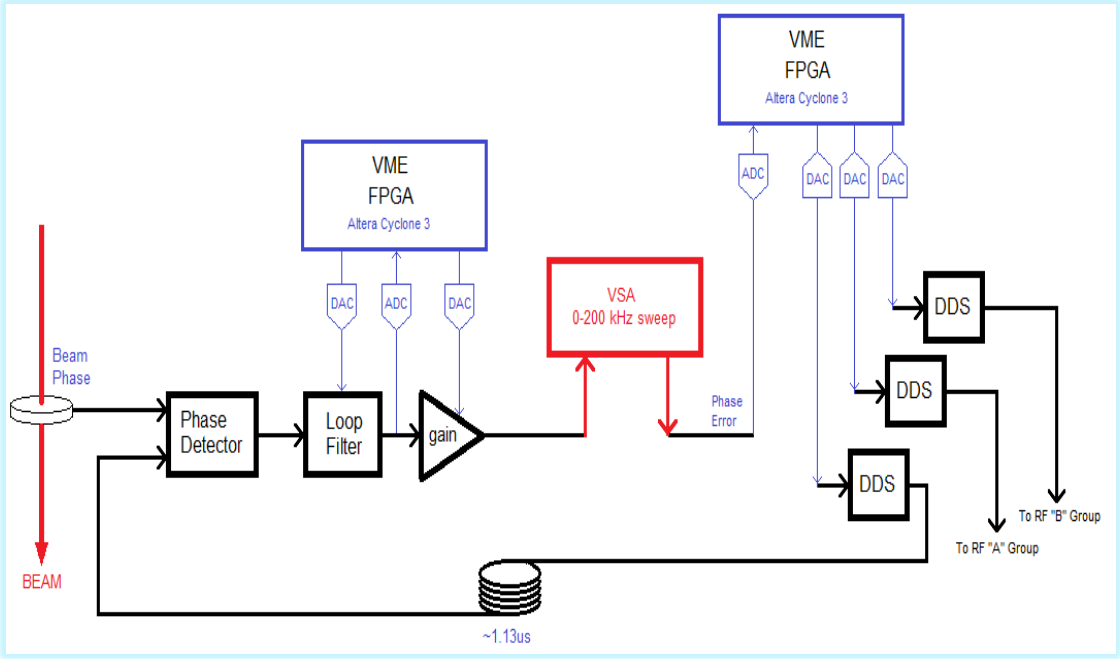
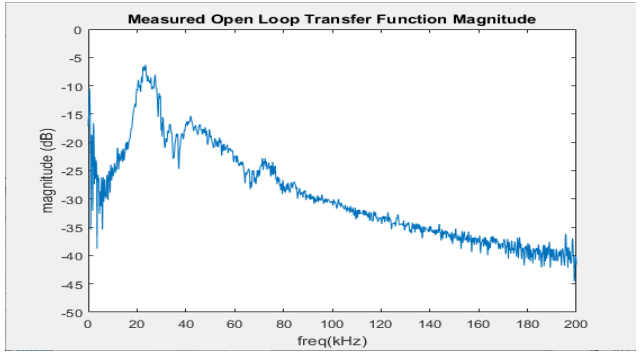
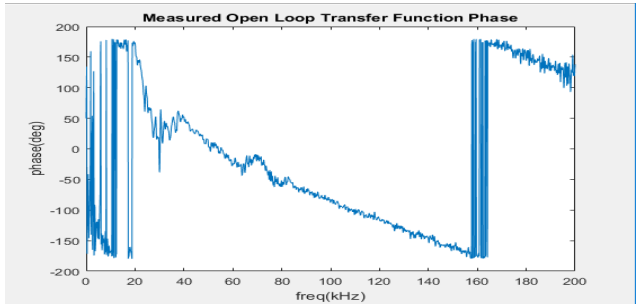
Current Booster LLRF System Open Loop Measurement







Total Loop delay = 4.5 us

Calculated delay of LLRF system = 3.37 us

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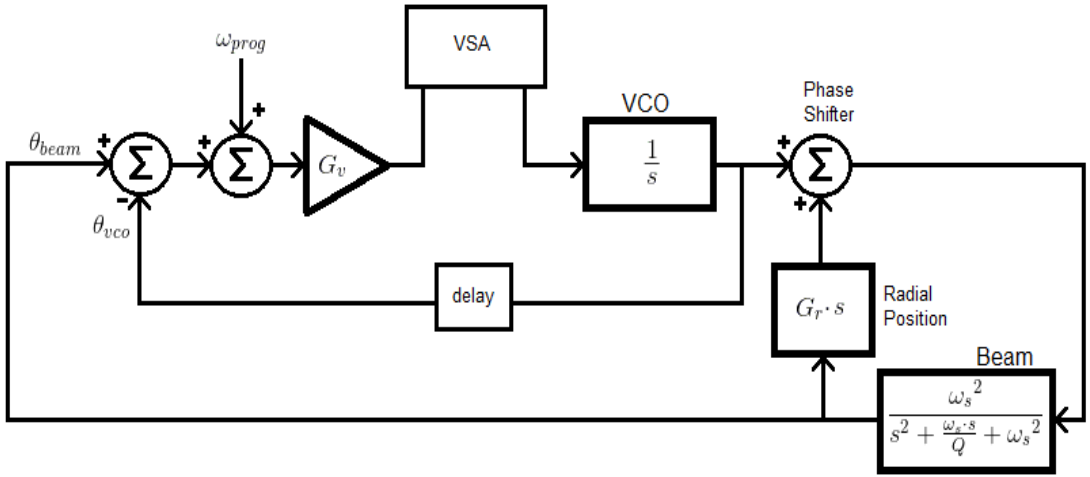
Open Loop Response – MATLAB Model vs Measured Data

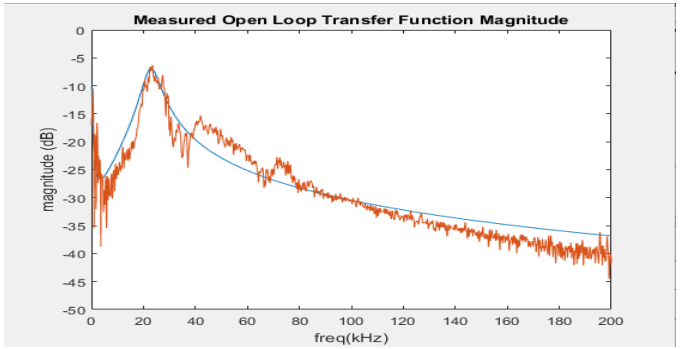


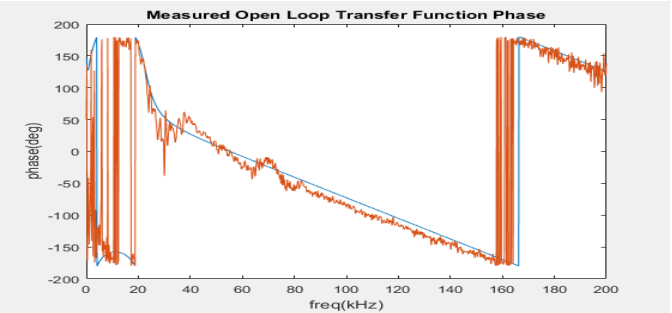
Model Parameters:

$$\omega_s = 2 \cdot \pi \cdot 23e3$$

$$Q = 3.5$$

$$G_r = 0$$





Blue = MATLAB model

Red = Measured data

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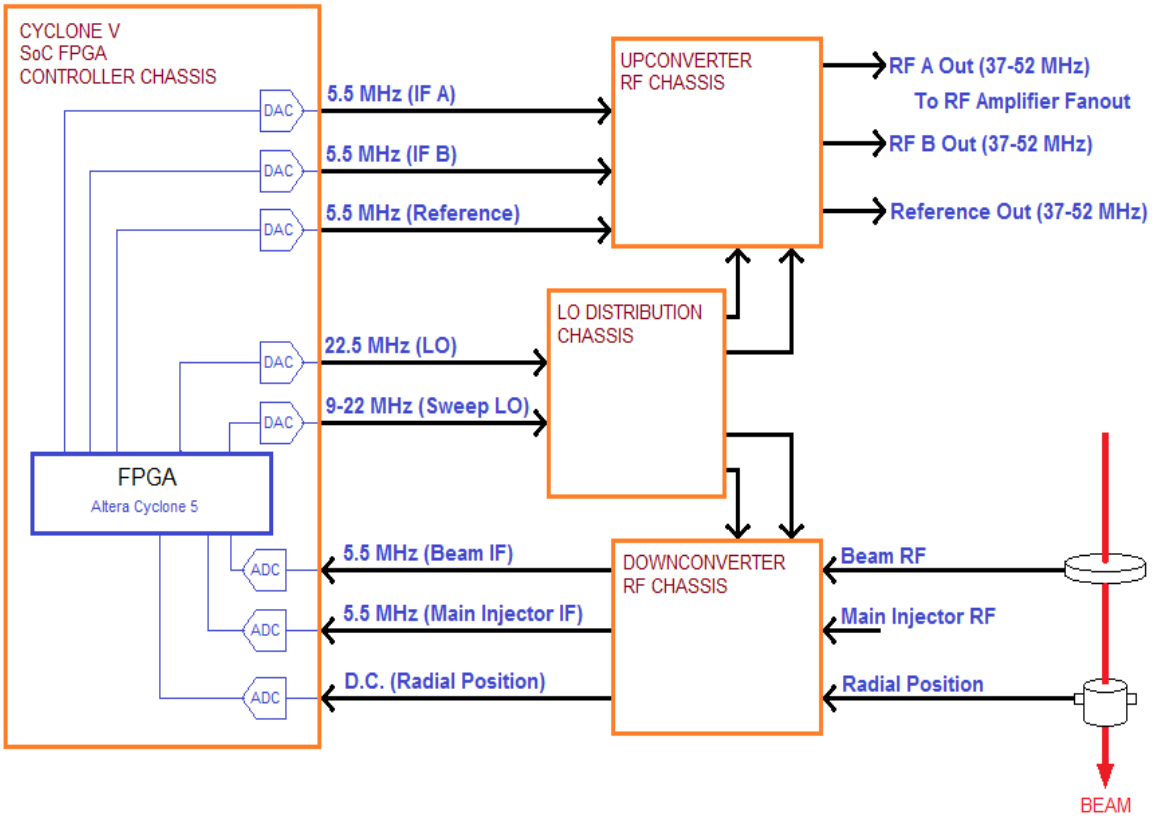
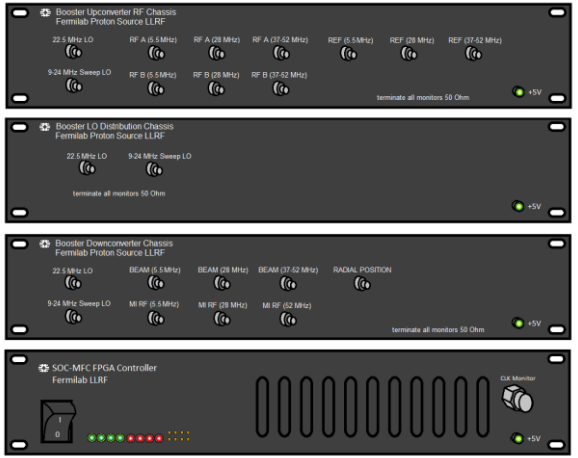
Fermilab Booster LLRF Upgrade Goals

- Reduce delay through the system
  - Increases closed loop gain
- Simplify architecture
  - Reduce number of FPGA's from 3 to 1
  - Complete controller logic on single FPGA.
- Simplify hardware layout.
- Simplify integration to PIP-II control system, timing system.
- Increase digital and RF system diagnostics.
- Ability to run at 20 Hz.
- Simplify future control system configuration upgrades.
- Simplify future FPGA hardware upgrades.

Proposed Booster LLRF System



- Single FPGA
- Fully digital feedback system
- Increased digital and analog diagnostics
- Increased system control
- Upgradable
- Low cost
- Reduced electrical
- Simple Hardware Layout



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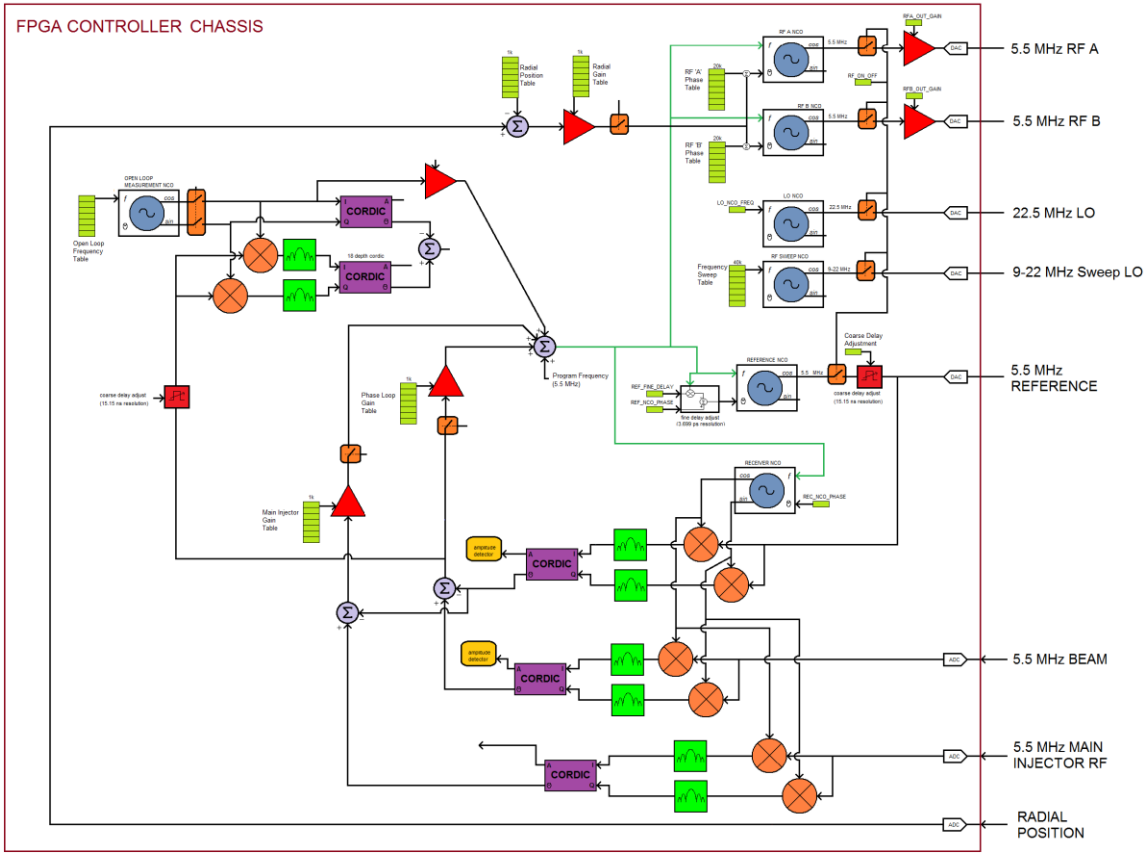
FPGA Controller



- NCO's for RF signal generation
- I/Q receivers.
- CORDIC amplitude and phase measurement.
- Internal digitally delayed reference.
- Open loop measurement circuit.
- ~1.2 us delay through FPGA chassis (includes ADC's and DAC's).
- 5.5 MHz IF chosen because running the ADC's at 66 MHz, implementing downconverter CIC filters at fs/6 is simple.
- Low 5.5 MHz IF allows for low cost ADC/DAC components.

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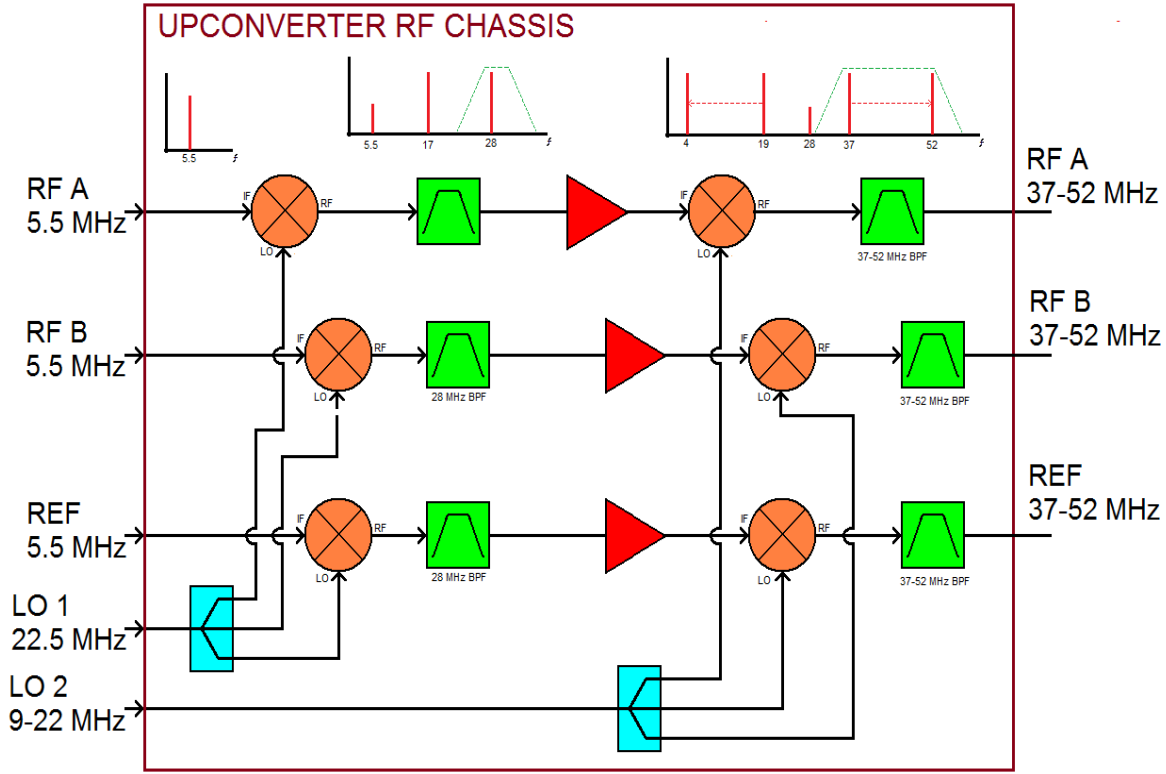
RF Signal Processing - Upconverter



- **IF/LO frequencies chosen for simplified analog and digital filter implementation**

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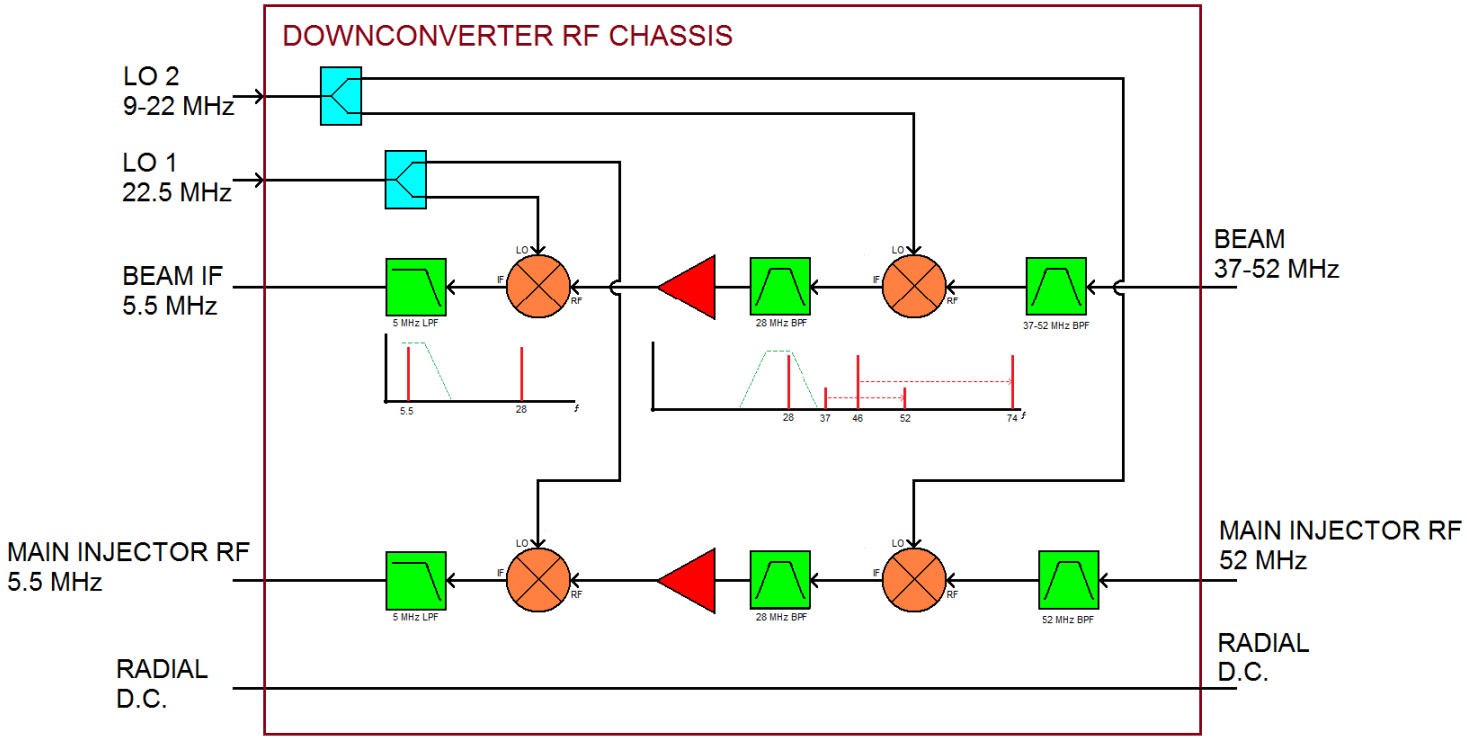
RF Signal Processing - Downconverter



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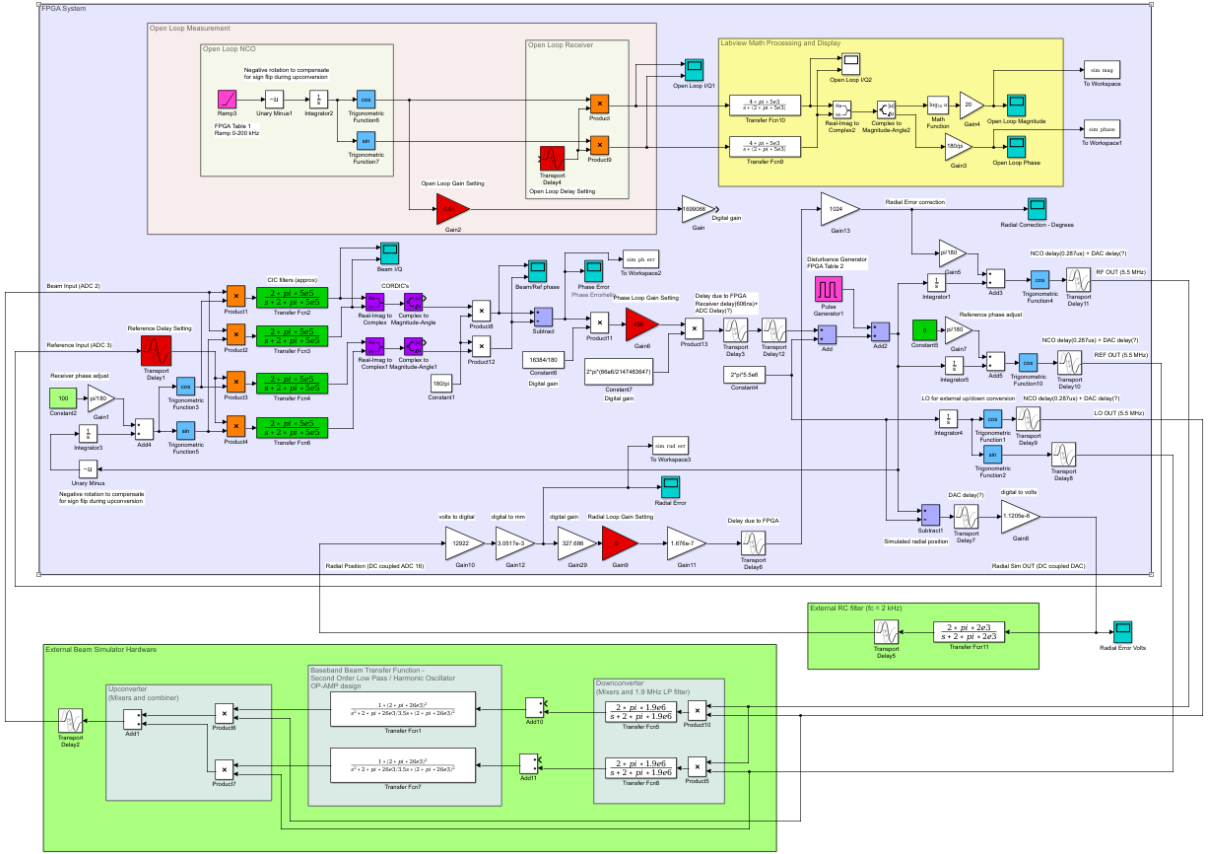
Simulink Time Domain Simulation



Simulink model features:

- Radial position simulation included.
- External radial position low pass filter.
- External beam simulation circuit uses I/Q down conversion to baseband, followed by second order low pass filters, then upconverted back to IF.
- Open loop simulation circuit included in the FPGA block.

Simulations:

- Simulation of open loop transfer function for comparison to measured data.
- Simulation with disturbance added to the frequency input of NCO's to measure the feedback suppression of phase error and radial position error.

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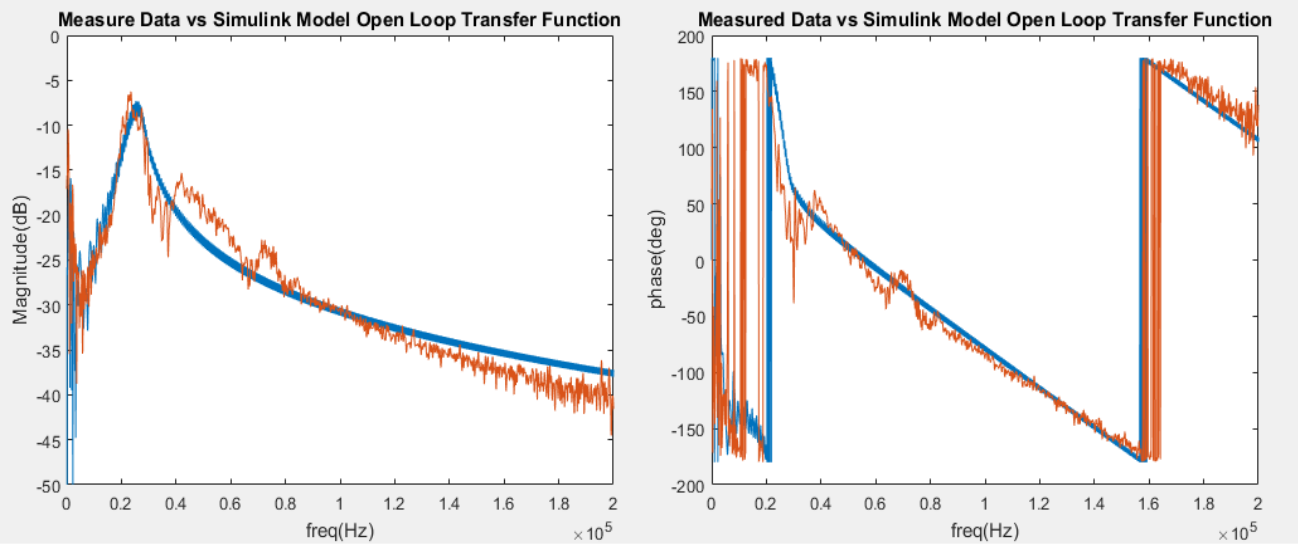
Simulink Open Loop Simulation



To match measured data, the model has the following parameters:

- 4.5 us of total electrical delay
- Beam simulation circuit has fc of 23 kHz and a Q of 3.5.

Simulink model showing good agreement with measured data.

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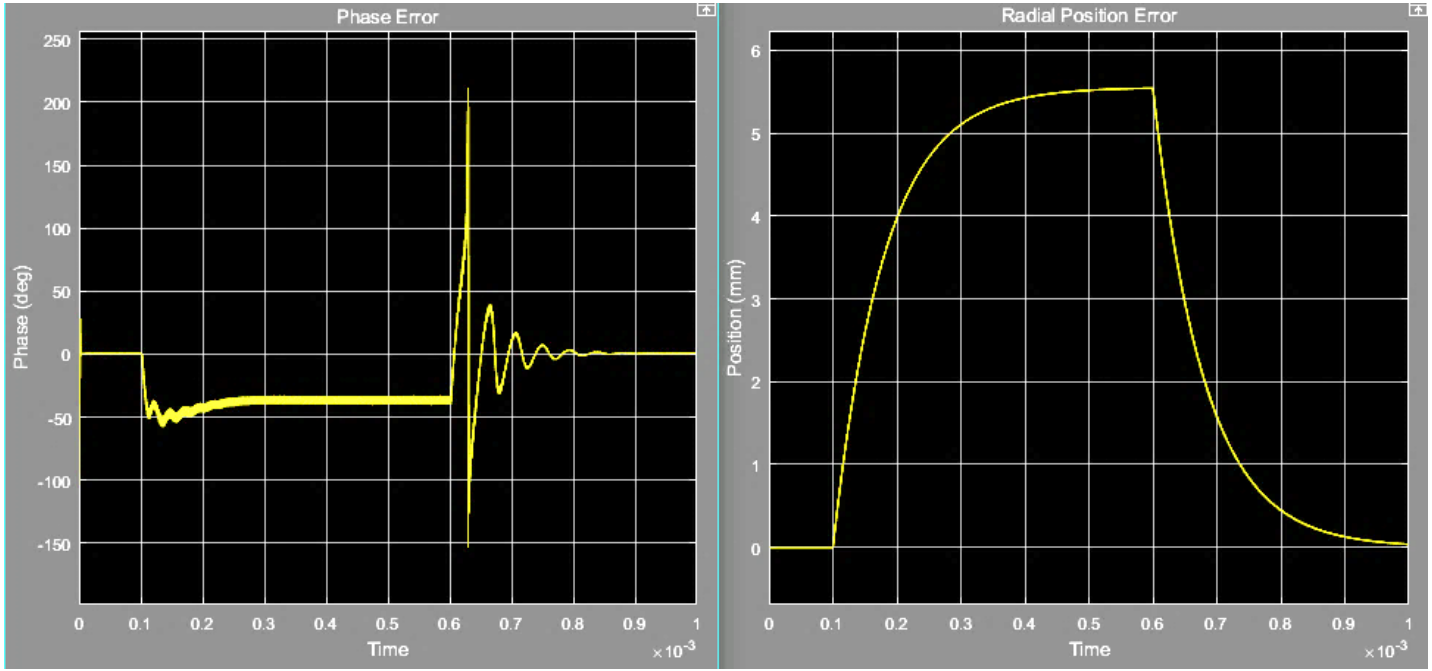
Simulink Disturbance Response



- 20 kHz step at frequency input of NCO
- Phase and radial feedback loops OFF

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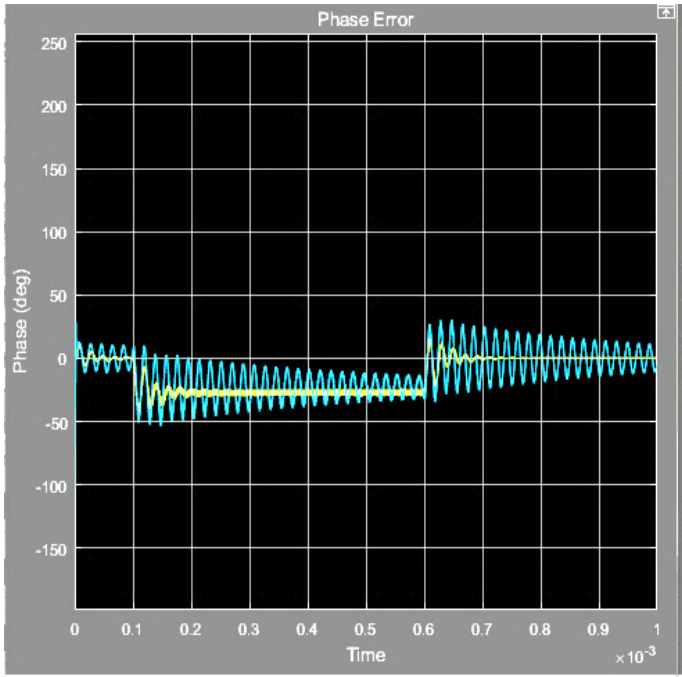
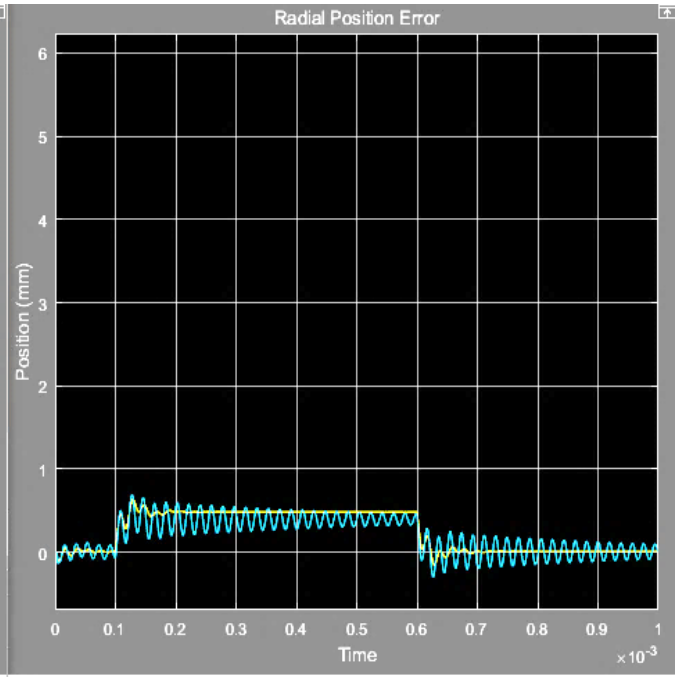
Simulink Disturbance Response





Yellow:
- Phase loop gain of ~670 Hz/deg
- Stable operation

Blue:
- Phase loop gain of 830 Hz/deg
- Instabilities starting

- 20 kHz step at frequency input of NCO
- Phase and radial loops ON
- Radial loop gain held constant
- Phase loop electrical delay = 4.5 us

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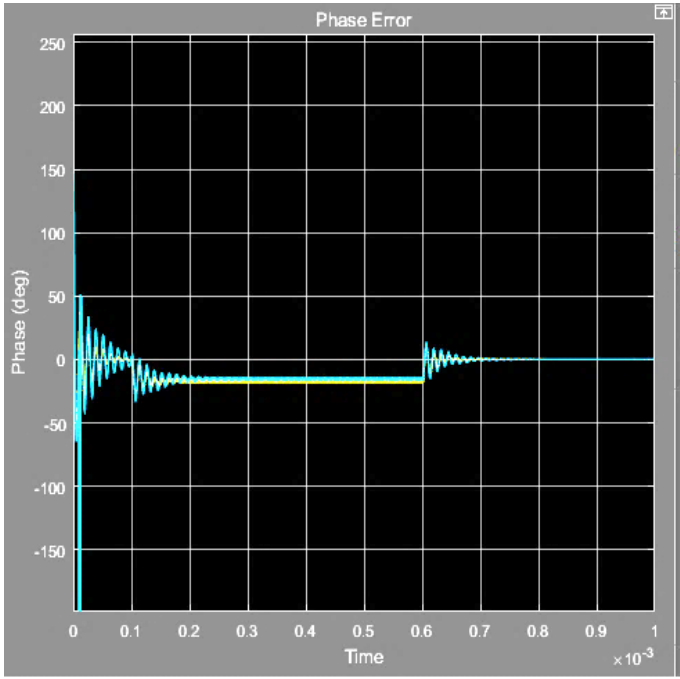
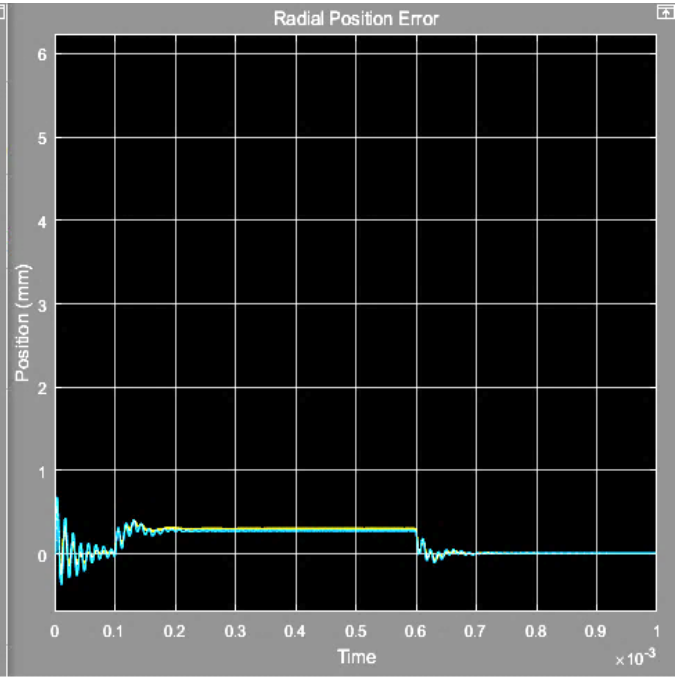
Simulink Disturbance Response – reduced electrical delay





Yellow:
- Phase loop gain of 1120 Hz/deg
- Stable operation

Blue:
- Phase loop gain of 1230 Hz/deg
- Instabilities starting

- 20 kHz step at frequency input of NCO
- Phase and radial feedback loops ON
- Radial loop gain held constant
- Phase loop electrical delay = 2.8 us

* 30% increase of phase error suppression by reducing electrical from 4.5 us to 2.8 us

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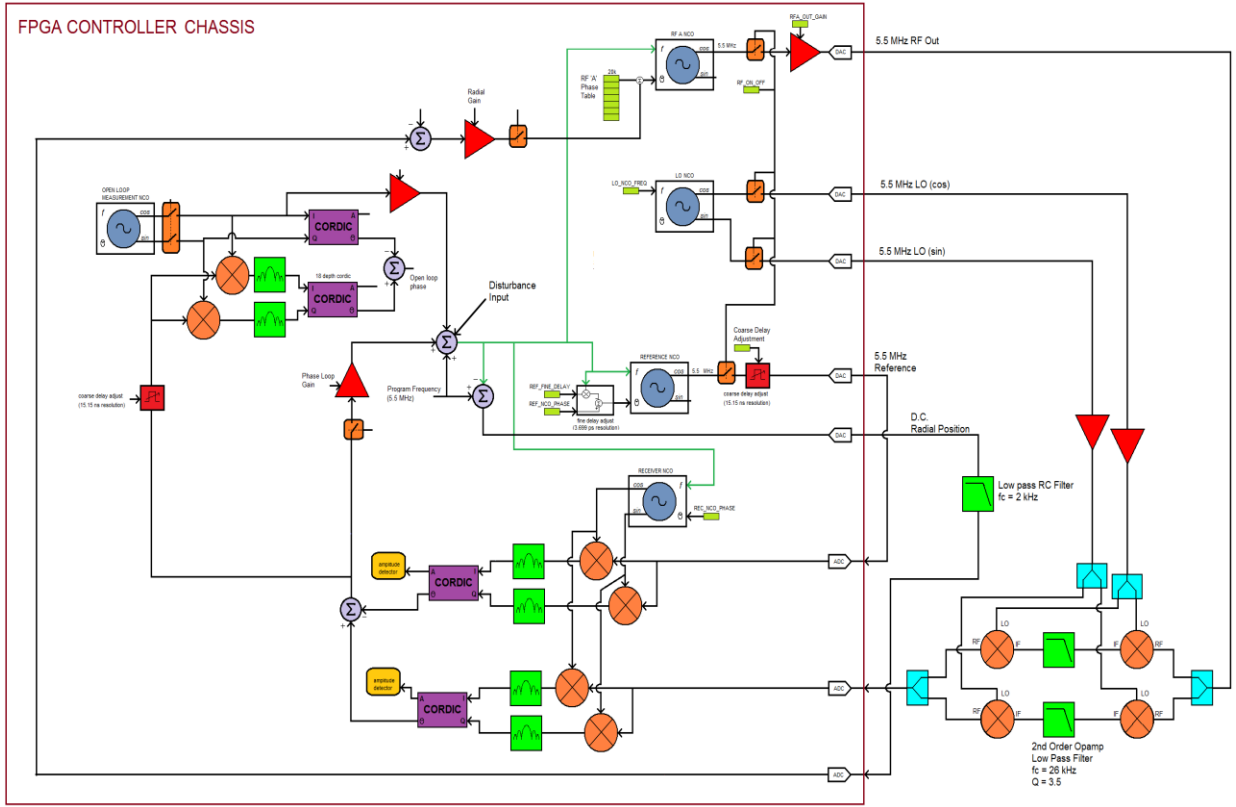
Hardware Prototyping and Testing



Hardware Test setup features:

- Signal processing done at 5.5 MHz.
- Radial position simulation included.
- External radial position low pass RC filter.
- External beam simulation circuit uses I/Q down conversion to baseband, followed by second order low pass OP-Amp filters, then upconverted back to IF.
- Open loop simulation circuit included in the FPGA block.

Testing:

- Measure open loop transfer function for comparison to measured data and Simulink model data.
- Measure phase error and radial error with disturbance added to the frequency input of NCO's, then compare to Simulink model data.

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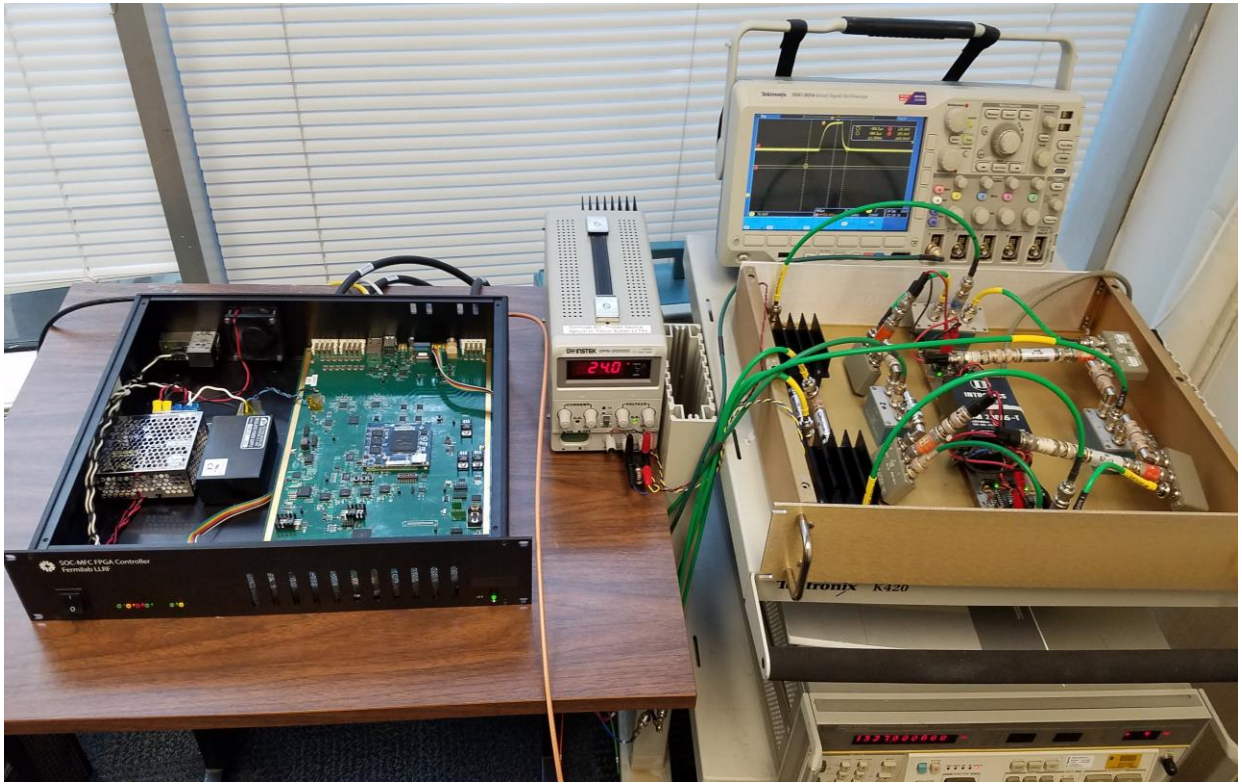
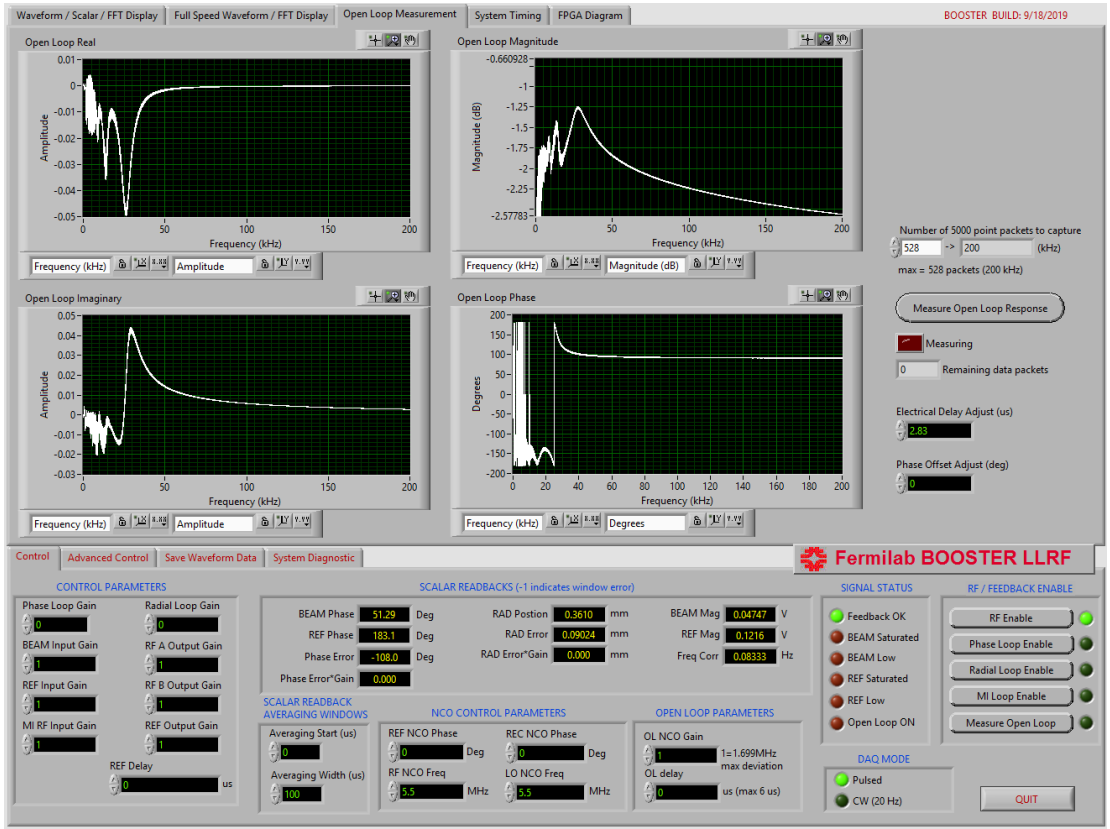
Hardware Prototype Testing Setup



FPGA Controller Chassis Features:

- Altera Cyclone 5 System on Chip (SoC)
- 16x 14 bit ADC's @ 66 MHz
- 8x 14 but DAC's @ 66 MHz

Hardware Prototype Open Loop Measurement



Measurement shows a phase loop electrical delay of ~2.8 us. (This is the electrical delay used in the previous Simulink simulations showing 30% phase suppression improvement)

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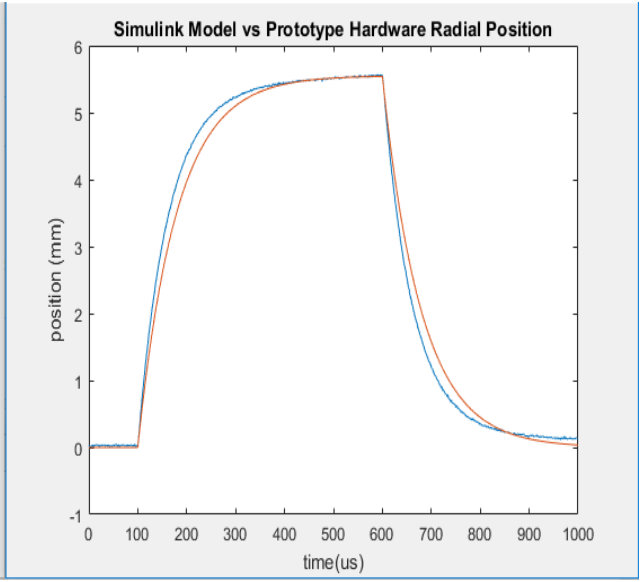
Hardware Prototype vs Simulink Model Disturbance Response



Red: Simulink

Blue: Prototype hardware

* Feedback loops OFF

Good agreement between hardware prototype and Simulink model

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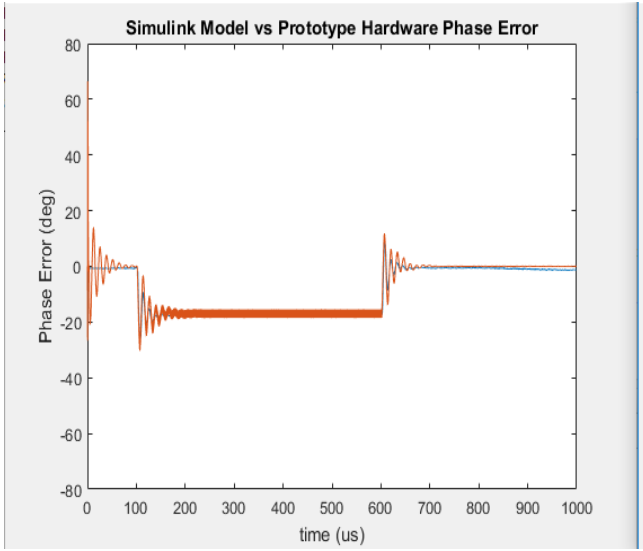
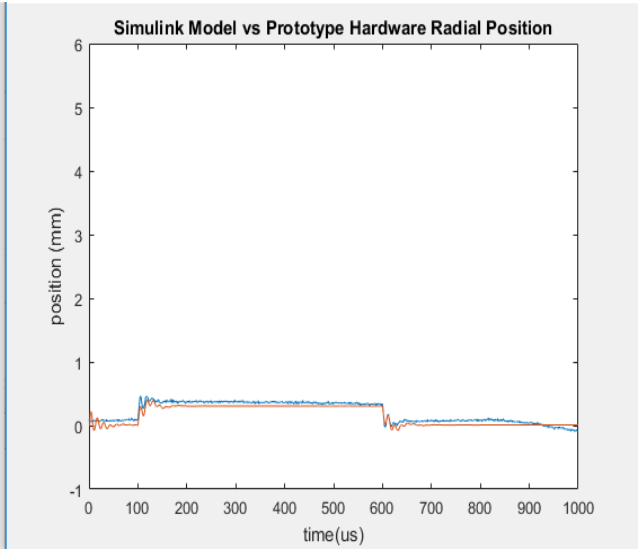
Hardware Prototype vs Simulink Model Disturbance Response





Red: Simulink

Blue: Prototype hardware

* Feedback loops ON

Hardware shows stable operation at phase loop gain of 1230 Hz/deg in agreement with Simulink model.

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Conclusions

- A prototype of a proposed hardware FPGA controller for the Fermilab PIP-II Era Booster has been developed and has completed initial testing.
- The prototyped controller shows improvement over the current system by reducing the electrical delay through the system by 1.7 us and improving disturbance suppression by over 30%.
- A MATLAB model and Simulink model have also been developed that show good agreement with the hardware prototype and measured data.
- A feasible Booster LLRF system to interface with the PIP-II Linac has been demonstrated.