APS-U LLRF Systems

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Outline

- APS-U RF systems at a glance
- Digital LLRF Development
- Hardware Plans
- Plans for new RF source
- Conclusion

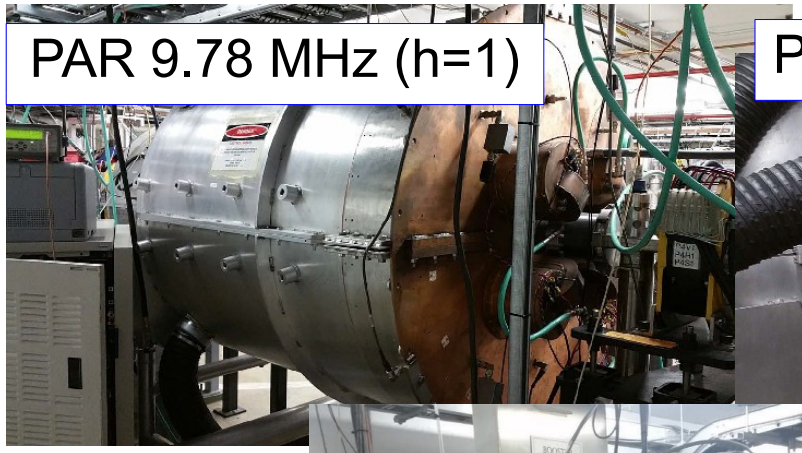
APS-U RF systems at a glance

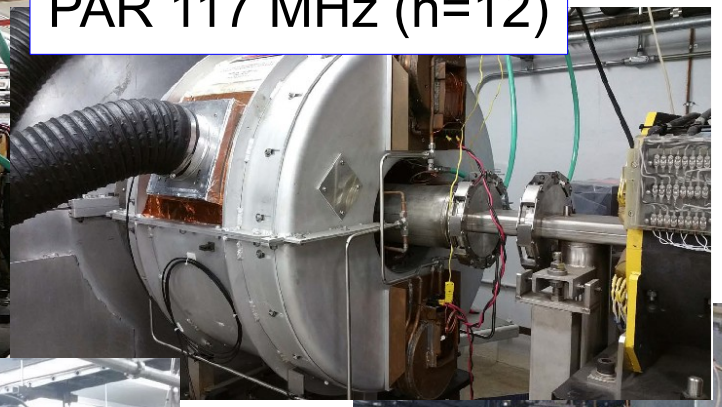
- Storage Ring is being replaced with a Multi-Bend Achromat (MBA) lattice
- Adding a passive superconducting bunch lengthening system (BLS) cavity to alleviate emittance and lifetime concerns
- Upgrading existing LLRF analog systems to digital
- Linac 375 MeV presently → 450 MeV (operations)
  - Reduce PAR bunch length blowup
- Particle Accumulator ring 2nC → 20nC
  - Heavy beam-loading
- Booster 7GeV → 6GeV, 2nC → 20nC
  - Heavy transient beam-loading
- Storage Ring 7GeV → 6GeV
  - top-up → swap-out (hence need for 20nC)

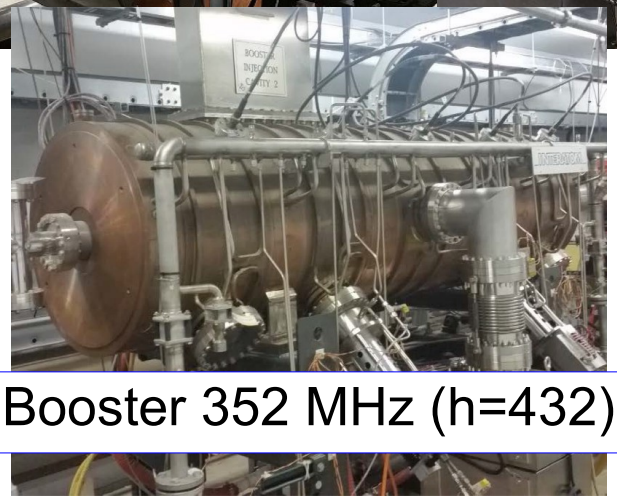
- Storage Ring circumference is shrinking, Booster staying the same → need for new synchronization scheme

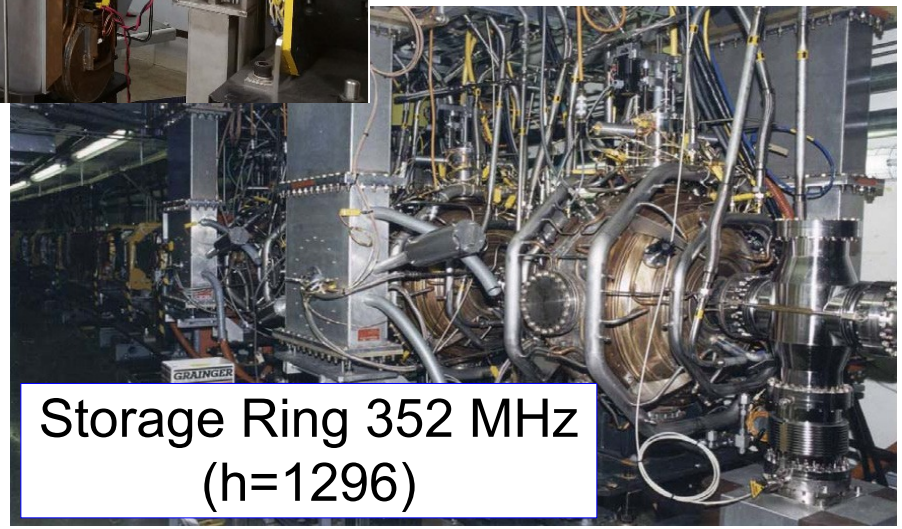
APS-U RF systems at a glance

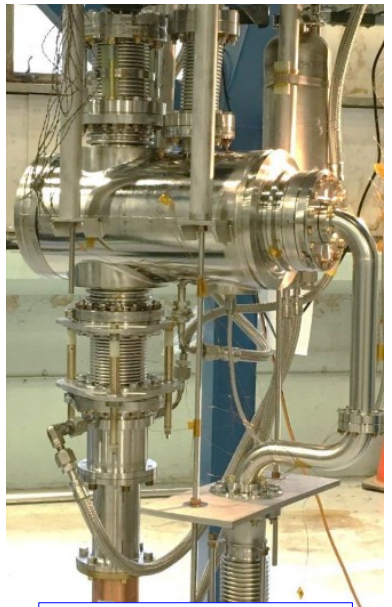
- We have a variety of RF systems with various configurations to support and various bandwidths
- PAR cavities: 1 CW, 1 pulsed, both use dynamic ferrite tuners, 117MHz ½ BW = 96kHz (**latency matters**)
- Booster: Four 5-cell cavities, all 4 driven by a single klystron
- Storage Ring: 16 present single-cell cavities, (12 APS-U), driven by 2 klystrons (eventually individual SSAs)
  - SRF bunch lengthening cavity driven only by beam, amp regulation via pneumatic tuner, active tune-up
- Sought a common framework and platform, started on the simplest system: PAR Fund. CW, ½ BW = 2kHz


PAR 9.78 MHz (h=1)


PAR 117 MHz (h=12)


Booster 352 MHz (h=432)

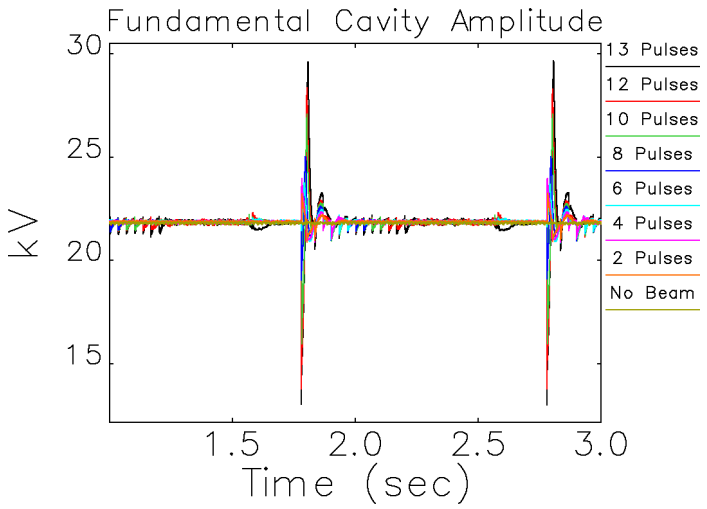

Storage Ring 352 MHz (h=1296)

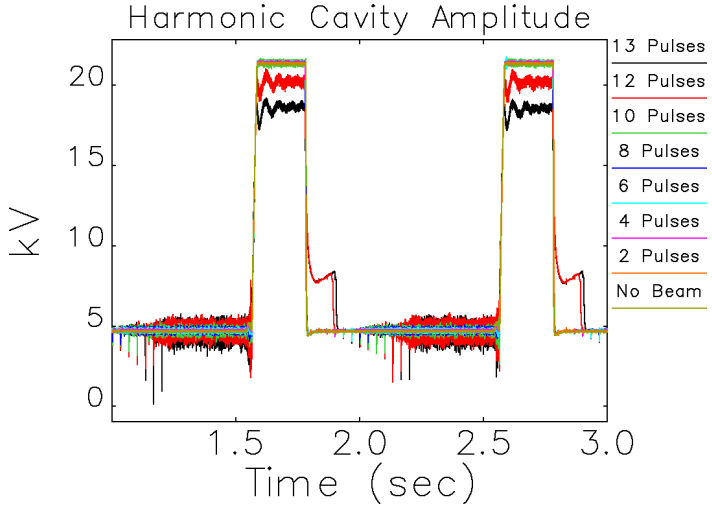

4th harmonic 1.4GHz BLS cavity

Digital LLRF Development in PAR

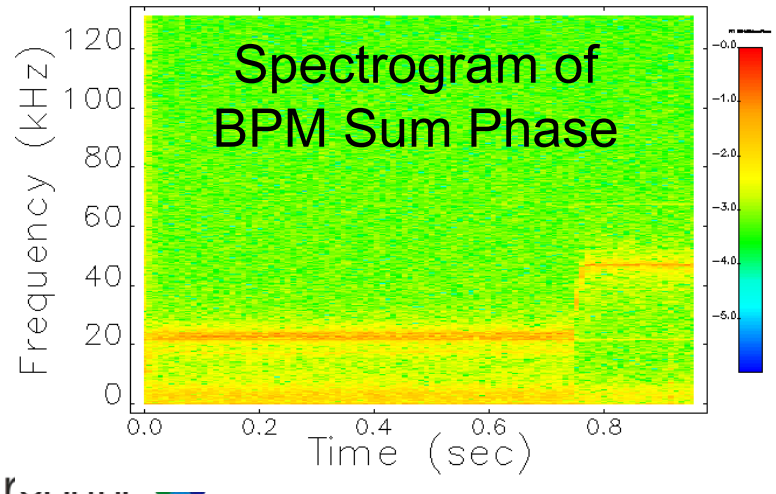
Digital LLRF Development in PAR

- LLRF4-based system provided us diagnostics to support physics studies
- and motivation for software framework (see T. Madden's talk)

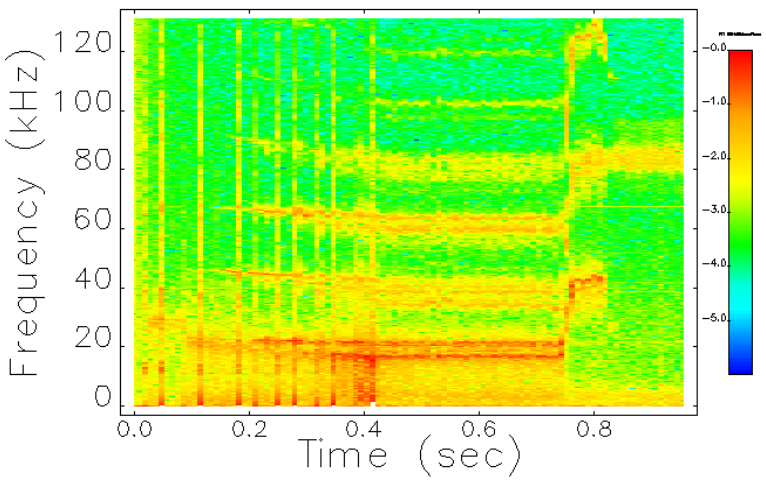




~ 2nC in PAR



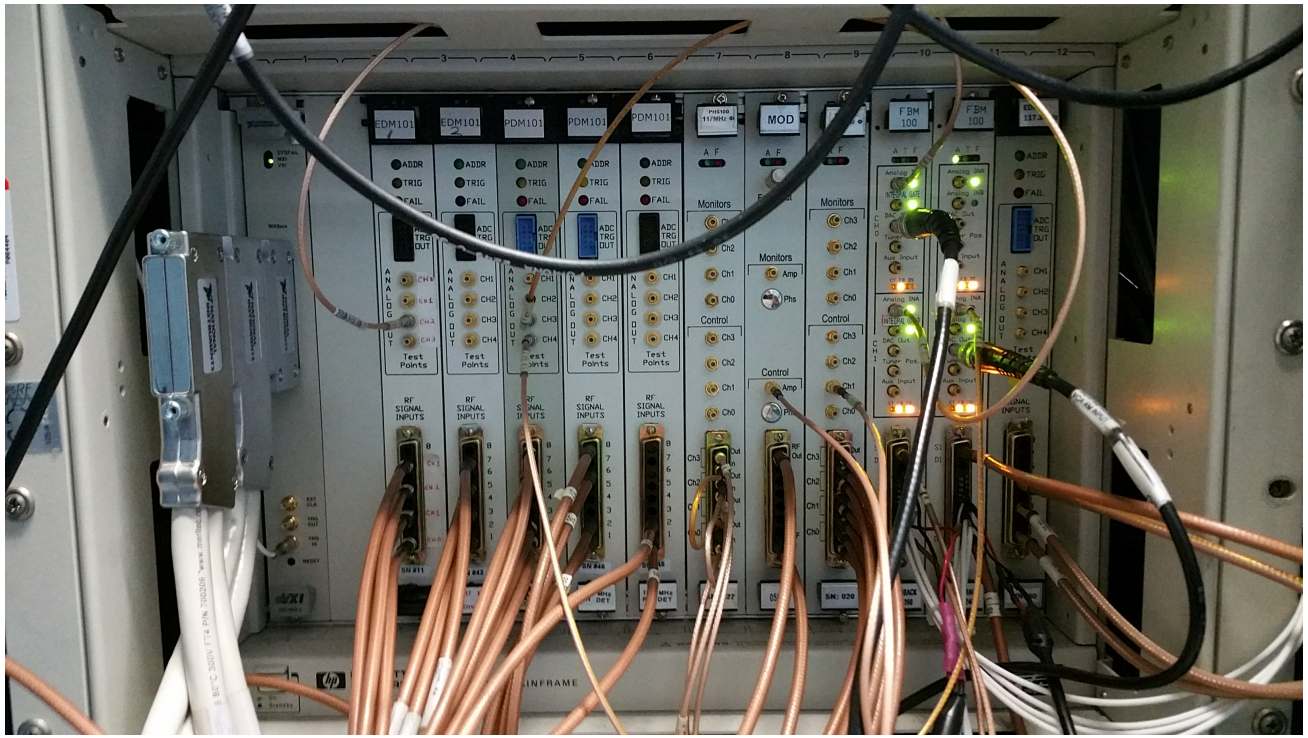
~ 14nC in PAR



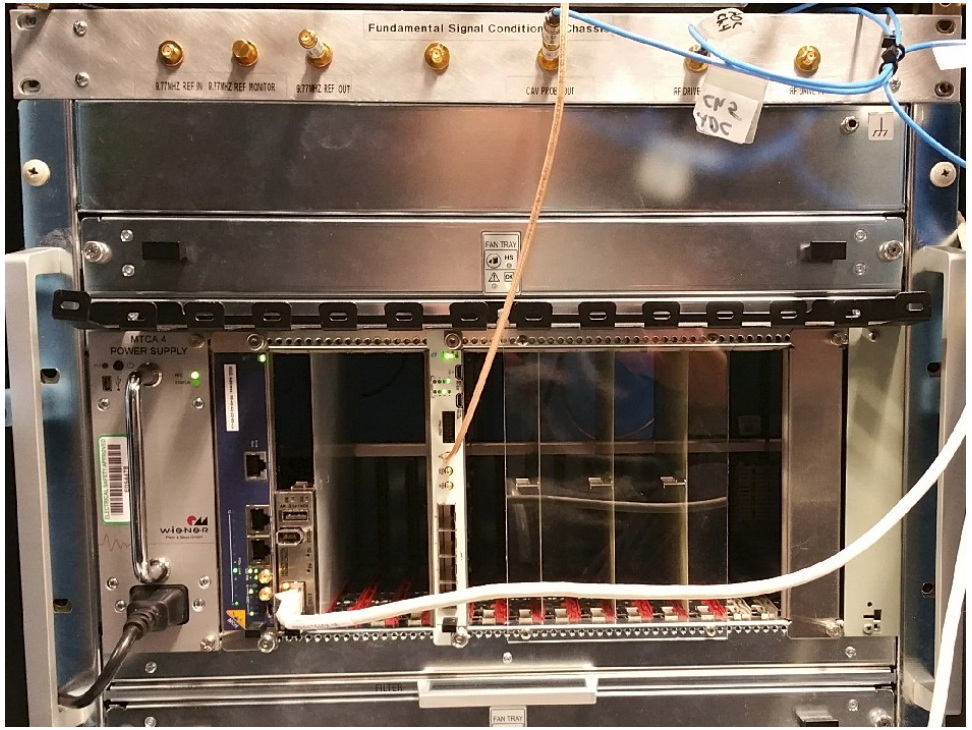
Digital LLRF Development in PAR

- Replace plethora of analog modules (amp/phase det., variable atten., phase shifts, op-amp PIDs) with single Digital LLRF module
- Nothing relatively new, but always a good reminder of what things used to be
- Will eventually go to smaller uTCA chassis for single cavity systems

Existing Analog LLRF

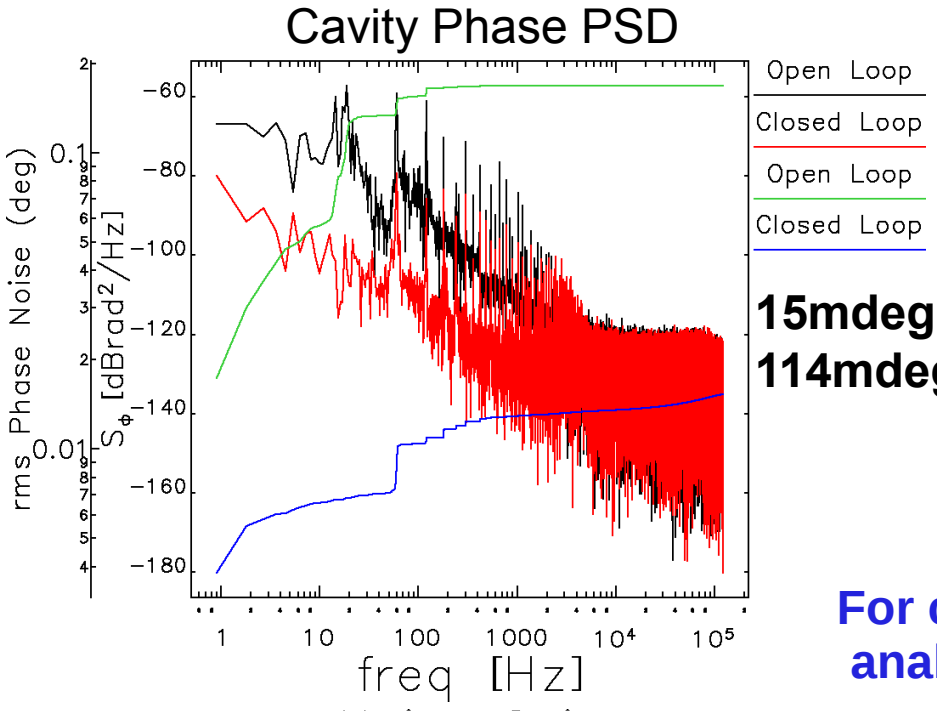


Prototype Digital LLRF

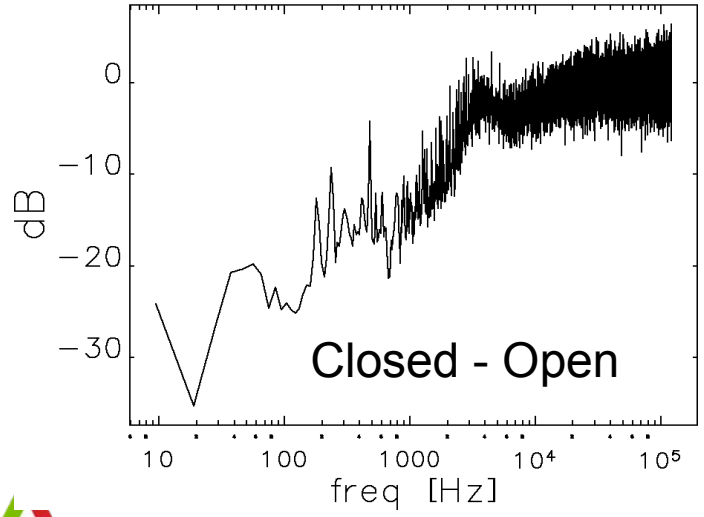


Digital LLRF Development in PAR – uTCA Demo (not yet pushing gains)

Out-of-Loop w/ LLRF4



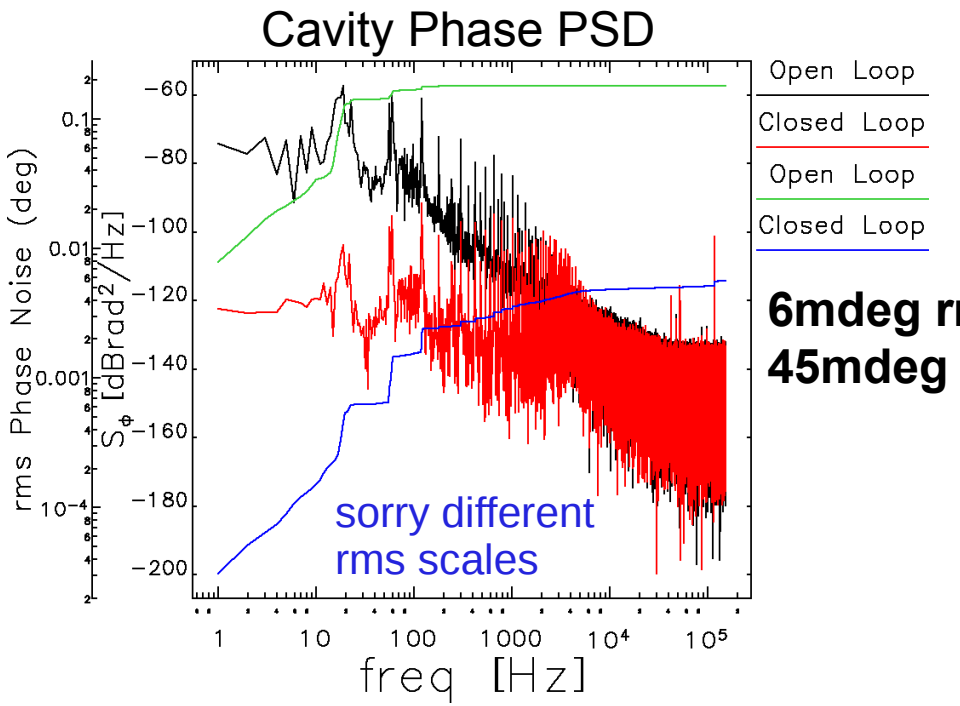
15mdeg rms
114mdeg pp



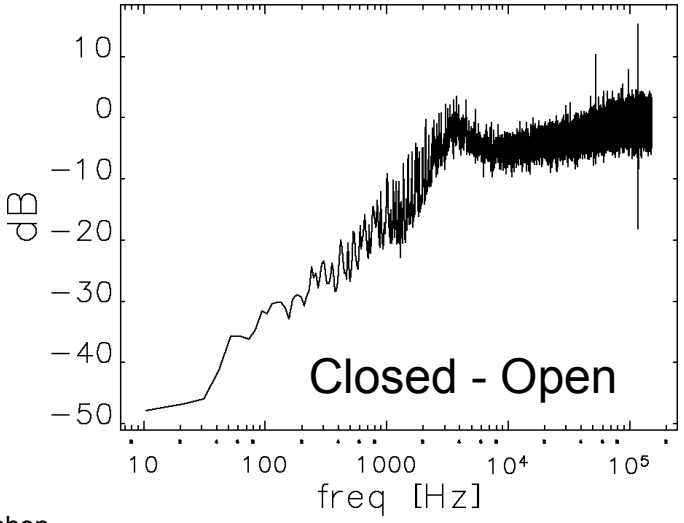
For comparison, analog system:

81mdeg rms
0.5deg pp

in-Loop

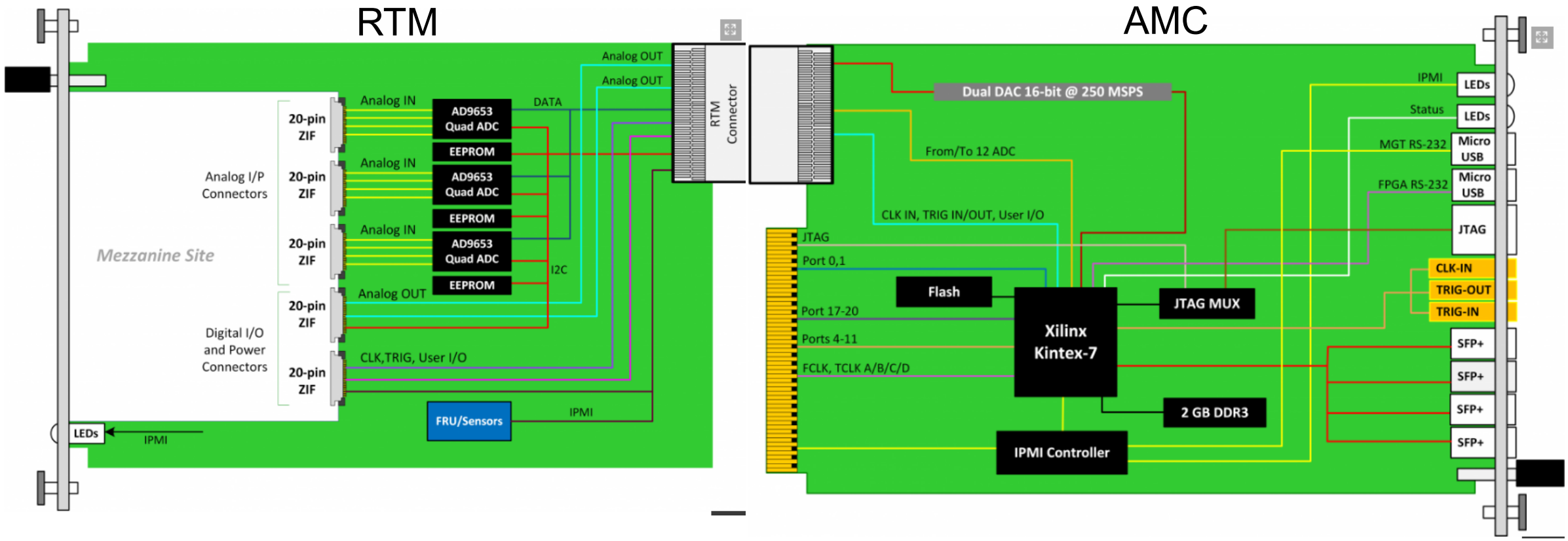


6mdeg rms
45mdeg pp



Hardware Plans

uTCA Hardware Options – AMC + RTM



Advantages

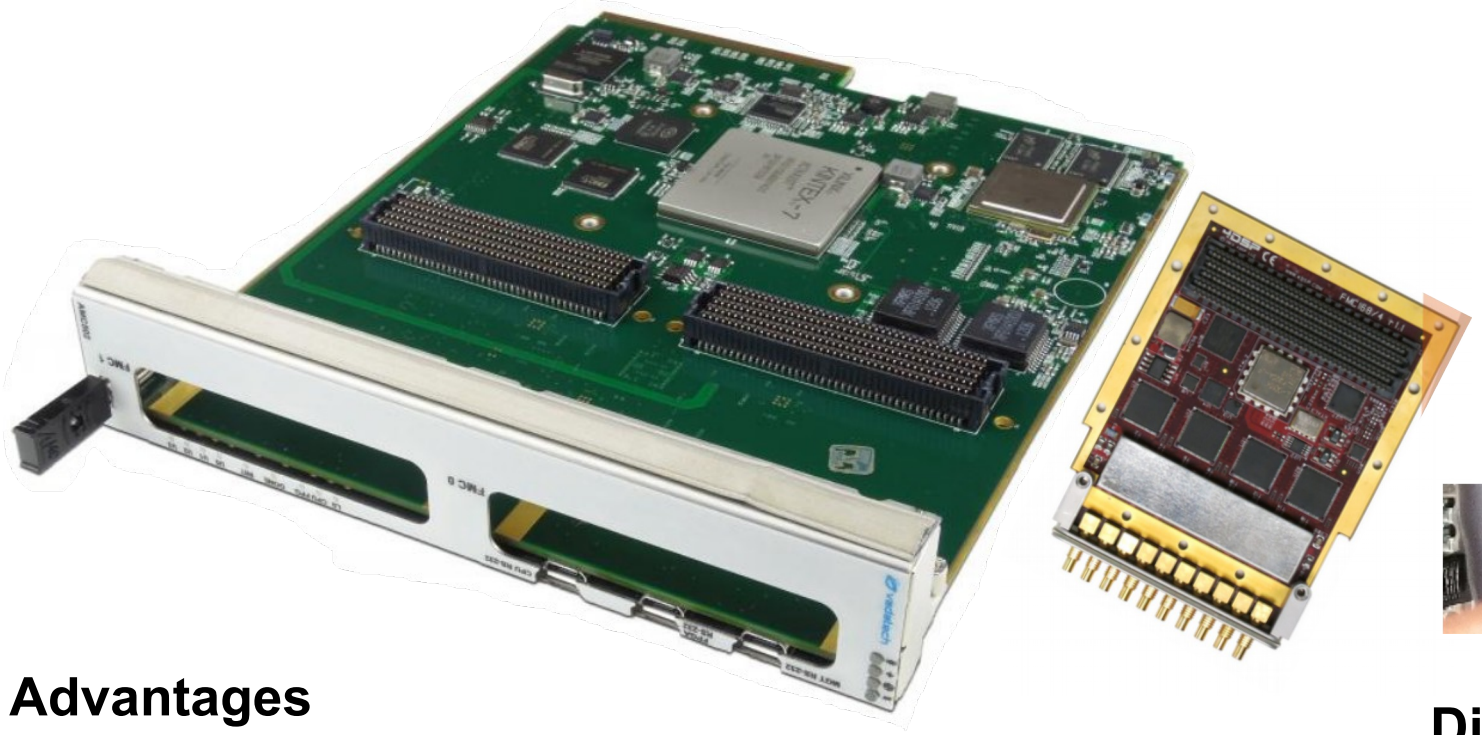
- real estate
- I/O / cabling in back

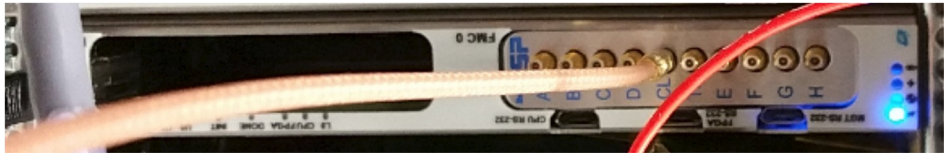
Disadvantages

- RTM Connector (Zone 3) lacks standards (various classes)
  => limited interoperability of AMCs & RTMs (i.e., have to buy together)
- Zone 3 has limited number of pins (120 pins, 60pairs only 48 are user-defined)
  => limits interconnects between RTM and AMC / FPGA, especially parallel LVDS

uTCA Hardware Options – FMC Carrier

We have chosen to use FMCs





Advantages

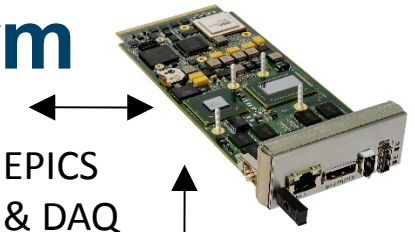
- FMC is a clear standard, high pin count connector (HPC) has 400 pins, 80 user-defined pairs or 160 single-ended signals, 10 multi-gigabit transceivers, dual FMC carrier doubles all that !
- Can mix/match FMCs and AMCs
- Can upgrade AMC or FMC without the other
- Not locked into uTCA.4

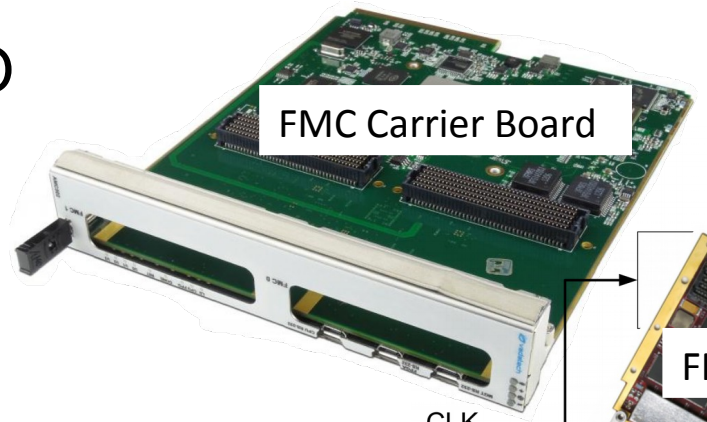
Disadvantages

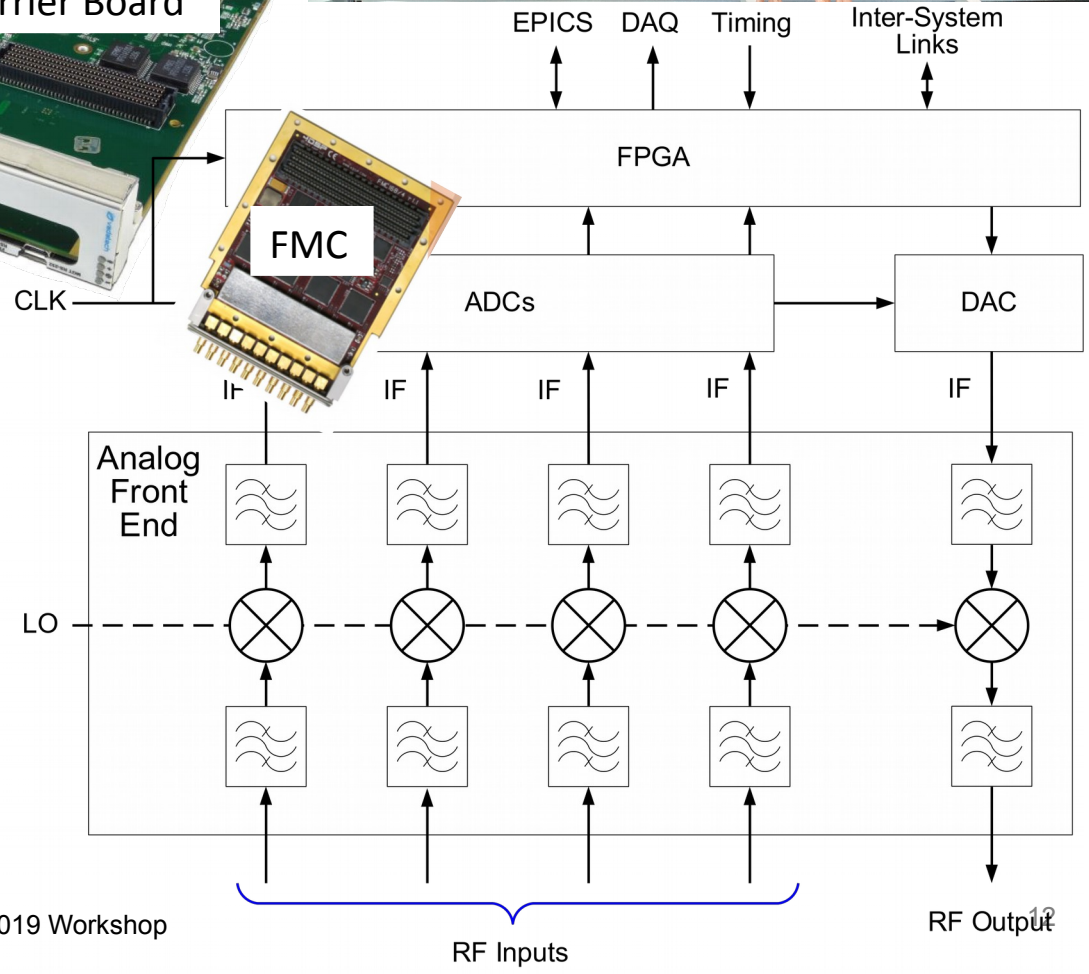
- Limited FMC real estate, BUT ….
  can stack / have double high FMC's
- Limited front panel space, BUT ….
  can go to full size or 8HP panel
- I/O / cabling in front

Common uTCA LLRF Platform

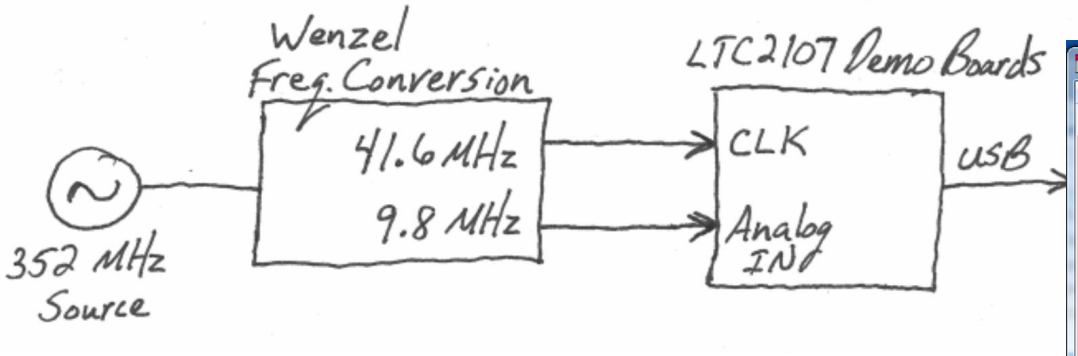
- MicroTCA chassis
- FPGA Mezzanine Card carrier
- FMCs with ADCs/DAC and I/O
- CPU for communications
  - PCIe between FPGA and CPU
  - EPICS IOC runs on CPU
    - register read/write
    - waveform streaming to fast Data AcQuisition System (DAQ) – (see T. Madden's talk)
- External analog front ends for down-converting from/to RF/IF, Fermilab AFE for Booster and BLS, PAR direct sample





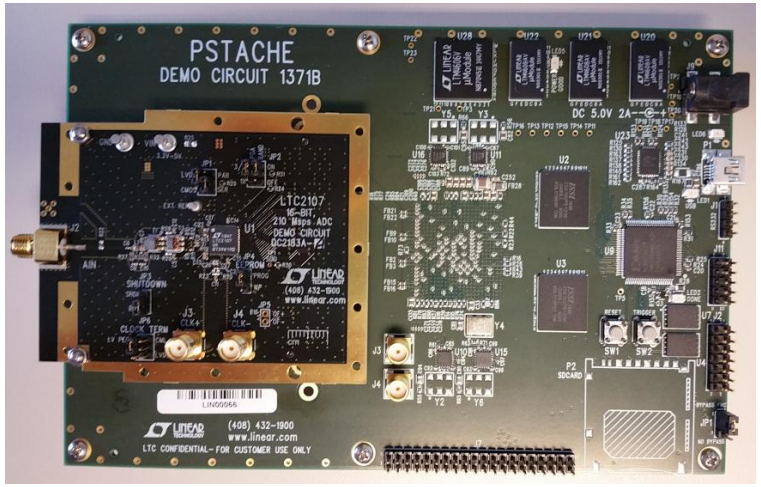


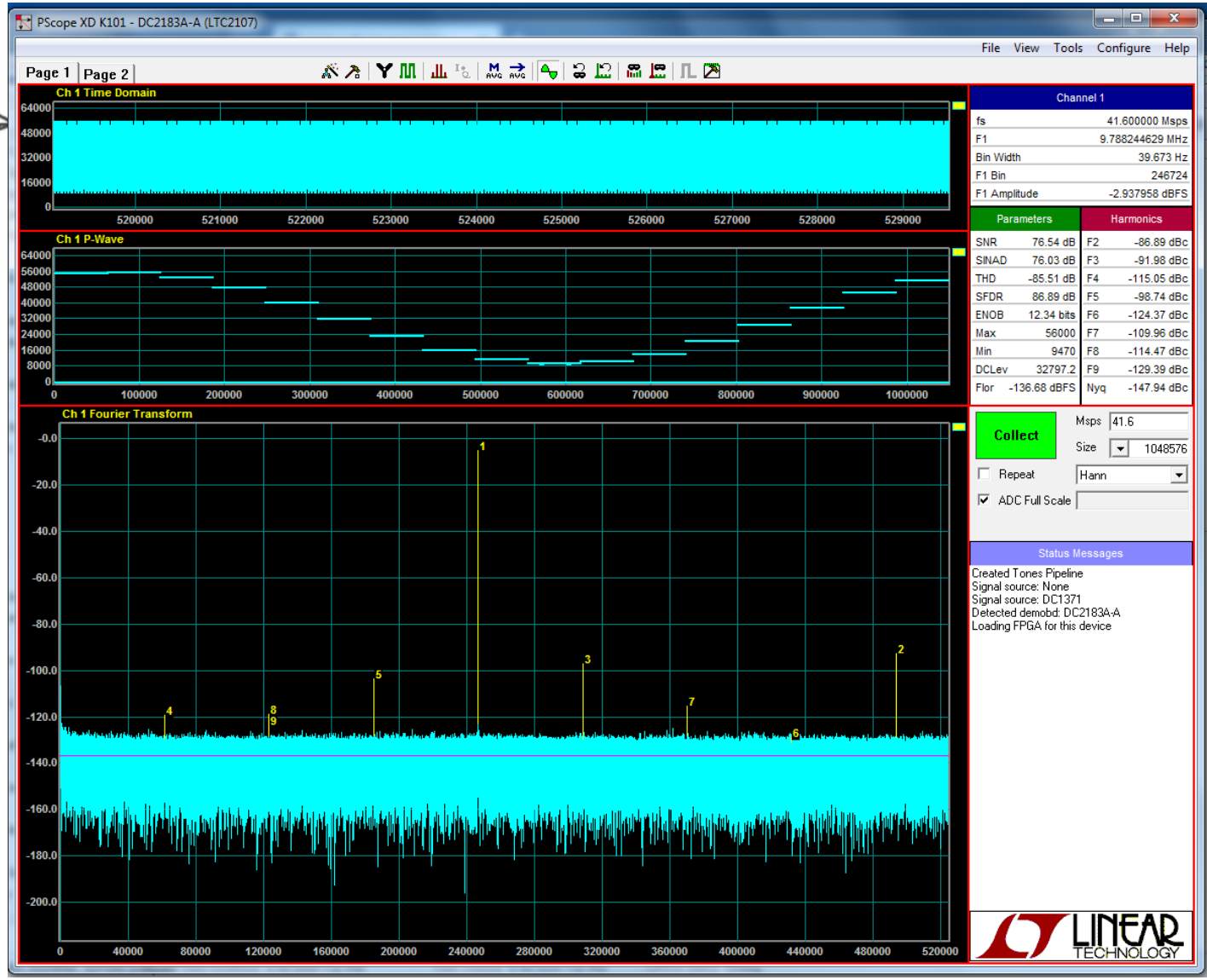
Component Eval. - LTC2107 ADC (16-bit, 210MSPS, 80dBFS SNR, latency=7 cycles)



- Coherent sampling with 4/17 ratio
- Meas. 76.5dB SNR at -2.9dBFS input

  → **~ 79dBFS SNR, datasheet is 80dBFS**





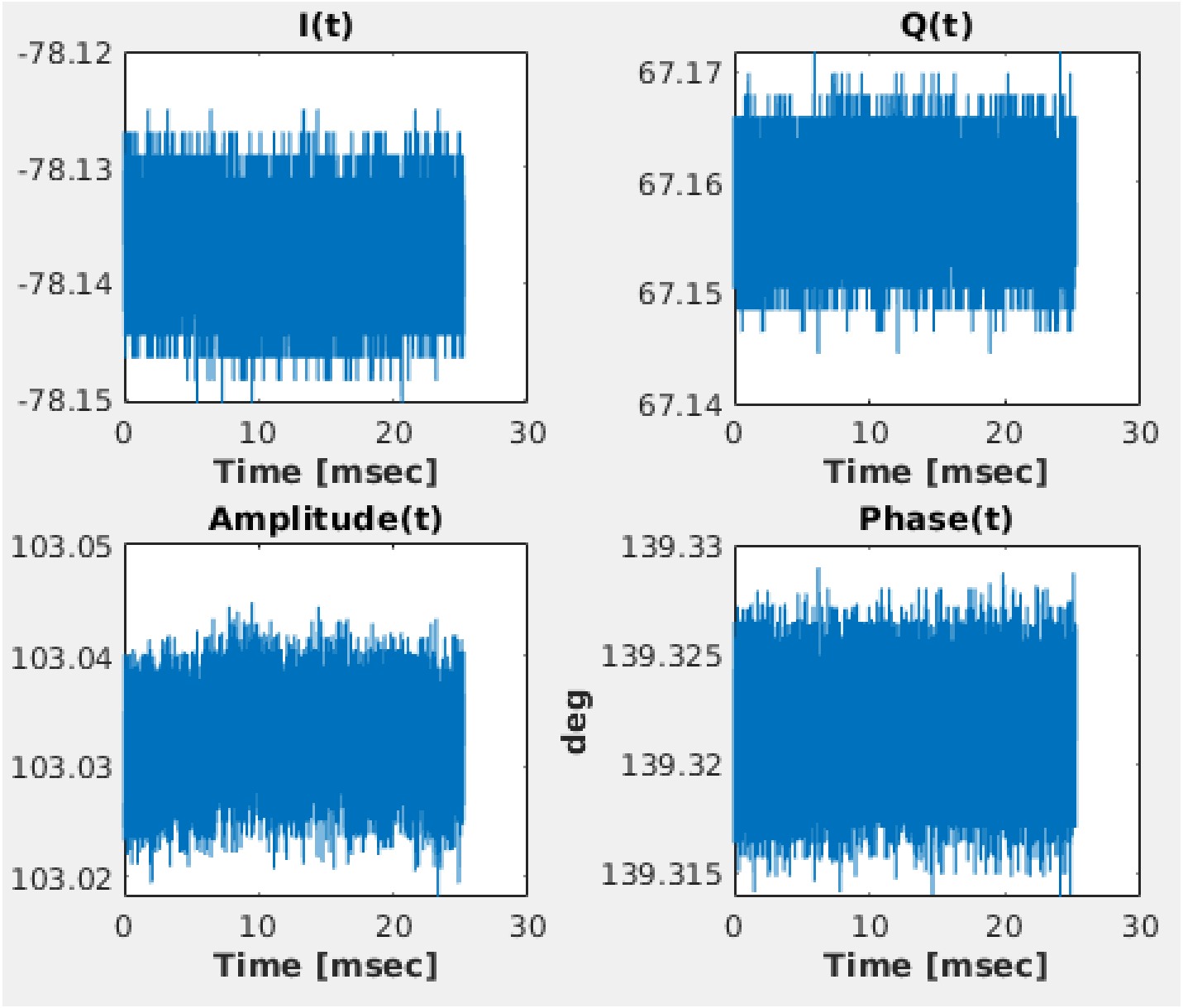
Component Evaluations – LTC2107 ADC

@ -2.9 dBFS input

- Post-process the data with bit accurate simulation of Digital Down-Conversion

- Phase Noise (1.2 MHz BW)
  - **15 mdeg peak-to-peak**
  - **1.9 mdeg rms**

- Amplitude Noise (1.2 MHz BW)
  - **0.026% peak-to-peak**
  - **0.003% rms**



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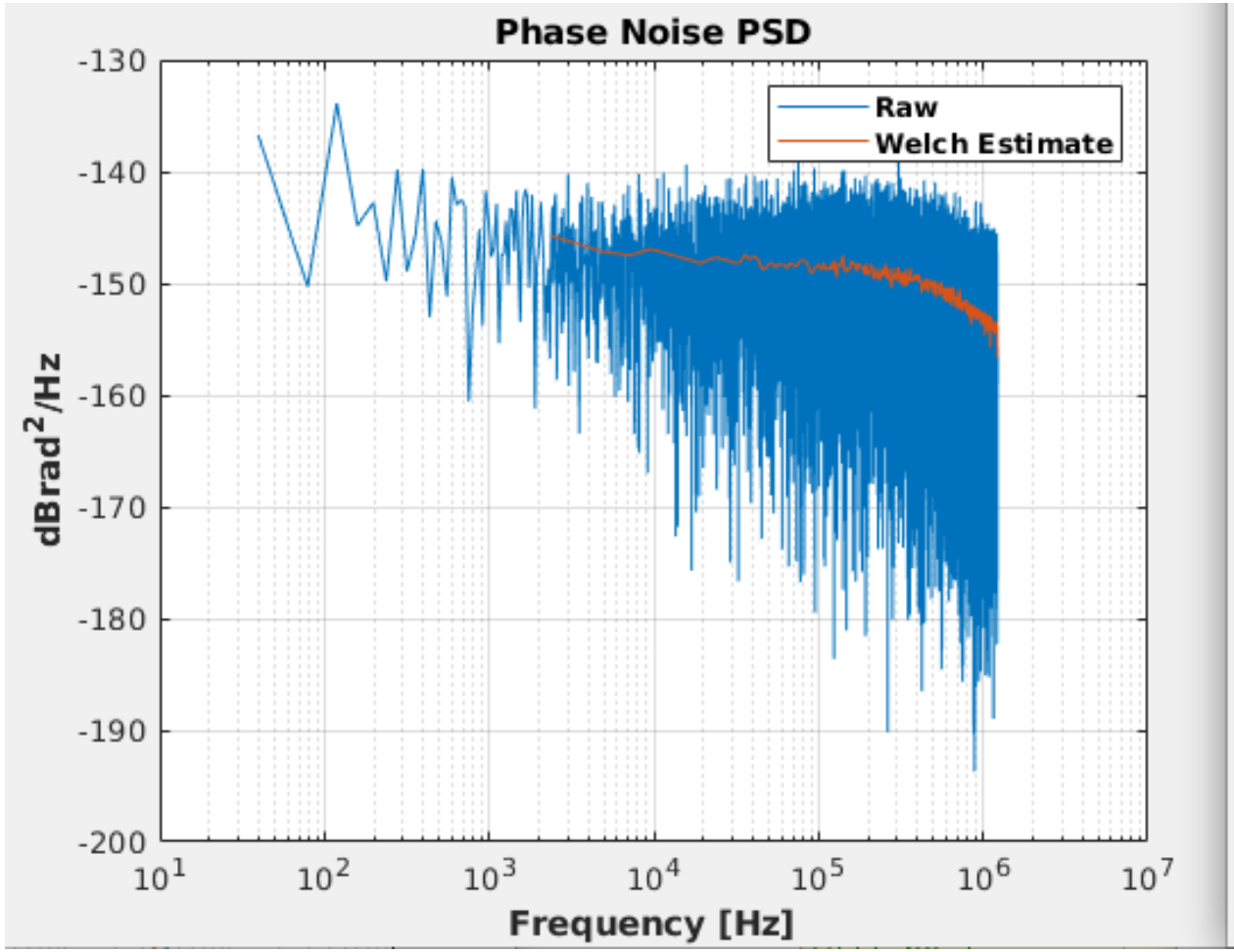
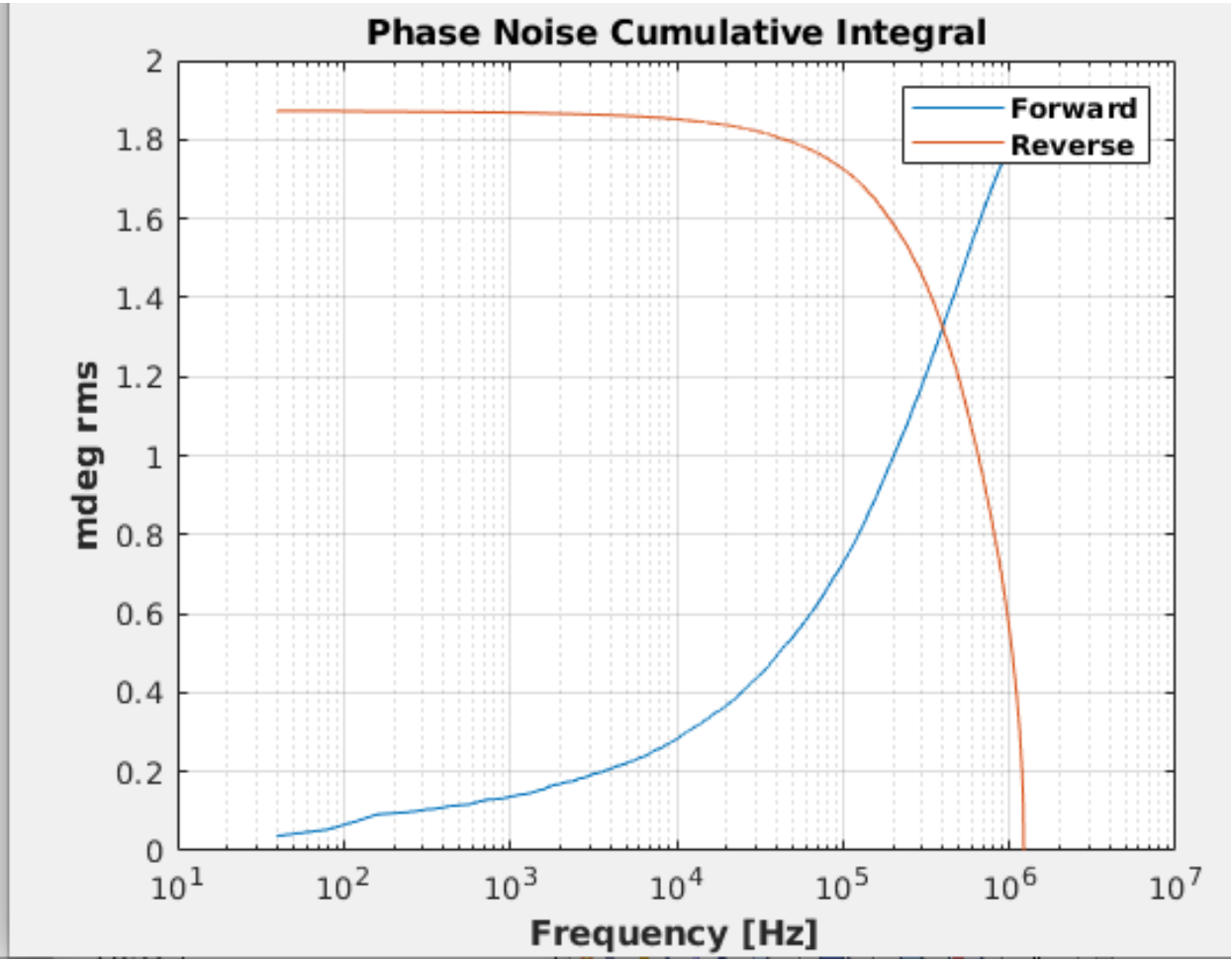
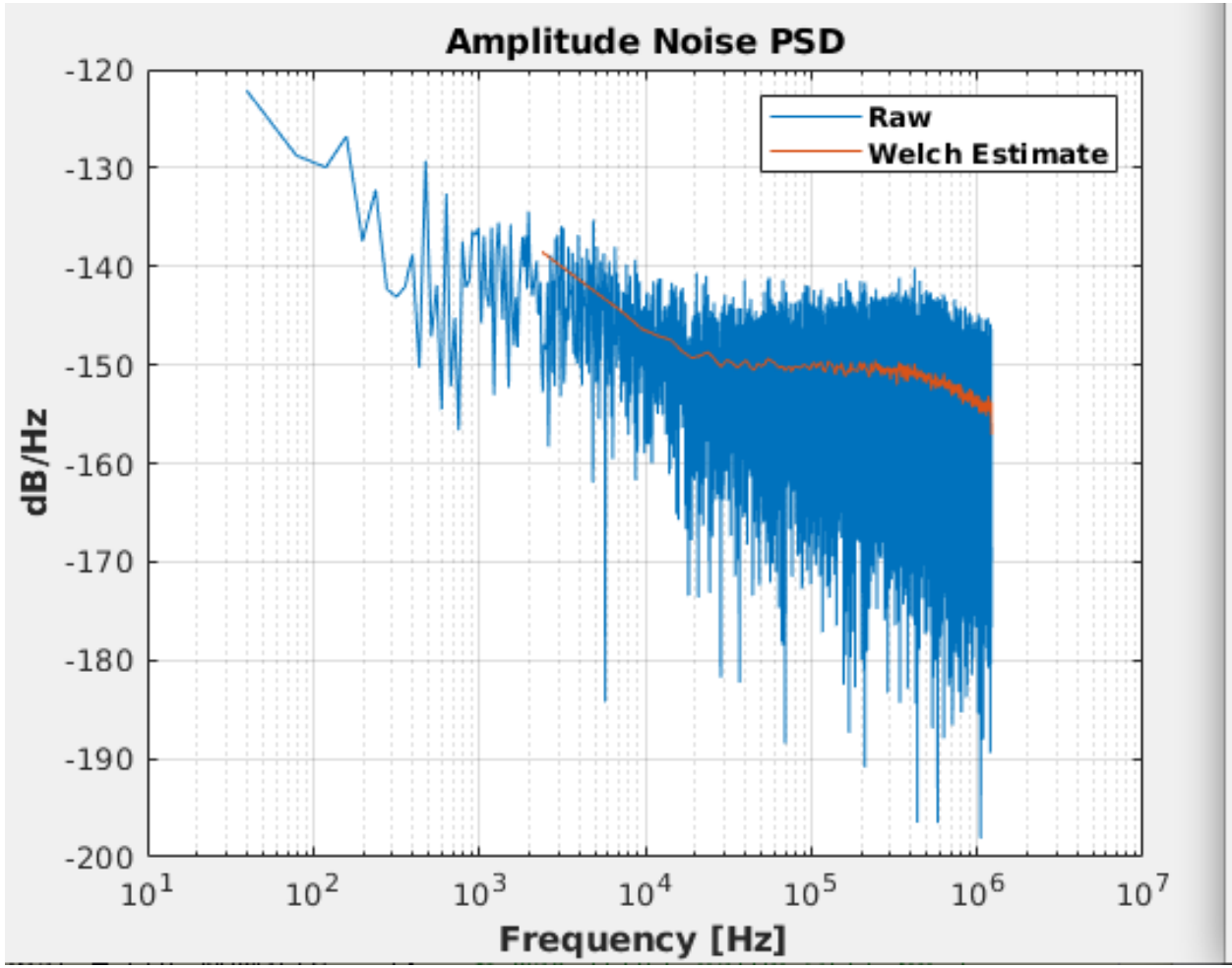
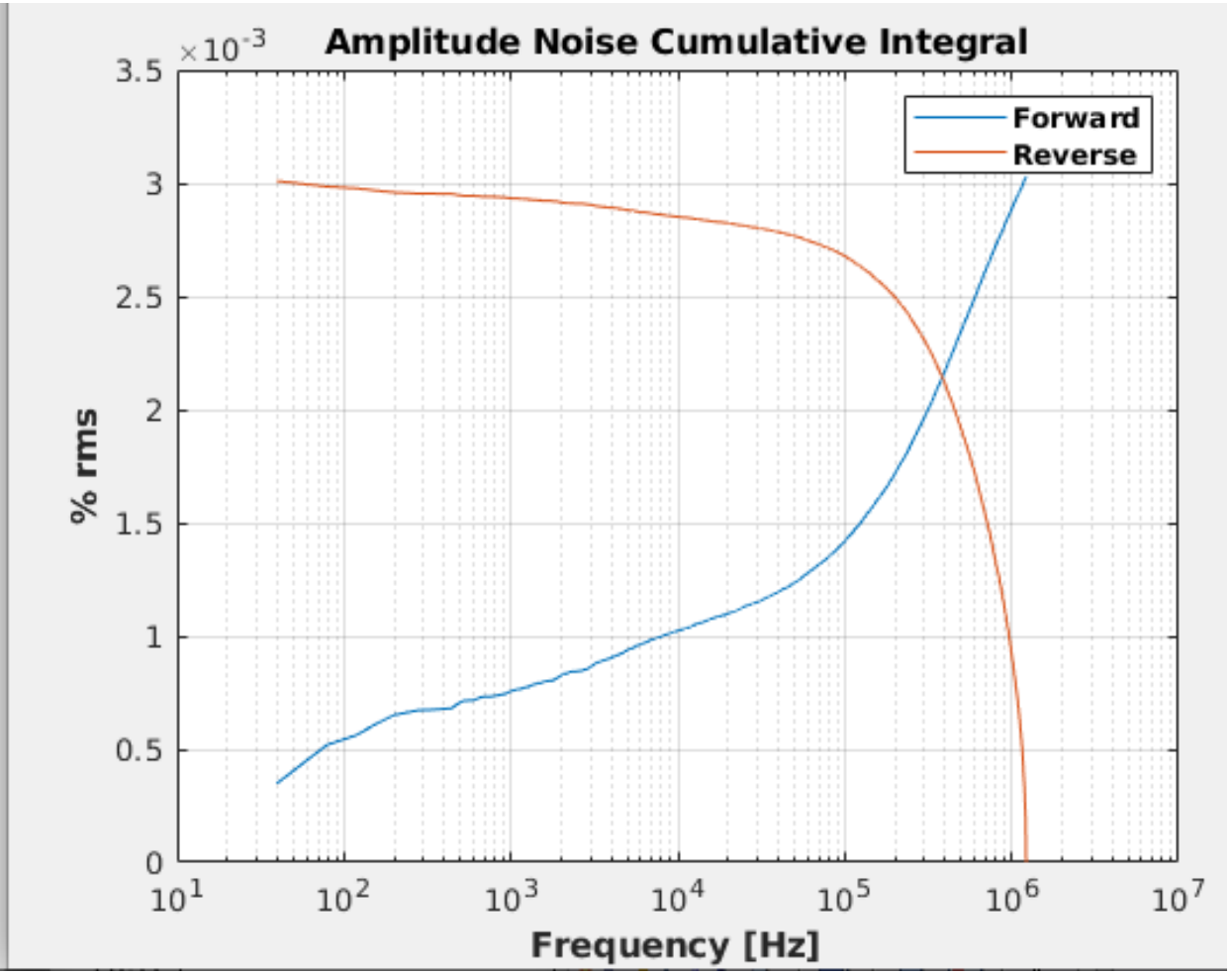




Component Evaluations – LTC2107 ADC

@ -2.9 dBFS input





Component Evaluations – LTC2000-16 DAC

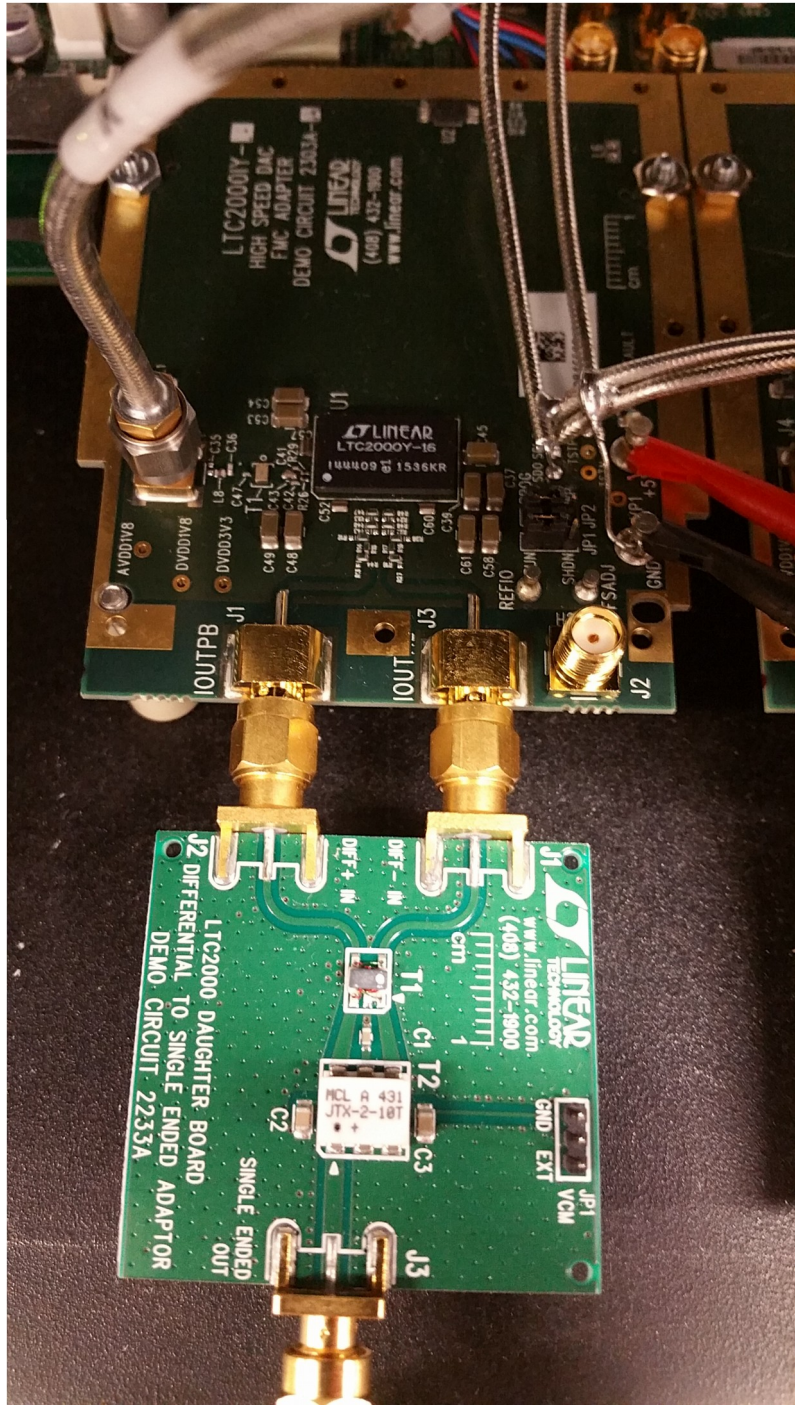
(16-bit, 2.5GSPS, 80dBc SFDR, latency=7.5 cycles)

- Intent for DAC to support both LLRF and new RF source for Booster-to-Storage Ring Timing/Synchronization

- LTC2000-16 Eval Board (DC2303A)
- DC2233A differential to single ended adapter board

- SMA100A source = 328MHz => DDS clock = 164MHz
- DDS output frequency = ~ 23 MHz

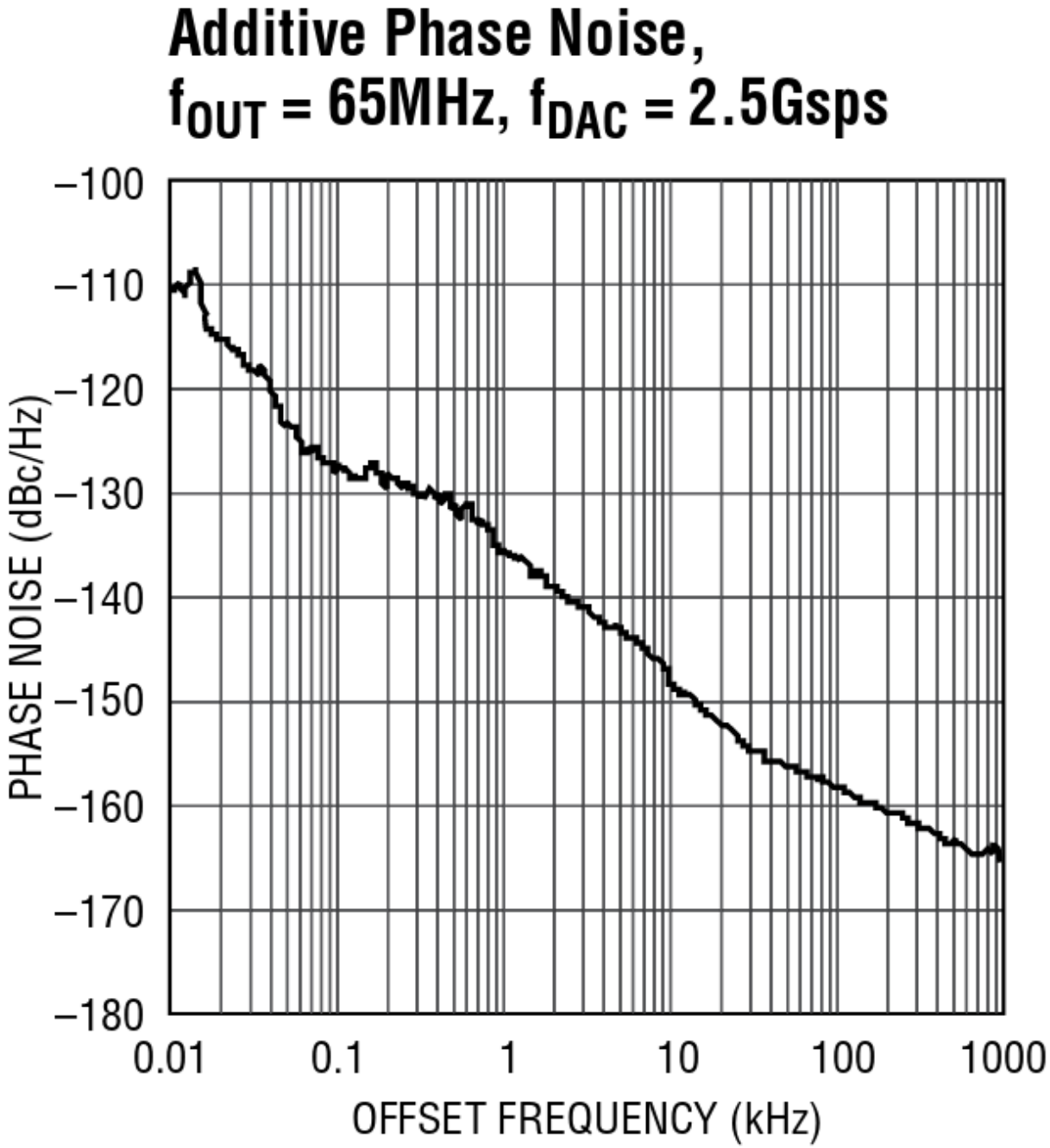
- Measured absolute phase noise with an Agilent E5052B (see following slides) to extract residual phase noise info



LTC2000-16 Datasheet

- **Only known DAC with phase noise data in its datasheet !**

- Integration of this data is **~ 66 fsec rms** (10Hz – 1MHz)

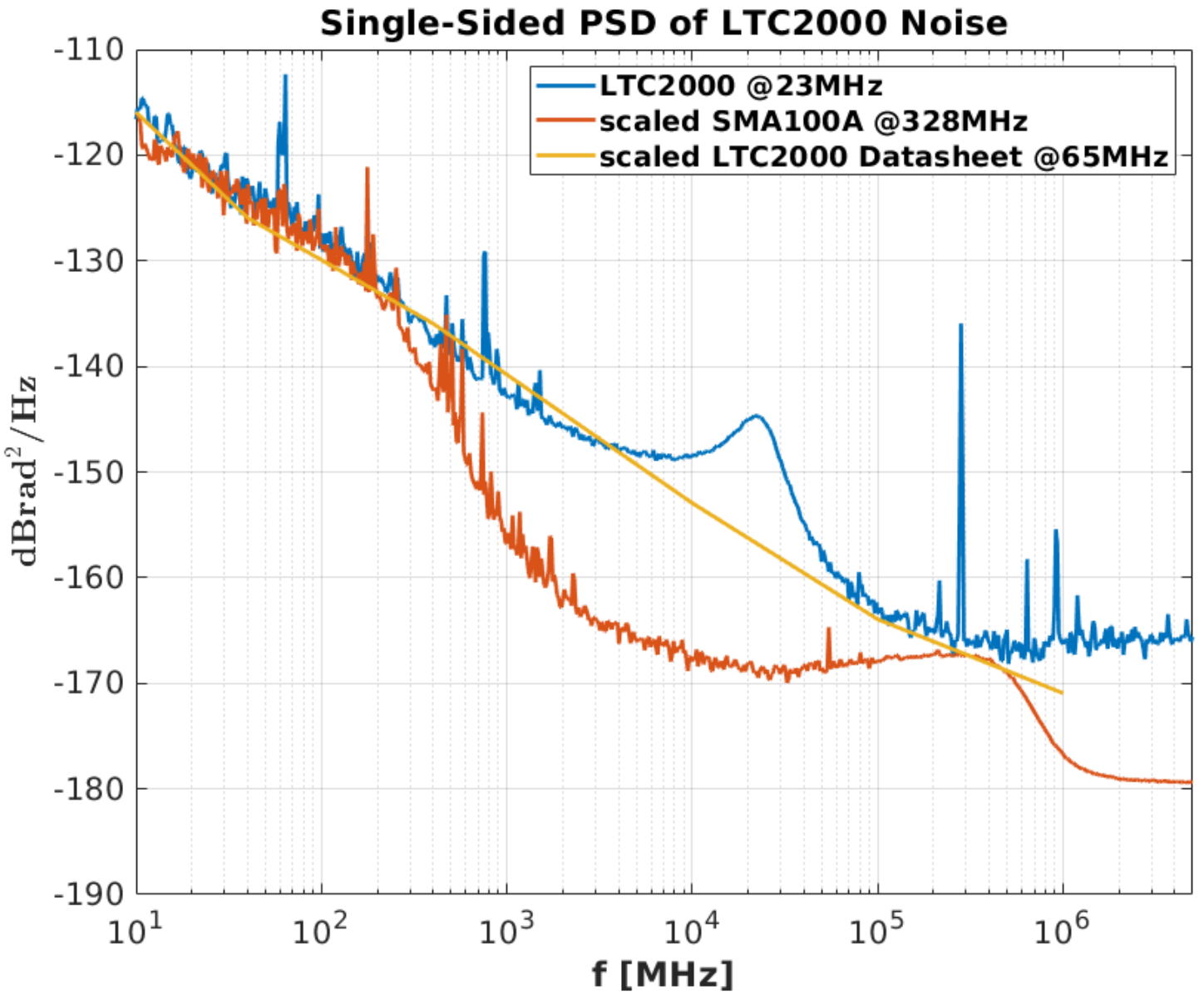


Measurement of LTC2000 Eval Board

- SMA100A measurements at 328MHz were scaled to 23MHz, i.e., 20*log10(23/328)
- LTC2000 meas. matches scaled datasheet except for bump near 20kHz. This is due to regulators on eval board

  … spur at 300kHz = -100dBc (switcher??)
- SMA100A jitter = **56 fsec rms**
- LTC2000 datasheet = **66 fsec rms**
- **rms sum = 86 fsec rms**
- LTC2000 Eval = **126 fsec rms**

  => Eval adds = ~ 90 fsec rms



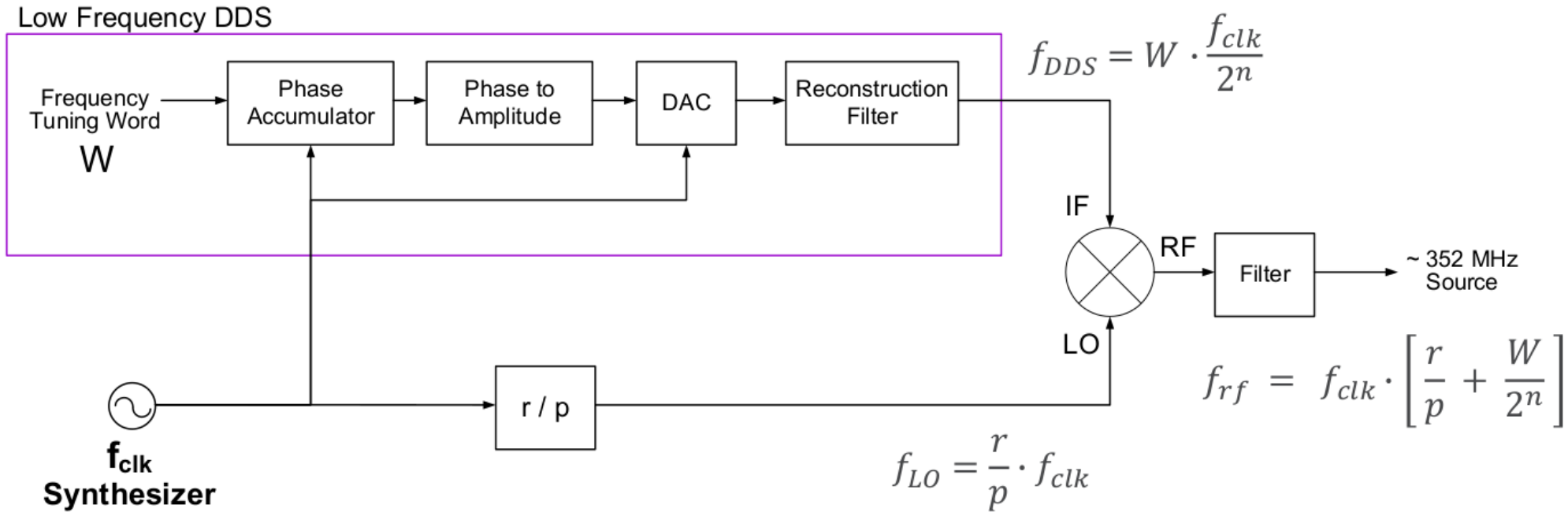
Plans for new RF Source

Plans for new RF source

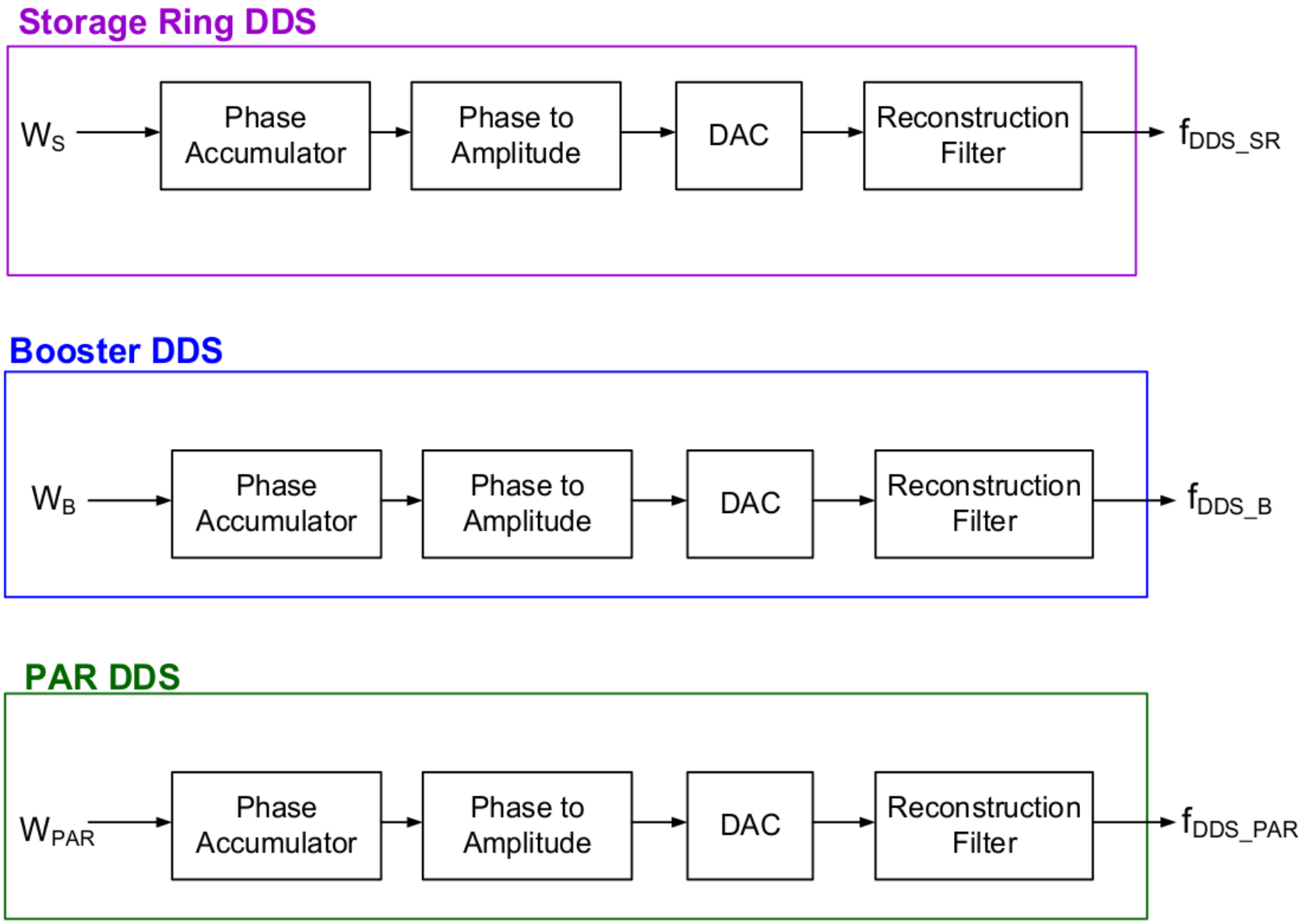
- Storage Ring circumference is reduced for new lattice → higher frequency
- Booster circumference is staying fixed → unequal frequencies

$$f_B = f_{SR}\left[1 - \frac{m(t)}{N_i N_e}\right]$$

- High charge operation in Booster requires momentum / frequency sweep
  - Close to on-momentum injection for efficiency, extract off-momentum to reduce emittance
- Solution → DDS based source shown below (similar to standard digital LLRF DDS + up-converter) with proper numerology to achieve desired results, p=power of 2 ensures tuning word = integer

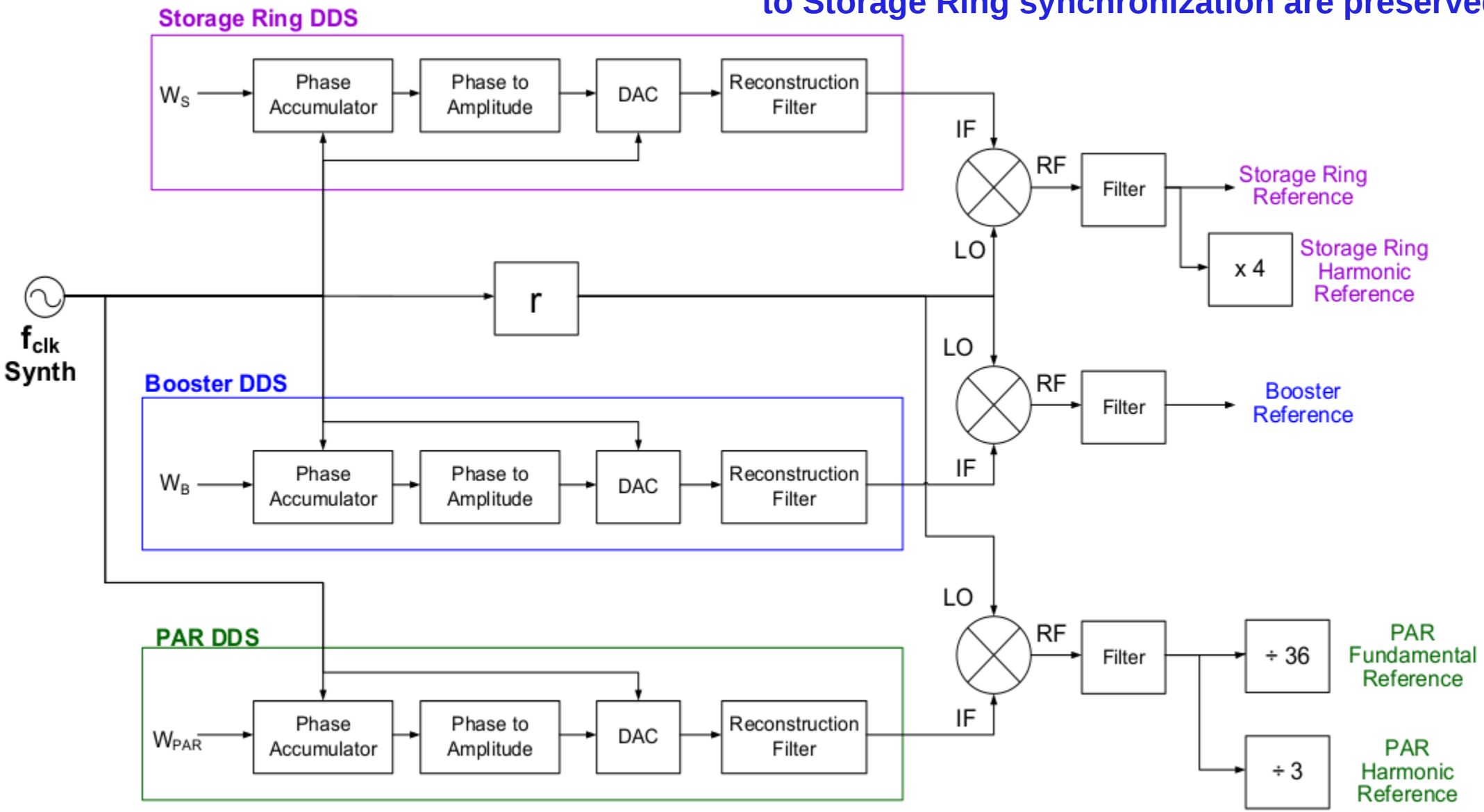


Plans for new RF source

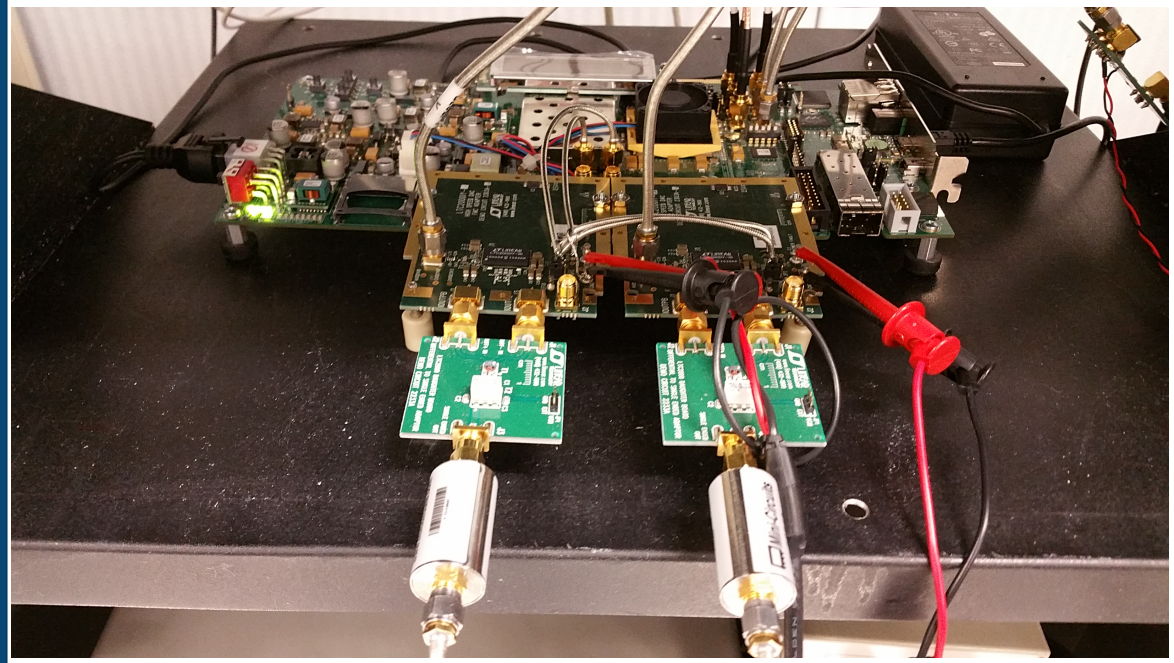


Plans for new RF source

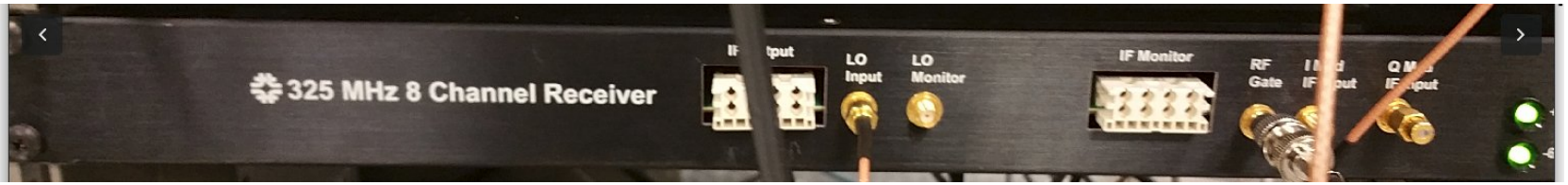
For Slow Orbit feedback in the Storage Ring, tune the master synth and all rational relationships for Booster to Storage Ring synchronization are preserved



Plans for new RF source



- DDS is being developed under APS-U Timing/Synchronization System (led by **Tom Fors**) which includes timing fiducials as well
- DDS development by **Dan Paskvan**
- Fermilab AFE design will be used for up-conversion
- Original momentum sweep algorithms developed by **Uli Wienands**.
- Fixed rational relationship proposed by **Bob Hettel**



Conclusion

- Digital LLRF based on uTCA platform is being used for the APS-U upgrades
  - tests performed on PAR, first BLS tests by end of year
- Vibrant and productive collaboration with Eric Breeding and Klemen Vodopivec from SNS, also benefitting from using Fermilab Analog Front End design
- Will use FMC based approach over RTMs, key components chosen
- Common platform will be used through all systems
- DDS based design with proper numerology supports Booster to Storage Ring synch.
  - development by Dan Paskvan
- Mature firmware and software (see T. Madden's talk next)

Thanks for your attention ！