ICEBERG Firmware Effort
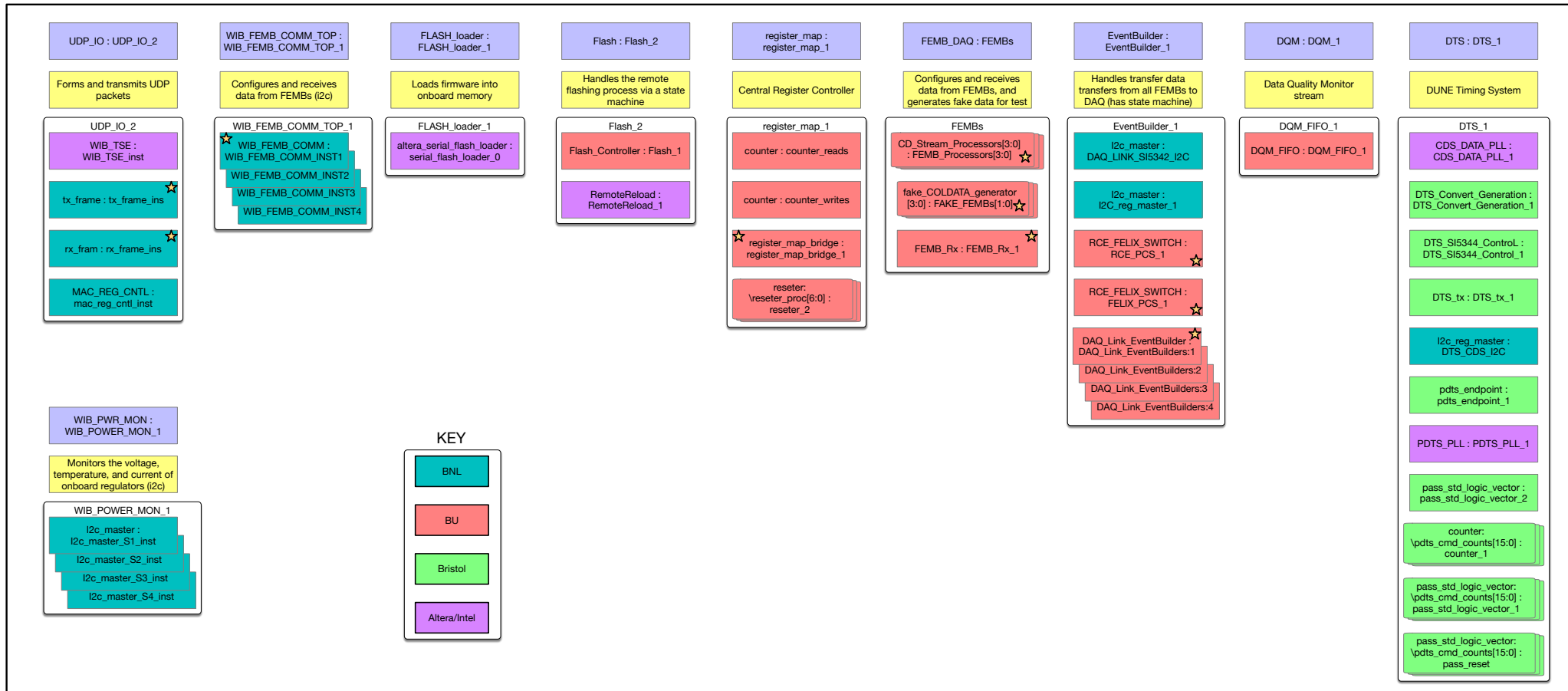
Goals:

- Test COLDATA functionality
- Test CRYO functionality
- Start of development of DUNE-relevant WIB firmware

WIB_TOP

UDP_IO : UDP_IO_2

Forms and transmits UDP packets

UDP_IO_2
- WIB_TSE : WIB_TSE_inst
- tx_frame : tx_frame_ins ☆
- rx_fram : rx_frame_ins ☆
- MAC_REG_CNTL : mac_reg_cntl_inst

WIB_FEMB_COMM_TOP : WIB_FEMB_COMM_TOP_1

Configures and receives data from FEMBs (i2c)

WIB_FEMB_COMM_TOP_1
- ☆ WIB_FEMB_COMM : WIB_FEMB_COMM_INST1
- WIB_FEMB_COMM_INST2
- WIB_FEMB_COMM_INST3
- WIB_FEMB_COMM_INST4

FLASH_loader : FLASH_loader_1

Loads firmware into onboard memory

FLASH_loader_1
- altera_serial_flash_loader : serial_flash_loader_0

Flash : Flash_2

Handles the remote flashing process via a state machine

Flash_2
- Flash_Controller : Flash_1
- RemoteReload : RemoteReload_1

register_map : register_map_1

Central Register Controller

register_map_1
- counter : counter_reads
- counter : counter_writes
- ☆ register_map_bridge : register_map_bridge_1
- reseter: \reseter_proc[6:0] : reseter_2

FEMB_DAQ : FEMBs

Configures and receives data from FEMBs, and generates fake data for test

FEMBs
- CD_Stream_Processors[3:0] : FEMB_Processors[3:0] ☆
- fake_COLDATA_generator [3:0] : FAKE_FEMBs[1:0] ☆
- FEMB_Rx : FEMB_Rx_1

EventBuilder : EventBuilder_1

Handles transfer data transfers from all FEMBs to DAQ (has state machine)

EventBuilder_1
- I2c_master : DAQ_LINK_SI5342_I2C
- I2c_master : I2C_reg_master_1
- RCE_FELIX_SWITCH : RCE_PCS_1 ☆
- RCE_FELIX_SWITCH : FELIX_PCS_1 ☆
- DAQ_Link_EventBuilder : DAQ_LINK_EventBuilders:1 ☆
- DAQ_Link_EventBuilders:2
- DAQ_Link_EventBuilders:3
- DAQ_Link_EventBuilders:4

DQM : DQM_1

Data Quality Monitor stream

DQM_FIFO_1
- DQM_FIFO : DQM_FIFO_1

DTS : DTS_1

DUNE Timing System

DTS_1
- CDS_DATA_PLL : CDS_DATA_PLL_1
- DTS_Convert_Generation : DTS_Convert_Generation_1
- DTS_SI5344_ControL : DTS_SI5344_Control_1
- DTS_tx : DTS_tx_1
- I2c_reg_master : DTS_CDS_I2C
- pdts_endpoint : pdts_endpoint_1
- PDTS_PLL : PDTS_PLL_1
- pass_std_logic_vector : pass_std_logic_vector_2
- counter: \pdts_cmd_counts[15:0] : counter_1
- pass_std_logic_vector: \pdts_cmd_counts[15:0] : pass_std_logic_vector_1
- pass_std_logic_vector: \pdts_cmd_counts[15:0] : pass_reset

WIB_PWR_MON : WIB_POWER_MON_1

Monitors the voltage, temperature, and current of onboard regulators (i2c)

WIB_POWER_MON_1
- I2c_master : I2c_master_S1_inst
- I2c_master_S2_inst
- I2c_master_S3_inst
- I2c_master_S4_inst

KEY
- BNL
- BU
- Bristol
- Altera/Intel

Rivera's Diagram

High-Level Work Breakdown

- Porting of existing firmware from Altera to Xilinx
- Removal of legacy firmware (e.g., RCE interface, COLDATA simulator)
- Implementation of Fast Command Interface
  - Not clear how this will be implemented end-to-end at ICEBERG
- Update to I2C interface for COLDATA (does this change?)
- Software tools updates
- CRYO Interface
- Update to power and monitoring
- Update to control register mapping
- Timing (?)
- Firmware loading (will this still be only via JTAG?)
- Anything else?

Path Forward

- Would be nice to get volunteers to work on particular IPs
- Will need at least one (warm) test stand available---WIB available soon
- Timeline is early 2020 for COLDATA tests
- Early Spring 2020 for CRYO tests
- Will need to coordinate via git as things progress
- Updates at bi-weekly(?) WIB meetings