DUNE ASICs Status and Plans

Marco Verzocchi
Fermilab
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ColdADC

- Work done mostly outside Fermilab
- Moved to test packaged parts at BNL/Uflorida
- Will be installed on FEMBs soon
- Additional testing of bare chip at BNL has highlighted source of non-linearity in the SHA
  - Caused by kickback from pipeline, disappears when ADC run at 500 KHz (needs to operate at 2 MHz)
  - Points out to area for improvement in next iteration

COLDATA

- All tests performed so far have been successful both at room and at LN_2 temperature
- Only 2 issues observed
  - If the first I2C operation performed from COLDATA on a ColdADC is a read command, the information from ColdADC is not relayed properly, need to make a 2nd read operation
  - At room temperature the PLL requires slightly higher voltage to lock compared to design (1.15-1.2V instead of 1.1V)
    - No problem at LN_2 temperature
- Additional issue observed on external component required by COLDATA
  - The MEMS oscillator requires large voltage at startup in LN_2
  - Voltage can be lowered for operation
  - May require small design change in COLDATA (provide additional external clock)
- Work done mostly by Scott Holm, David Christian, Xiaoran Wang (SMU)
- Next: data transmission tests and bit error rate measurements

Plans

- We are approaching the point where we want to restart some on ColdADC with the goal of a submission in late Spring 2020
- Followed quickly by 2nd iteration of COLDATA (minor fixes, possibly add capability of data transmission at 2.56 Gbit/s)

- As an aside:
  - SLAC has fixes for most of the problems observed in the first version of the CRYO ASIC
  - Will be ready to make a submission of the nEXO version of the ASIC as soon as the noise problem (160 KHz noise line observed) is understood and fixed
  - A 2nd version for DUNE will be submitted after system tests have been performed (ICEBERG TPC) using the nEXO version of the chip