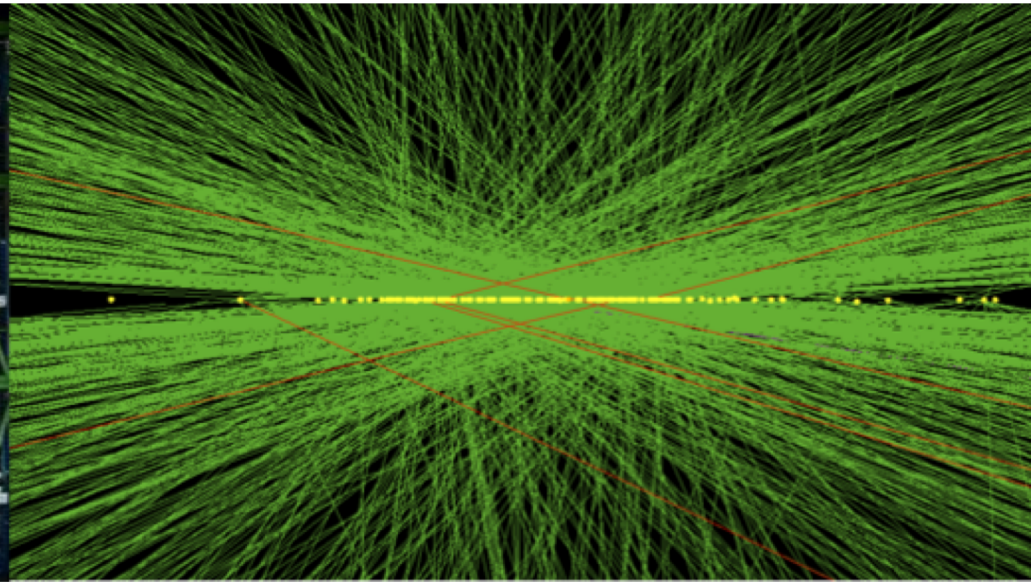
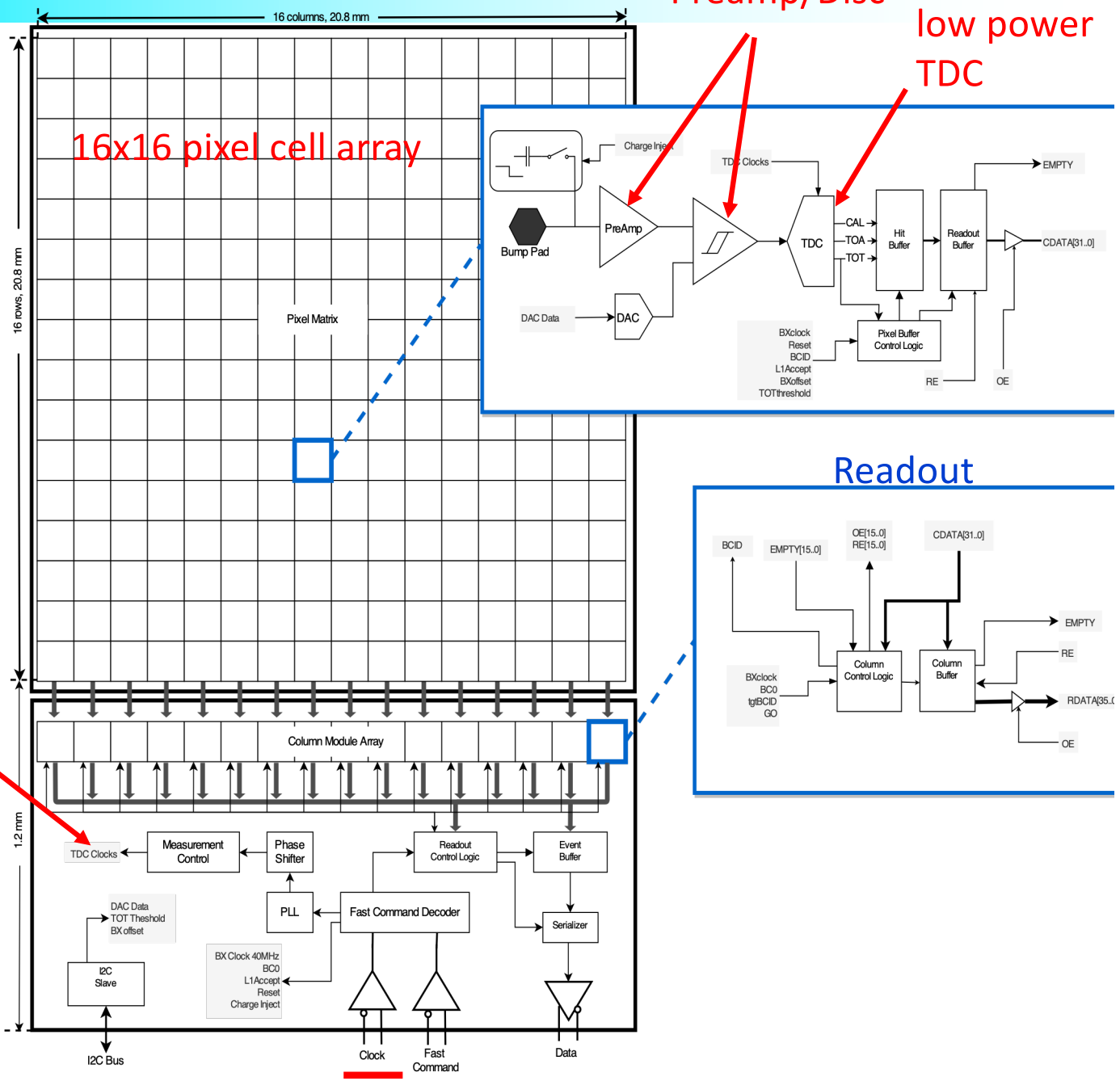
ETROC Plan

Ted Liu (FNAL)



ETROC Overview



clock distribution all the way into each pixel

ETROC Development: *divide & conquer*

ETROC0: 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

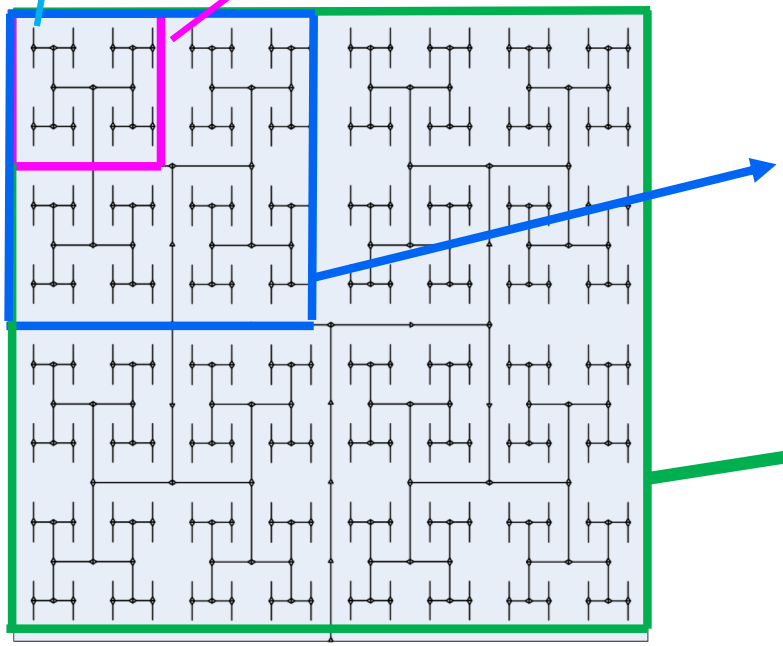
Goal: core front-end analog performance

the first prototype chip works well and agrees with simulation

ETROC1: 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

Goal: full chain front-end with TDC, 4x4 clock tree

This is the first full chain precision timing prototype



16 x 16 clock H-Tree

ETROC2: 8x8, *full functionality*, and ¼ clock tree (Q1 2021)

Goal: supporting circuitries, 8x8 clock tree

PLL, phase shifter, fast/slow control, I/O, L1 buffer…

ETROC3: 16x16 (full size): (Q1 2022)

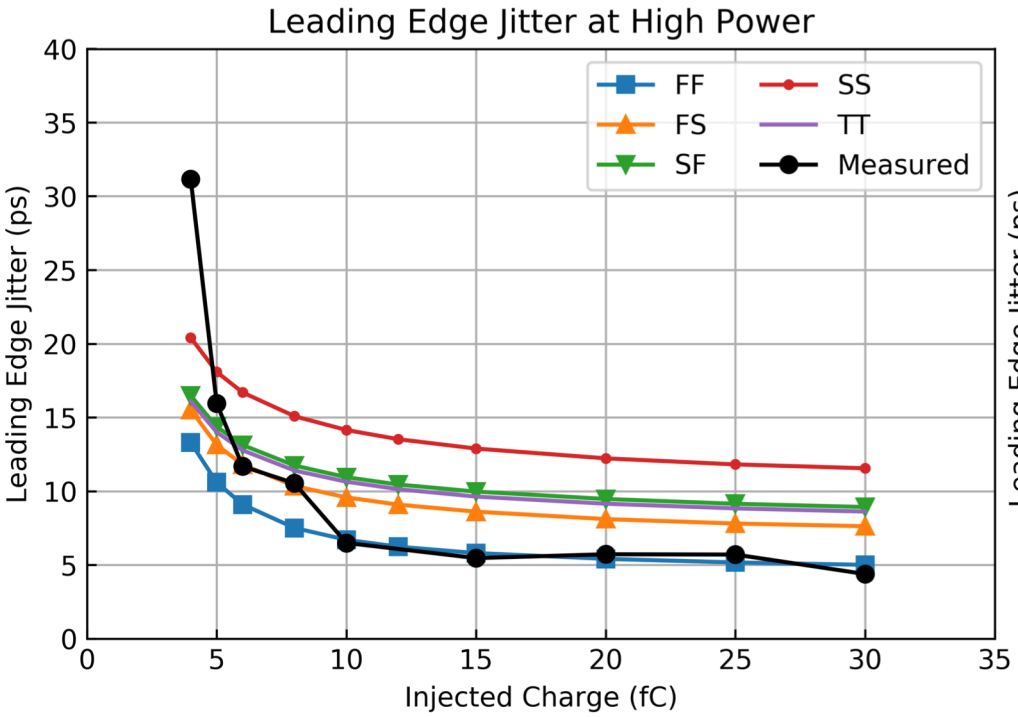
Goal: full size with full clock tree

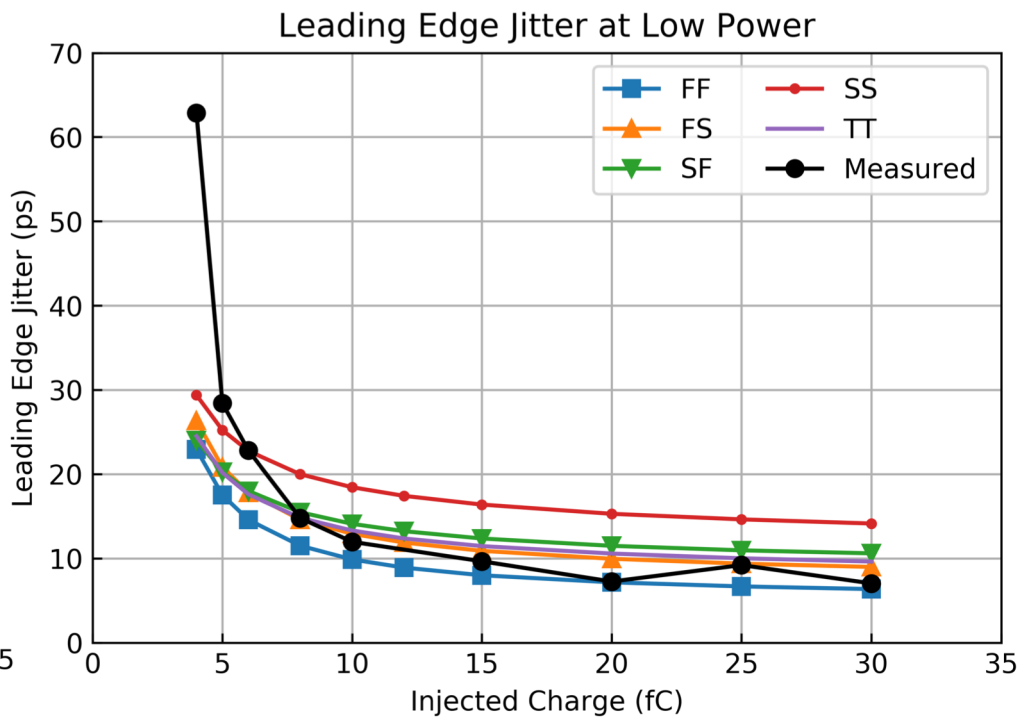
Production Q4 2022

Bottom-Up & Top-Down approach in parallel

ETROC0 jitter: measured vs simulation

ETROC0 post-layout simulation vs
testing results using 25ps risetime external pulse injection

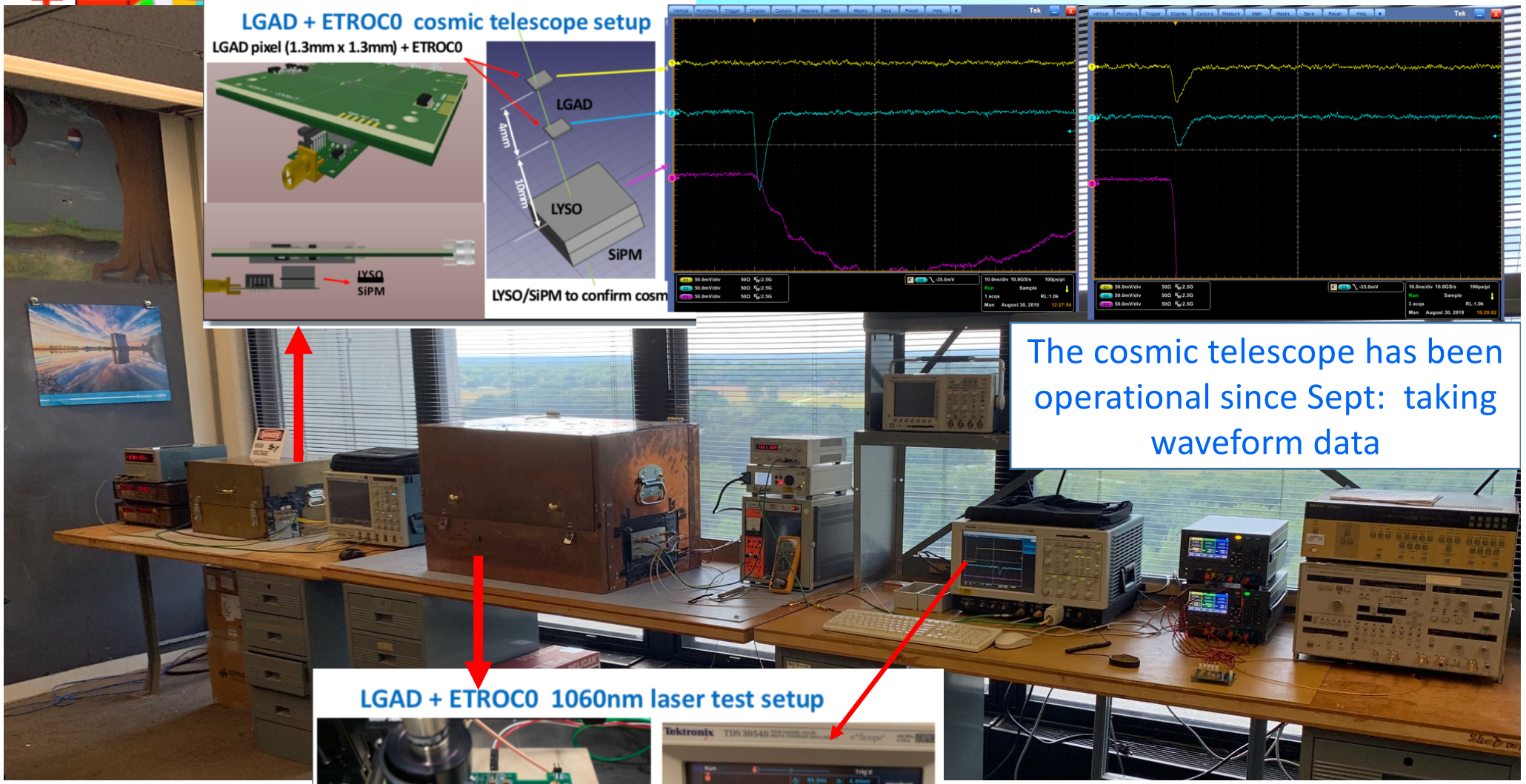




Jitter measurements agree with chip post-layout simulation

Power consumption for preamp and discriminator all match with simulation

LGAD+ETROC0 Test Stands at FNAL



The cosmic telescope has been operational since Sept: taking waveform data

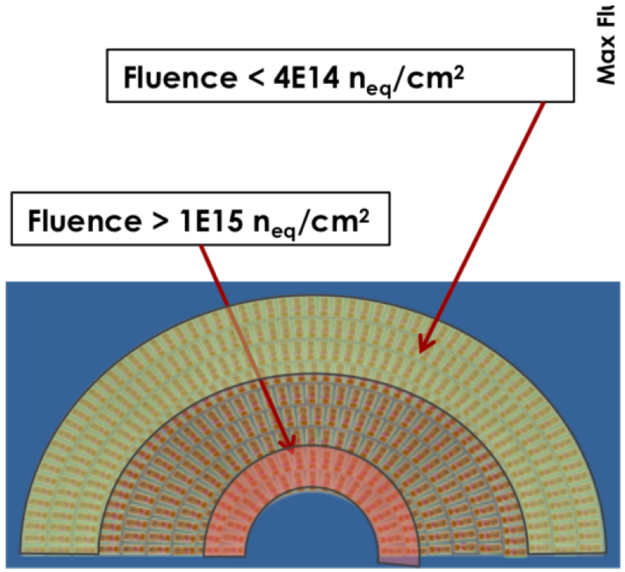
preparing for the upcoming beam test at FNAL (starting Dec 2019)

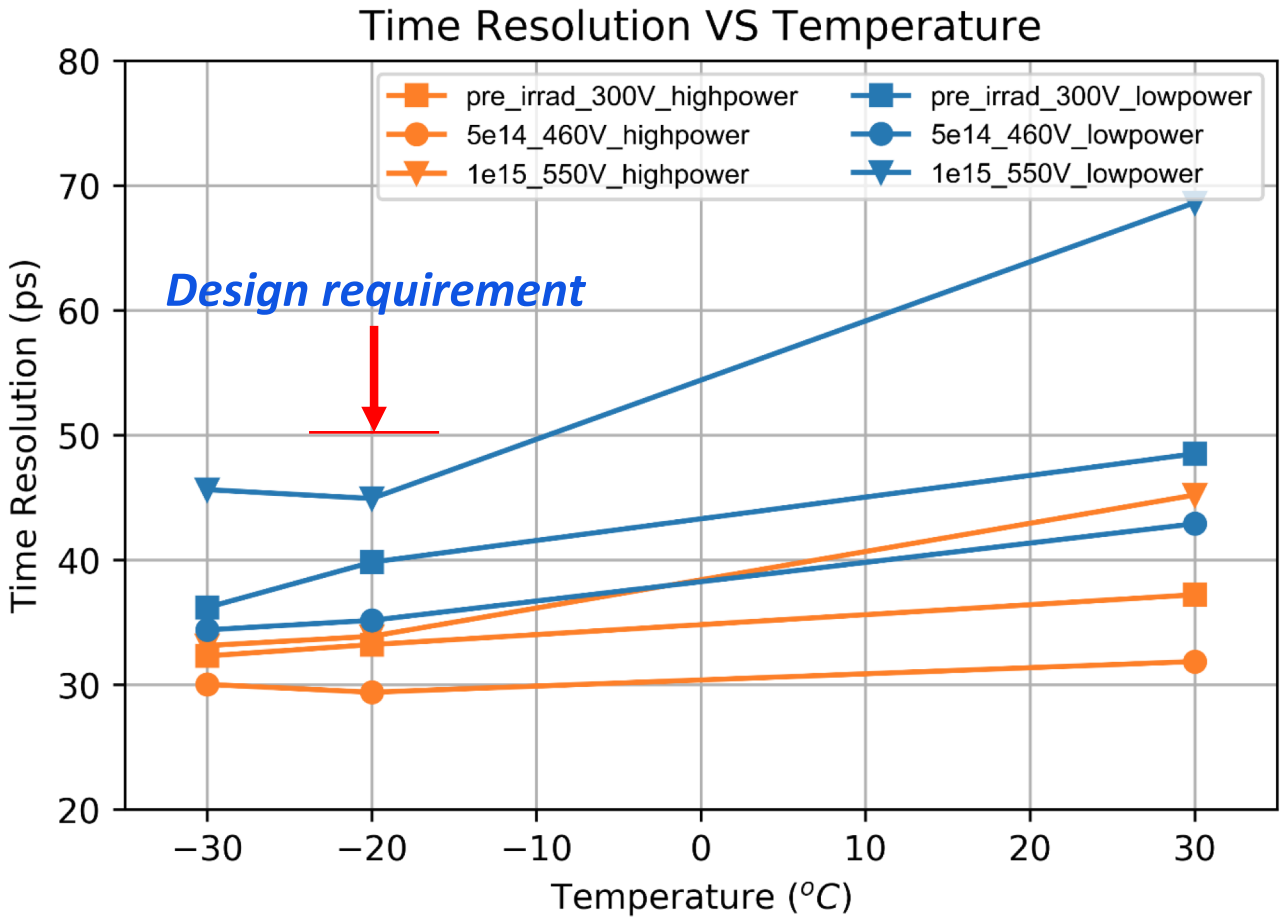
Full-chain post layout simulation: LGAD + Preamp + Disc

- Three irradiation levels for LGAD Sensor simulation: pre-irrad, 5e14, 1e15
  - Three representative cases of early, mid, late operations
- Two preamp bias current settings studied (low to high)
  - 0.35mA, 0.7mA, 1.05mA, 1.4mA

with preamp @ low power:
~ 35 ps @5e14

with preamp @ high power:
~ 35ps @1e15

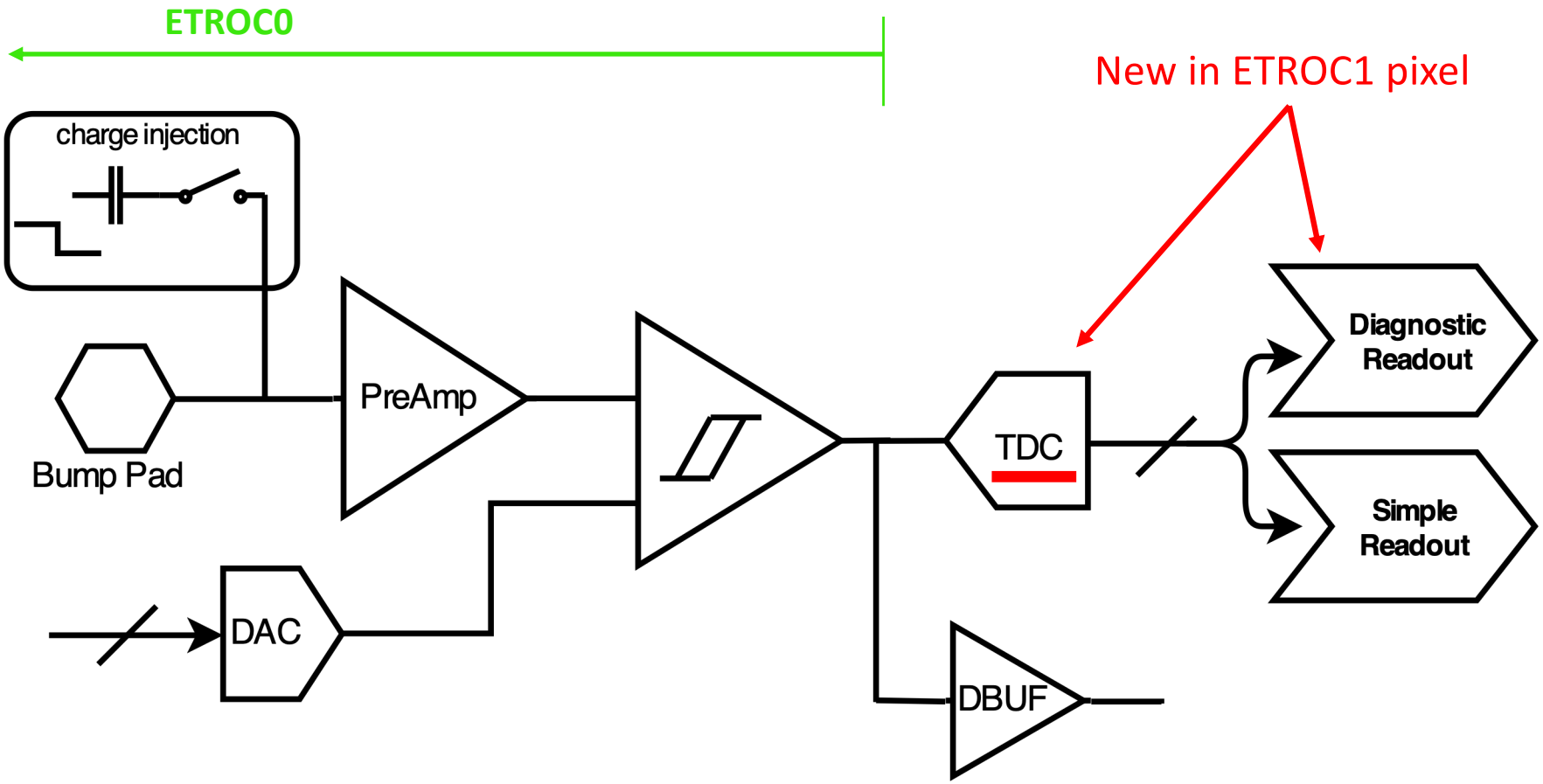




Post layout simulation results, to be validated in the upcoming beam test at FNAL (starting Dec 2019)

ETROC1 pixel: uses ETROC0 front-end

ETROC0 performance is as expected, it is used directly in ETROC1

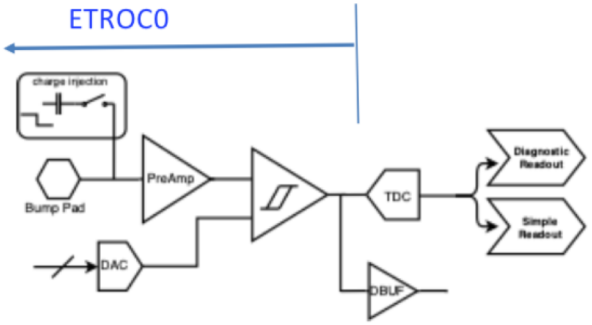


The TDC is brand new design (low power)
~ one year development effort

ETROC1 TDC Design

- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

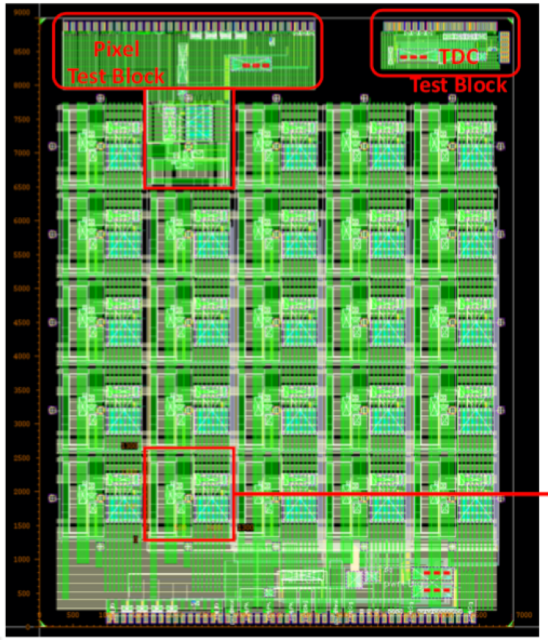
ETROC0



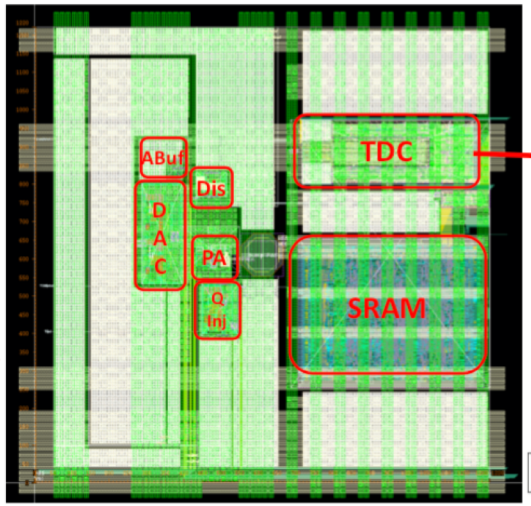
Extensive design verification has been done, mostly by EE students.

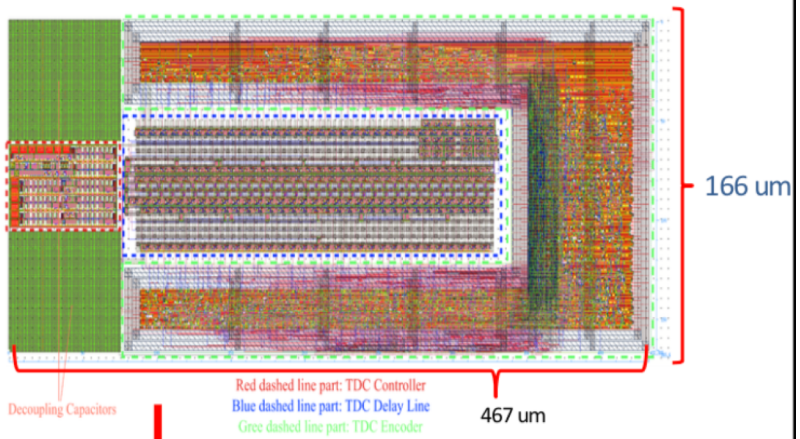
Low power TDC: <0.1mW

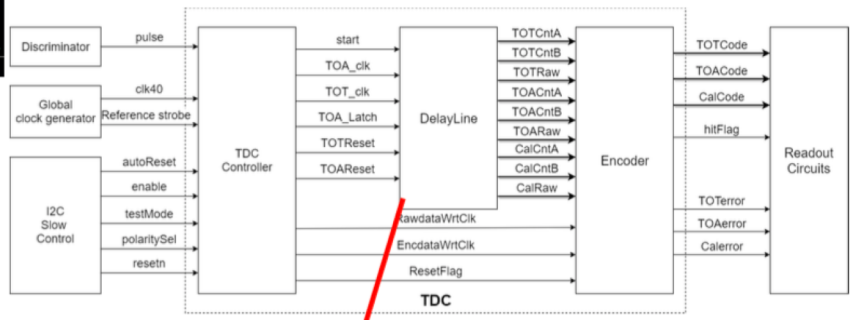
ETROC1 Top Layout



ETROC1 Single Pixel Layout





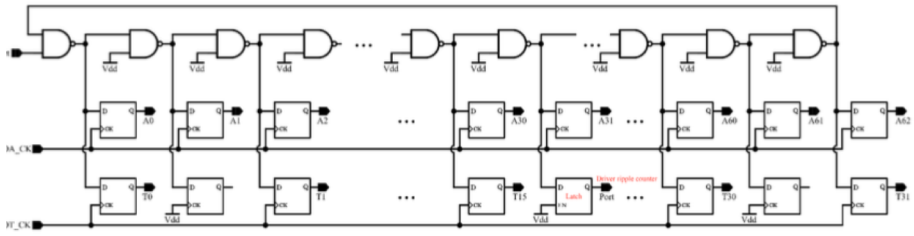


God-parent reviews in May and July 2019

ETROC1 submitted on time (Aug 28, 2019)

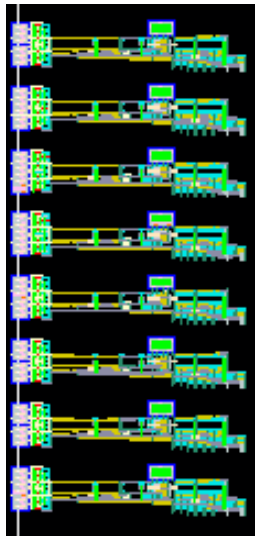
Expect chip delivery end of Nov 2019

TDC core logic: gated ring oscillator



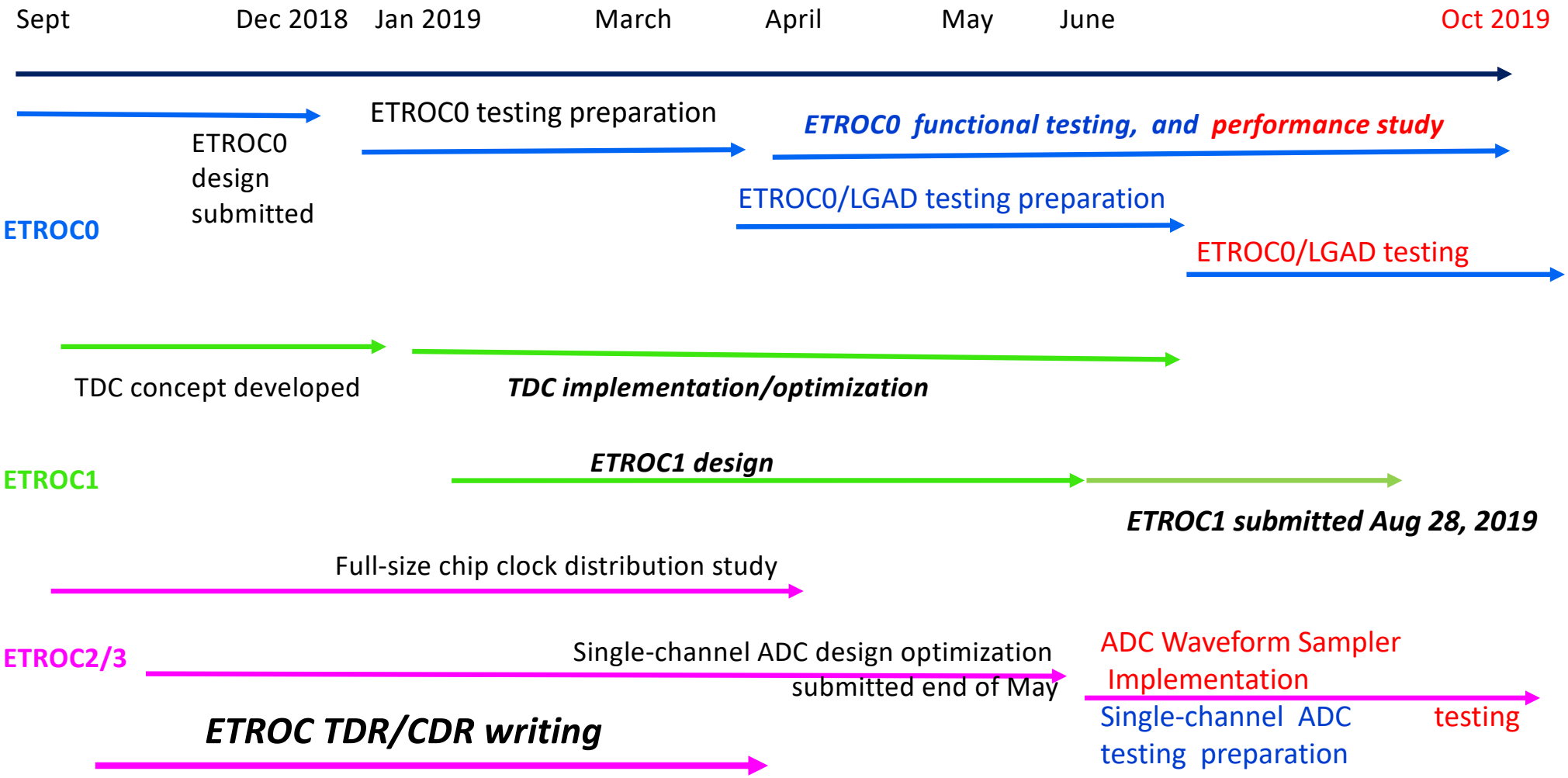
ETROC2&3: already on going

- ETROC specification has been fully developed (CDR)
  - Most critical components implemented in ETROC0&1
- Full-chip clock distribution design study done
  - The textbook H-tree clock distribution works well
- Waveform sampling spec and design developed
  - For monitoring and calibration
  - Single channel ADC prototype received, works well
  - The core 2.56 GS/s waveform sampler at post-layout simulation stage
- The rest of supporting circuitries will be based on existing design blocks in 65nm from CERN



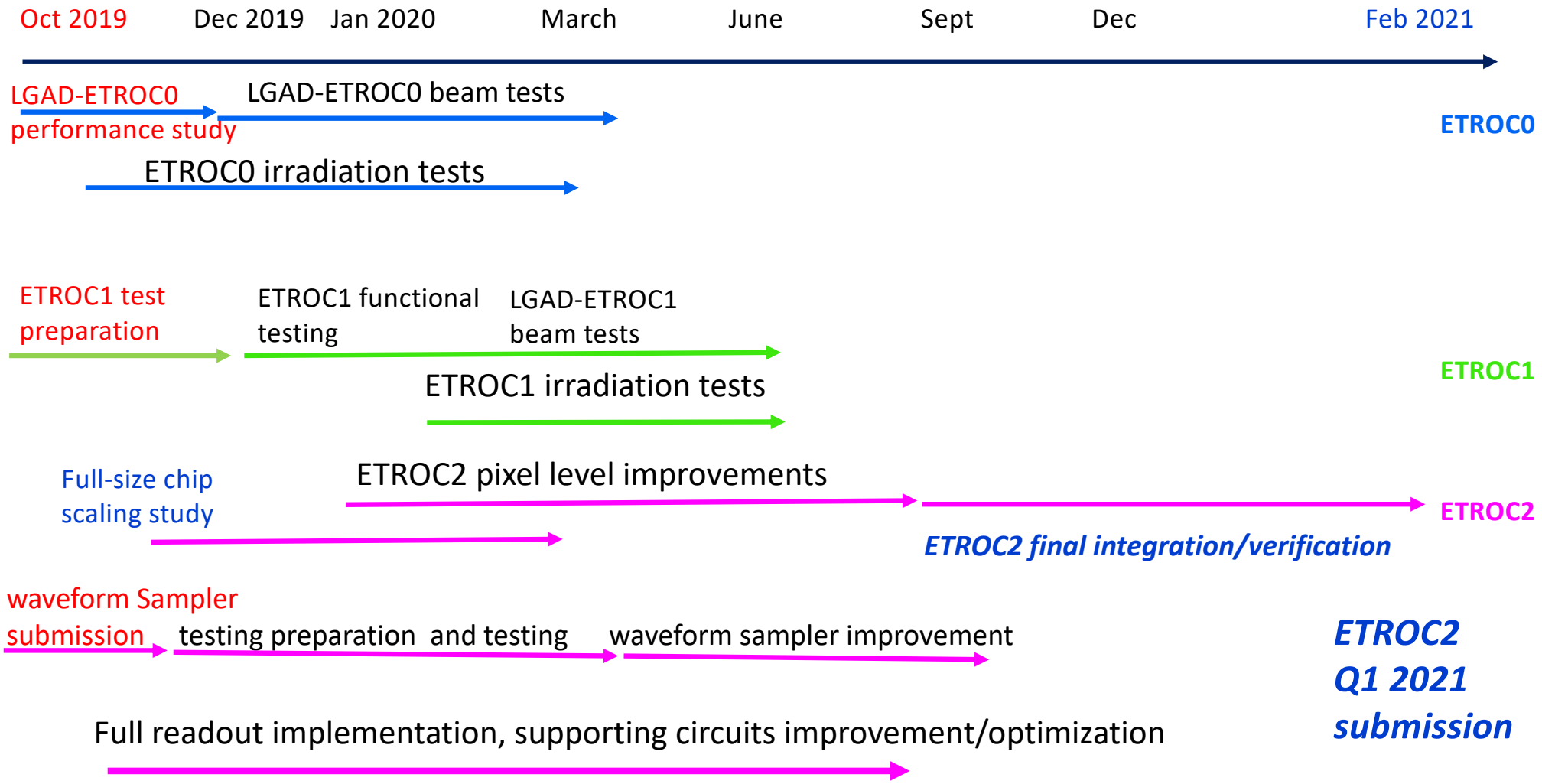
Area of
300um * 800um

ETROC activities over the past year (current activities)



Past year: making rapid progress with a strong team, proceeding just as we planned

Towards ETROC2 (current activities)



From ETROC2 to ETROC3

Feb 2021 March — June — Sept — Dec — March 2022

ETROC2

testing preparation → functional and beam tests → **ETROC2**

ETROC2 irradiation tests

ETROC3 pixel level improvements

supporting block improvements

Full-size chip initial Implementation & verification → **ETROC3**

ETROC3 optimization/verifications

Main task: design verification & verification

ETROC3 March 2022 submission