ECON ASICs

Jim Hirschauer, Ralph Wickwire

ASICs PMG

14 Oct 2019

Re-organization

- Ralph Wickwire takes over as Co-coordinator / Lead engineer after departure of Gregory.
  - Jim Hoff / Paul Rubinov continually consulted, as well.
  - Advantages / disadvantages of new organization ...

Team summary

- **Hirschauer (50%) :** 15+ yrs HEP / 5+ yrs Upgrade Coordination experience
  - ***Co-coordinator****: specification, ASIC and system architecture*
- **Ralph (100%)** : 15+ yrs digital experience in ASIC industry
  - ***Co-coordinator****: specification, ASIC architecture, top-level chip integration, RTL for some blocks*
- **Rubinov (20%) :** 20+ yrs system/PCB/FPGA experience & HGCAL system design
  - *Specification, ASIC and system architecture*
- **Sandeep (60%)** : 5+ yrs digital design experience
  - *Coordinate implementation (RTL ➔ physical design) and integrate lpGBT 1.28 Gbps receivers*
- **Davide (40%)** : 10+ years of mixed signals design experience
  - *Design 1.28 Gbps transmitters and integrate lpGBT PLL*
- **Mike (40%)** : 40 years digital design experience
  - *RTL for various blocks and implementation*
- **Hoff (80%)** : 20+ yrs digital design and verification experience
  - *Coordinate verification*
- **Cristian (60%)** : 20+ yrs verilog/HDL experience
  - *Verification*
- **Alpana (30%)**: 10+ yrs in ASIC design support
  - *Tools support, RTL, implementation, and verification*
- **University of Split /FESB, Croatia:** 3 elec eng faculty with verilog and synthesis experience
  - *RTL for ECON algorithms*
- **LLR, Paris :** Electrical engineer and physicist with verilog experience
  - *RTL for ECON algorithms*
- **FNAL, Florida Tech University, Northwestern University :** Scientist, 2 post docs, 2-4 students
  - *Specification and verification*

Color code

- **ASIC design**
- **Verification**
- **External RTL design**
- **Specification, architecture, support**

Recent activities

- Weekly "**ECON One-hour Round Table**" (Tuesday, 3pm) is proving productive and efficient.
- **ECON-T algorithm studies** concluded in Sep 2019, as planned.
    - we will implement all three algorithms in ECON-T
    - possible use cases :
        - (a) **threshold** algo in all HGCAL
        - (b) **super trigger cell** algo in HCAL + **best choice / sorting** algo in ECAL

- **Wickwire and Hirschauer** continue to make good progress on adding increasingly more detail to specification.
- **Jim Hoff and Cristian Gingu** continue to make excellent progress on **UVM package and plan.**
- **Davide Braga** has started work on 1.28 Gbps transmitter
- **Mike Hammer** starting work on verilog for latency management state machine
- **Split/LLR** have started work on **best choice / sorting** algorithm verilog
- **Alpana** is working on block synthesis for Switch Matrix -- will be redone by Sandeep during integration
- **ePortRx + Word Aligner implementation work stalled**
- **Integration of lpGBT PLL is uncovered – Gregory was responsible**

Recent implementation resource allocation

Report	ECON	ETROC	RD53	CDP1 paper	Cold ADC v2
June 10	25%	25%	25%		25%
July 8	25%	25%	25%		25%
Aug 9	25%	60%	15%		
Sep 9	25%	35%	15%	25%	

Milestones (1)

	1-Aug	15-Aug	1-Sep	15-Sep	1-Oct	15-Oct	1-Nov	15-Nov	1-Dec	15-Dec	1-Jan
UVM track		Start building UVM Test bench			Basic TB passing data	UVM test plan document complete	Physics data prepared for simulation **				
Verilog / Design track				Start extracting PLL from full custom block	EportTx design Start			Finish extracting PLL from full custom block		EportTx design Done	Start Latency Management Verilog
Integration track	Integrate Word Aligner, Fast Command, I2C into ECON-Top					All blocks (some empty) instantiated in EConT top and data flowing.	Start review/ modification of lpGBT RTL for EConT specific use		Complete review and correct functionality in EConT top (from top lpGBT laid out)	PLL integrated	ePortTx integrated
Physical design track	Complete library characterization for radiation corners		Start Full Implementation of ePortRx digital		Complete full Implementation of ePortRx digital	Start review of ePortRx analog functionality and layout		Complete review of ePortRx analog functionality and layout		ePortRx analog + digital layout complete	
Algorithm track	Preliminary Algo plan **				Final algorithm choice **		Algo spec complete **			Algo Verilog complete	
Review and Sign-off Track				EConT & specification reviewed with CERN.				EConT & specification reviewed with CERN.			

Hoff
Gingu
Wickwire
Miryala
Hammer
Unknown
Deptuch
Hirschauer/ Noonan **
Noy ***
All

Milestones (2)

	15-Jan	1-Feb	15-Feb	1-Mar	15-Mar	1-Apr	15-Apr	1-May	15-May	1-Jun	15-Jun
UVM track	Algo tested standalone with physics data		LM tested		System sim initiated with CERN team ***				UVM final signoff		
Verilog / Design track		Latency Management implemented in Verilog									
Integration track	Algo integrated		LM integrated								
Physical design track	Initial Floor plan complete	Start buffer PD		Complete buffer PD	Start Algo + LM PD		Finish Algo + LM PD		Top level PD done		
Algorithm track											
Review and Sign-off Track		EConT & specification reviewed with CERN.				EConT & specification reviewed with CERN.			System sim passing data & interfaces understood.***	Signoff review done	Submit

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Noy ***
All

- Sandeep has completed library characterization for new radiation models.

Homework

- **Meeting with SCD** for bringing software expert into ASIC verification effort.
  - Hirschauer followed up with Liz + JimA; they proposed a few names (with associated skill sets) and received Hirschauer's feedback.
  - Next step is to plan meeting(s) with Hoff and two candidates.

Additional material

Sep 9 ECON status

Color map	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx							0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	20.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134

- For next PMG : will adjust Status Matrix to improve consistency with Milestones
- Yellow = 20% complete, green = 100%