Development of a hybrid amorphous selenium/CMOS charge sensor for the Selena neutrino experiment

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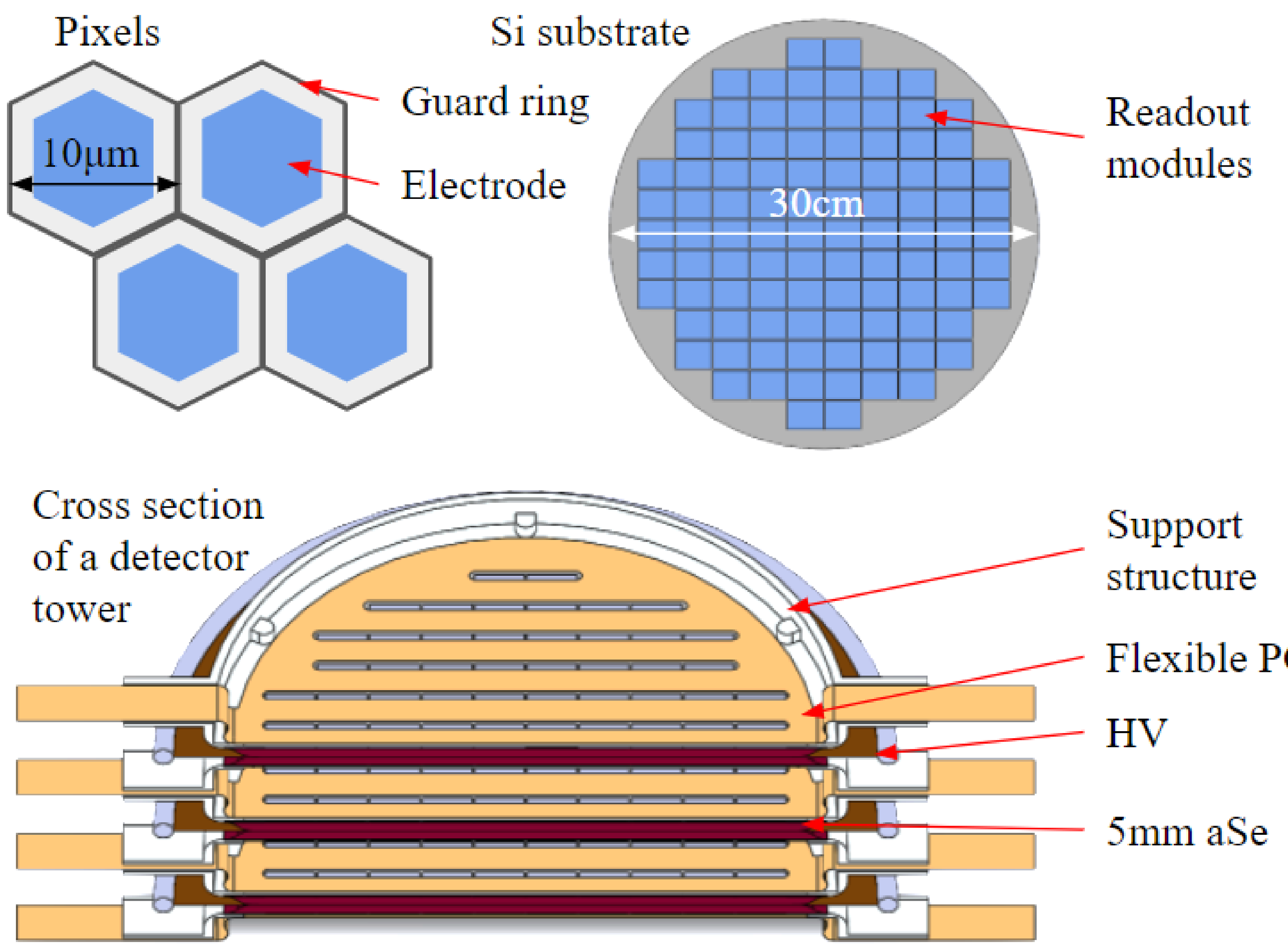
Introduction to Selena

The Selena Neutrino Experiment will utilize amorphous Selenium-82 (aSe) coupled to pixelated CMOS charge-sensing imagers to probe fundamental neutrino physics. The spatiotemporal resolution of CMOS imaging devices allow for unparalleled background rejection in neutrinoless double beta decay ($0\nu\beta\beta$) searches[3].



Conceptual design of the ton-scale Selena detector modules. Modularity allows for scaling up to the target mass of 10 ton of 95% ^{82}Se enriched aSe. High Voltage (HV) applied on each detector module drifts charge across the aSe onto the readout modules.

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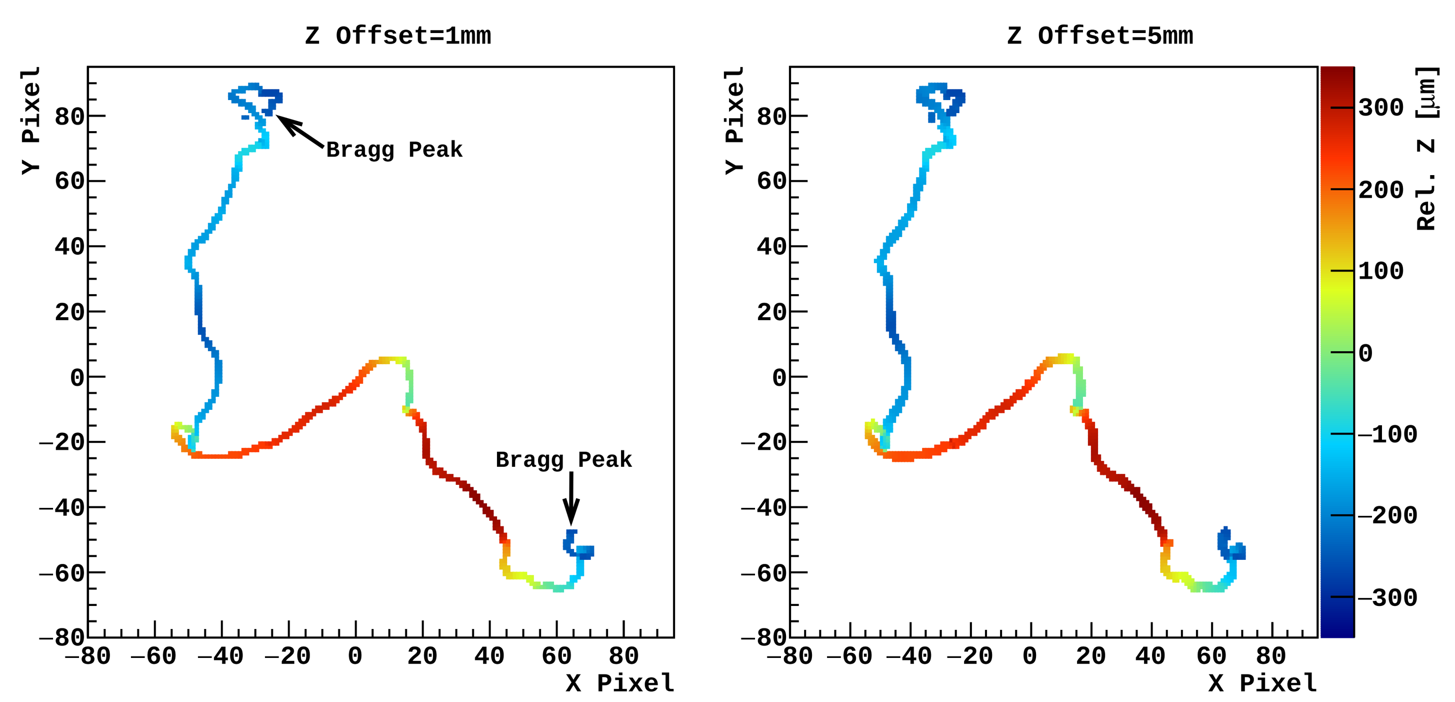
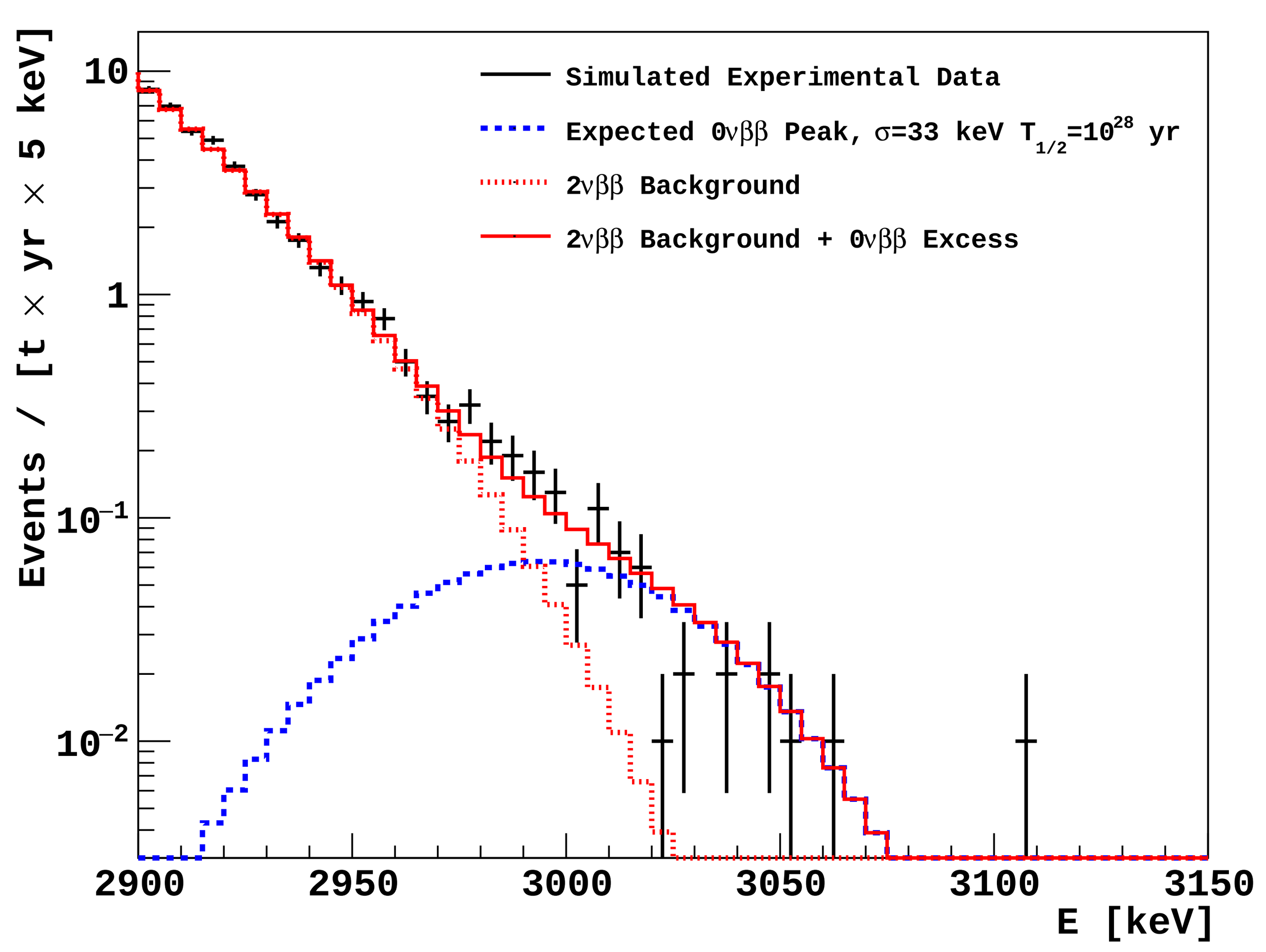


Simulated $2\nu\beta\beta$ event in the Selena detector with 10μm pixel pitch at different positions in the z-axis. The z-position can be fully resolved using the diffusion of the tracks and time of arrival measurements.

Science Goals

The Selena experiment makes use of ^{82}Se to perform a search for $0\nu\beta\beta$ free from the background from natural radioactivity. We achieve this since:

- Q$_{\beta\beta}$ = 2.998 MeV, which sits above most natural radioactive backgrounds
- **CMOS track geometry reconstruction and event timing** can be used to tag decay chains from ^{214}Bi and ^{208}Tl
- **Bragg peaks** can be used to differentiate single β events and γ-ray interactions.

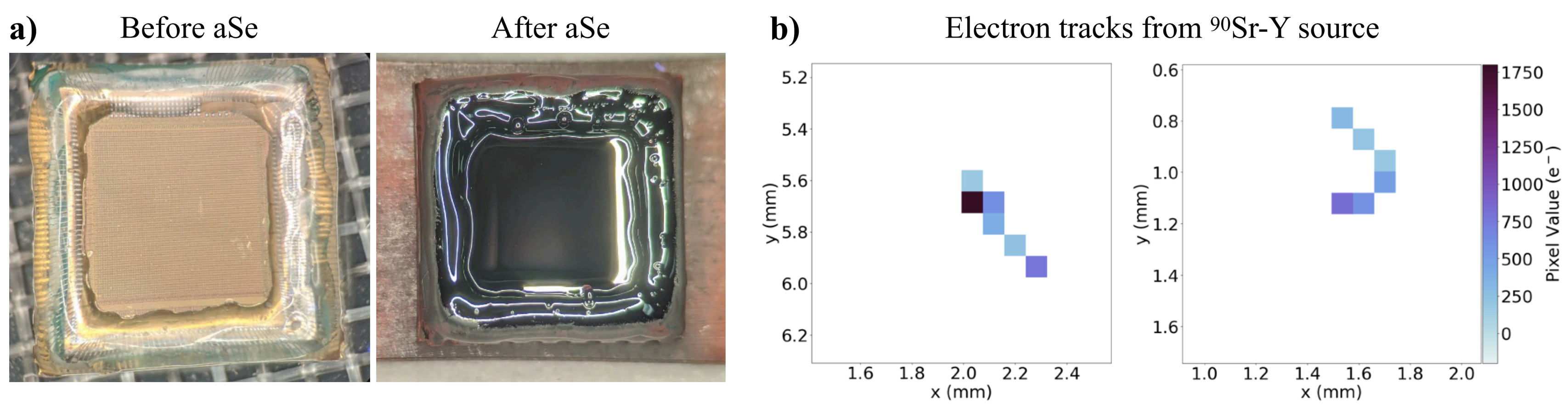


Simulated spectrum for a 100 ton-year exposure using the energy resolution of aSe measured in [5].We estimate a limit on the $0\nu\beta\beta$ half life to be $\tau_{1/2} > 5 \times 10^{28}$ yr at a 90% confidence level.

Additionally, the Selena neutrino experiment has recently expanded its science goals to include solar neutrino spectroscopy and an investigation into the "gallium anomaly," with implications for sterile neutrinos [3] [2].

Current Prototype

The current prototype detector module implements the Topmetal-II$^-$ chip [1]as the pixelated charge sensing device with 500μm of aSe deposited by Hologic Inc. Each *topmetal* pixel contains an exposed electrode made from the topmost metal layer. The electrode is directly connected to the input of a charge sensitive preamplifier (CSA). By tuning the CSA decay time for long signal retention, we can multiplex the signals from each pixel onto a single output for readout using a rolling shutter. Initial results indicate a noise performance of $\sim$23 electrons.



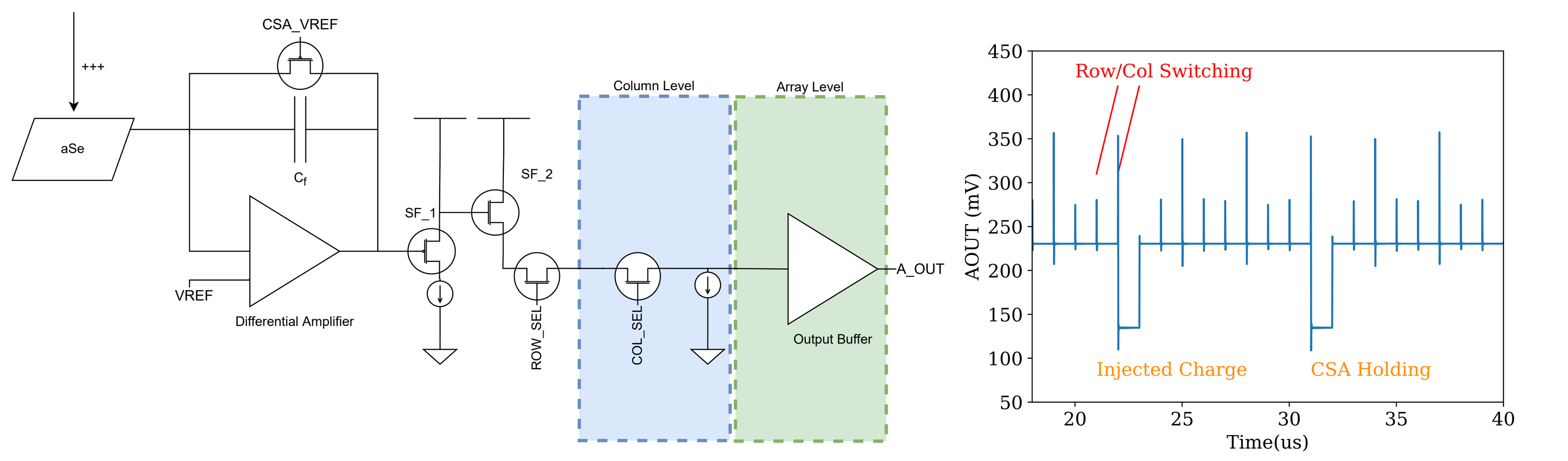
Left: 500μm of aSe deposited on the Topmetal-II$^-$ chip. **Right:** Single β tracks from ^{90}Sr taken using aSe deposited onto the Topmetal II$^-$

The Open-Source Sky130 Process

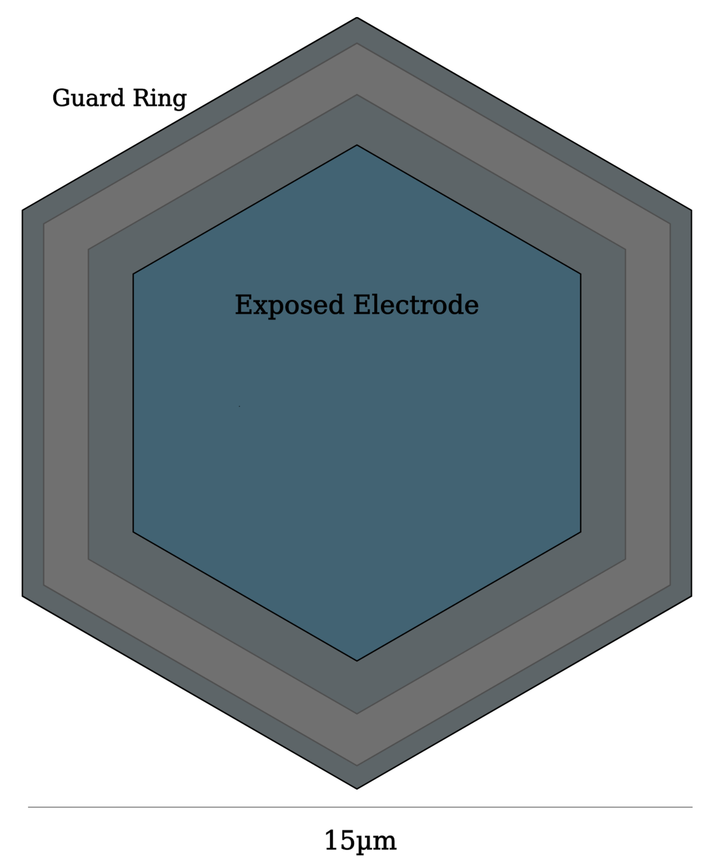
As of June 2020, the Skywater Foundry was the first foundry to offer a fully open-source process design kit (PDK), sponsored by Google. Traditionally under expensive licenses and limited NDAs, the Skywater Open PDK acts as an entry point into CMOS ASIC (application specific integrated circuit) design for physicists. Crucially, the open-source design of our sensor will allow for greater collaboration amongst collaborators and iteration, long after any NDA expires. Fabrication is offered through collaboration with efabless, which offers both a free lottery-based shuttle run and a paid reservation shuttle run.

The TopmetalSe

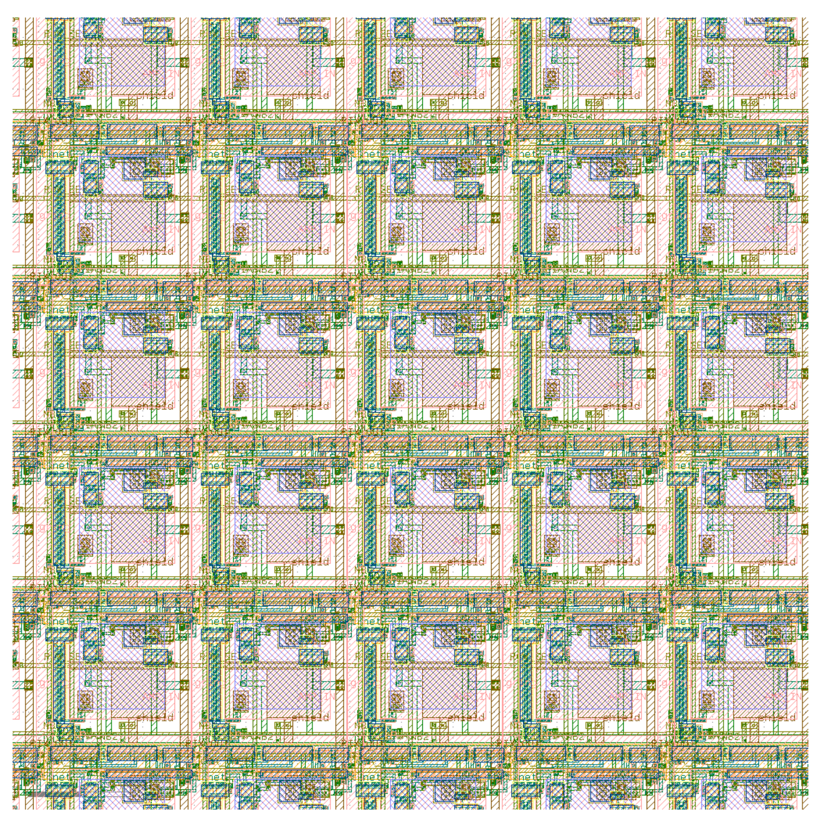
The final Selena detector modules require the design of a custom CMOS imager, known as the Topmetal-Se. We are currently in the process of designing the Topmetal-Se in the SkyWater open 130nm process and will be receiving our first prototypes in Fall 2022.



First prototype pixel and array structure. Charge within the aSe is presented as the input to a CSA, where the feedback resistance is controlled by the difference between the gate voltage CSA_VREF and the baseline voltage VREF. Rolling shutter is performed using the ROW_SEL and COL_SEL switches. Right shows SPICE simulated output response to an injected signal for a minimal 3x3 pixel array.



(a) Target pixel geometry for next iteration.



(b) Pixel array in IC layout design software, submitted for tapeout.

Ongoing design of the pixel. Figure a) shows pixel geometry, with exposed *topmetal* layer. The surrounding guard ring allows for application of a HV to focus field lines onto the electrode. Simulation in COMSOL suggests we can achieve > 99% collection efficiency.

The final iteration of the Topmetal-Se will feature:

- **10μm pixel pitch**, optimized for readout of aSe
- **Time of Arrival measurement**, with nanosecond precision
- $\sim$**10e$^-$ noise**
- **Digital pixel sensor readout structure** for fast readout [4]

References

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