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U.S. DEPARTMENT OF ENERGY

LArTPC Pixelated Readout

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with contributions from Jonathan Asaadi (UTA) and Dan Dwyer (LBNL)

DUNE P5 Strategy: Phase II Detector R&D

Neutrino Physics Frontier, SNOWMASS Community Summer Study

July 20, 2022

Why pixels?

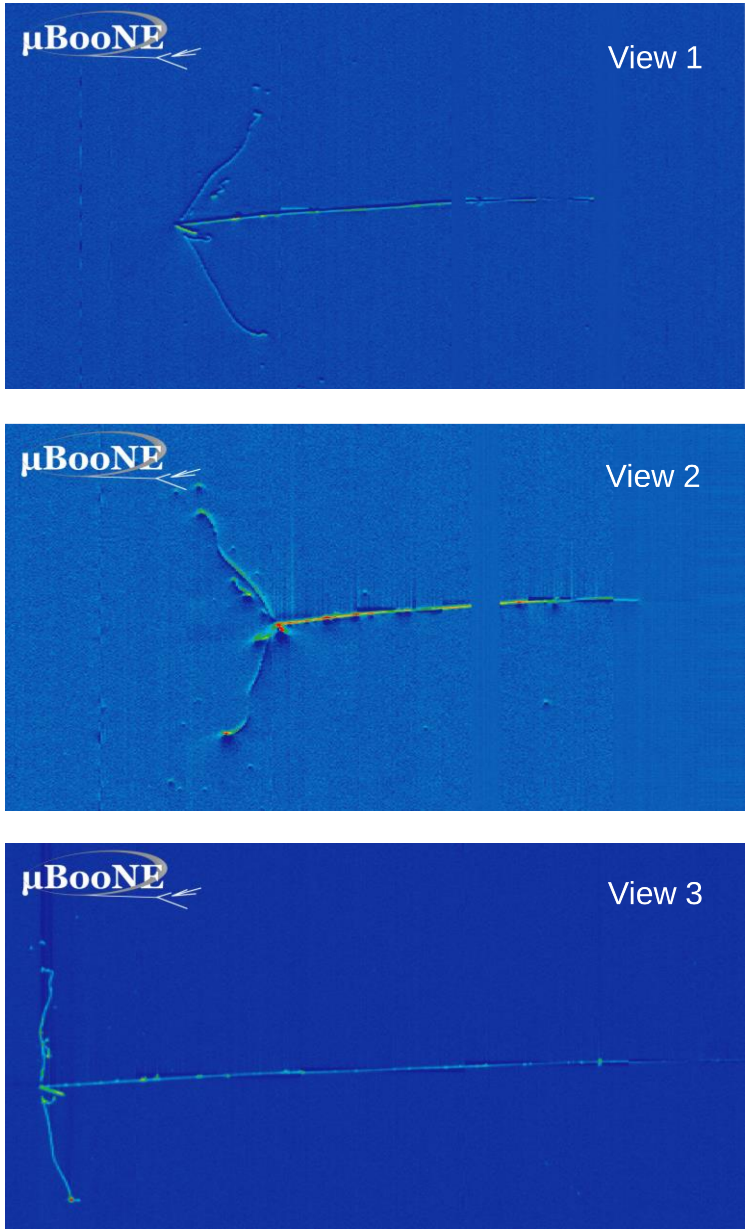
- True 3D imaging
  Unambiguous, inherently 3D raw data
- Self-triggered pixel-by-pixel data
  ~100% livetime

Technical challenge: instrumenting ~2000 m^2 anode area at 4 mm granularity → **requires scalable design**

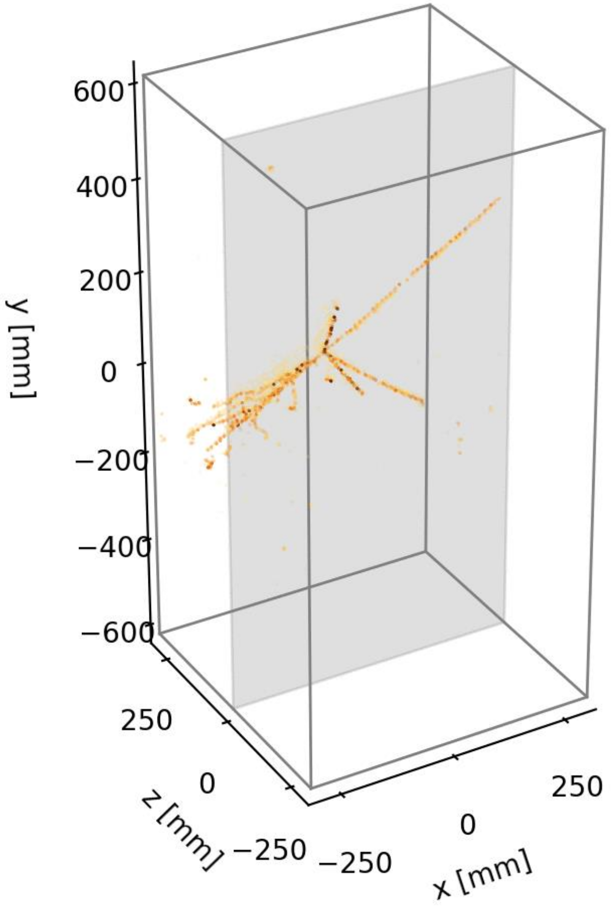
Two existing LAr pixel readout efforts discussed here:

QPix

LArPix



Traditional wire readout
(MicroBooNE ν data)

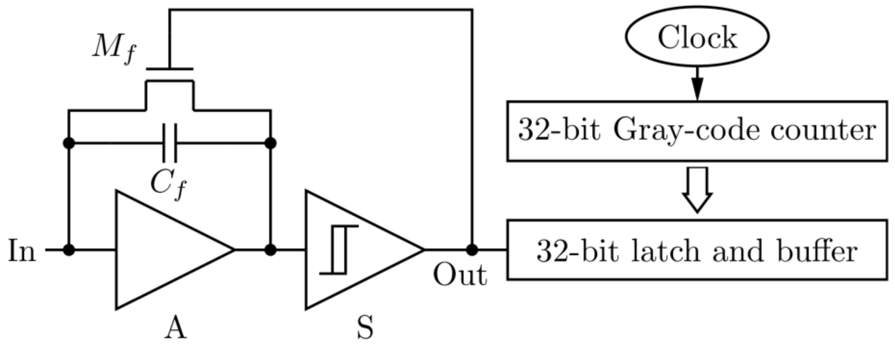


Pixel readout
(LArPix cosmics data)

QPix

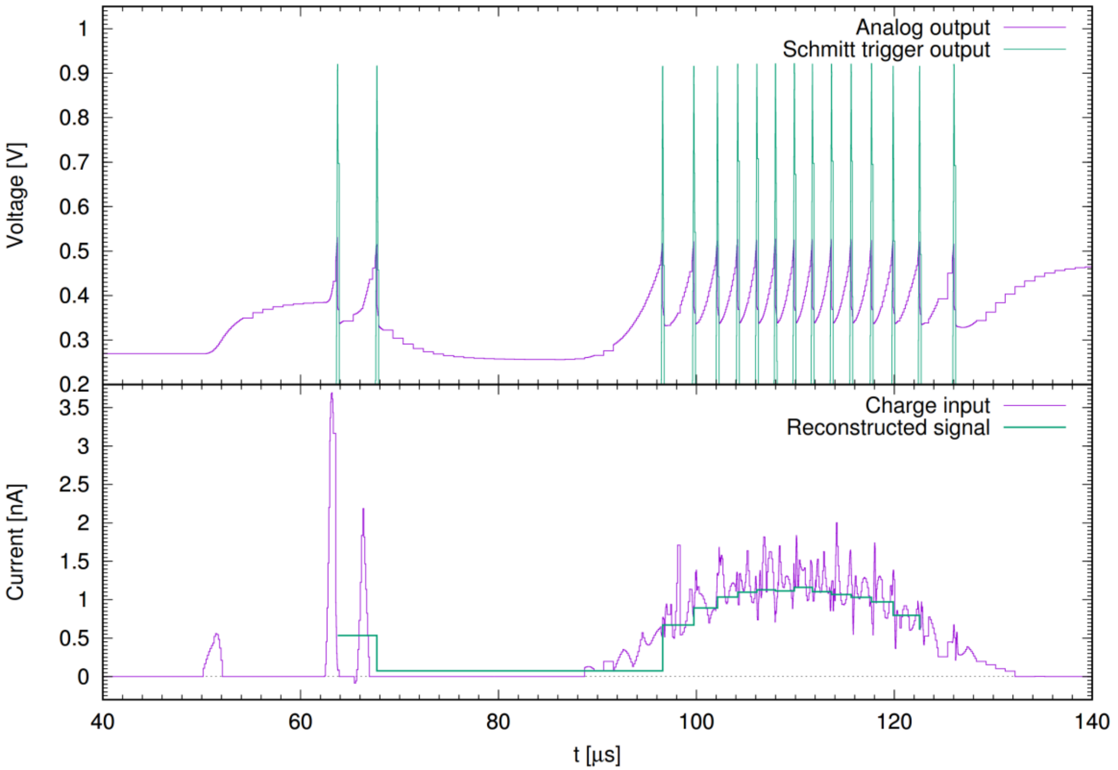
QPix Concept

Original QPix scheme delineated by Dave Nygren (UTA) and Yuan Mei (LBNL) [1809.10213](1809.10213)



Datum:

- ΔQ = Reset Time Difference (RTD)
- 64 bits (including 32 bit timestamp)



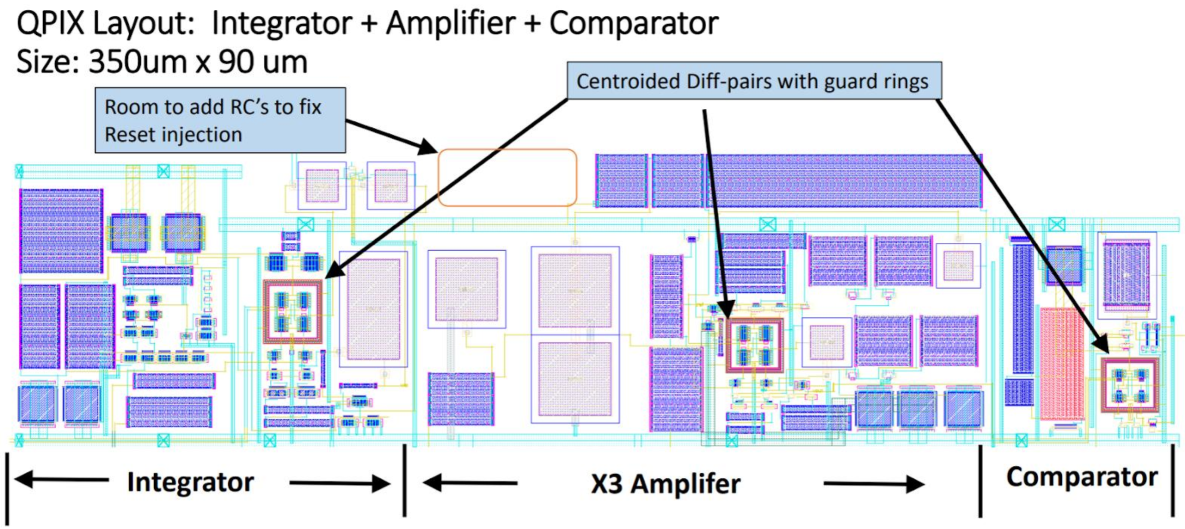
Transistor-level charge integration simulation for minimum-ionizing track in LAr for 1 fC threshold

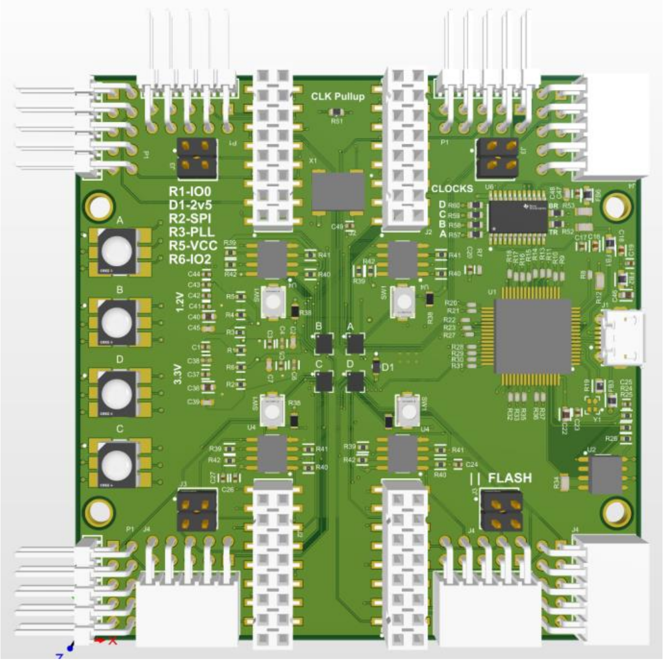
QPix ASIC

180 nm Implementation

- Front-end prototype (Penn)
  - charge replenishment
  - “basic” reset
- Ring oscillator and 10-bit r2r DAC (Hawaii)
- FPGA-implemented digital readout (Hawaii)
  - 4 (2x2) digital FPGAs with 16 optional IO pins per FPGA
  - Optional 50 MHz “global” clock or 4x48 MHz internal clock

→ *Submission targeted for August 2022*
– test structures and 16 channel chip



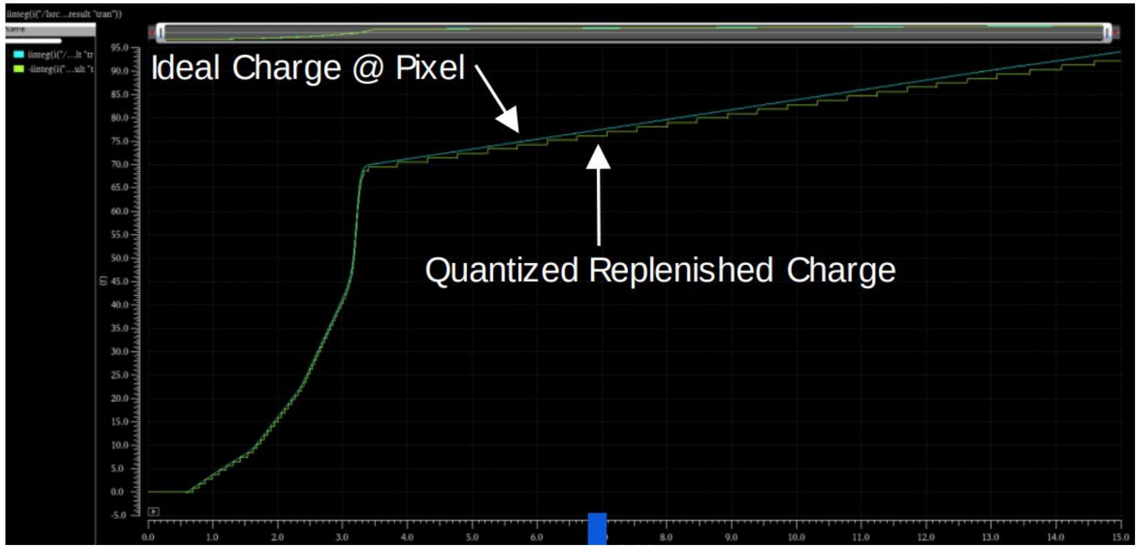


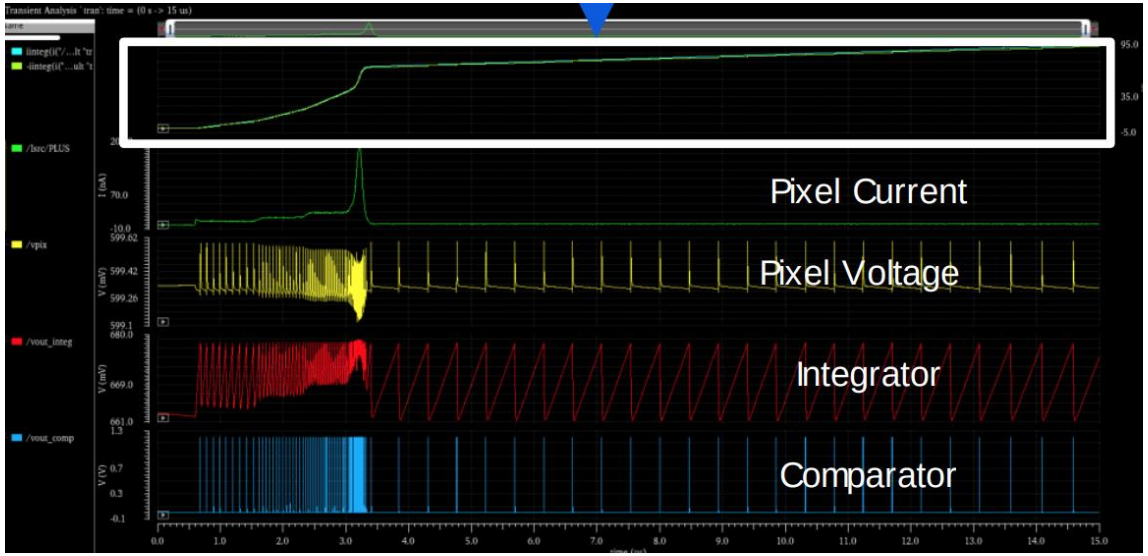
QPix ASIC

65 nm Implementation

- Front-end design (FNAL)
  - charge replenishment circuit evaluation
    - Bandwidth study with ideal components
    - First version of the low power front end amplifier
  - dynamic vision sensing evaluation for asynchrounous photon detection
- Further work dependent on resource availability at FNAL

→ Submission targeted in 12-15 months timescale (16 channel chip)



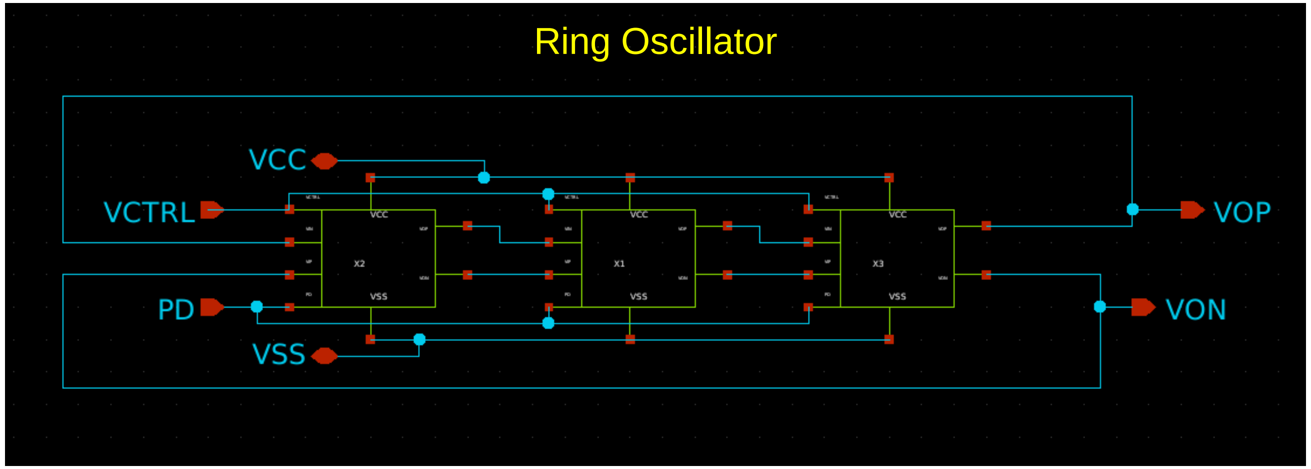


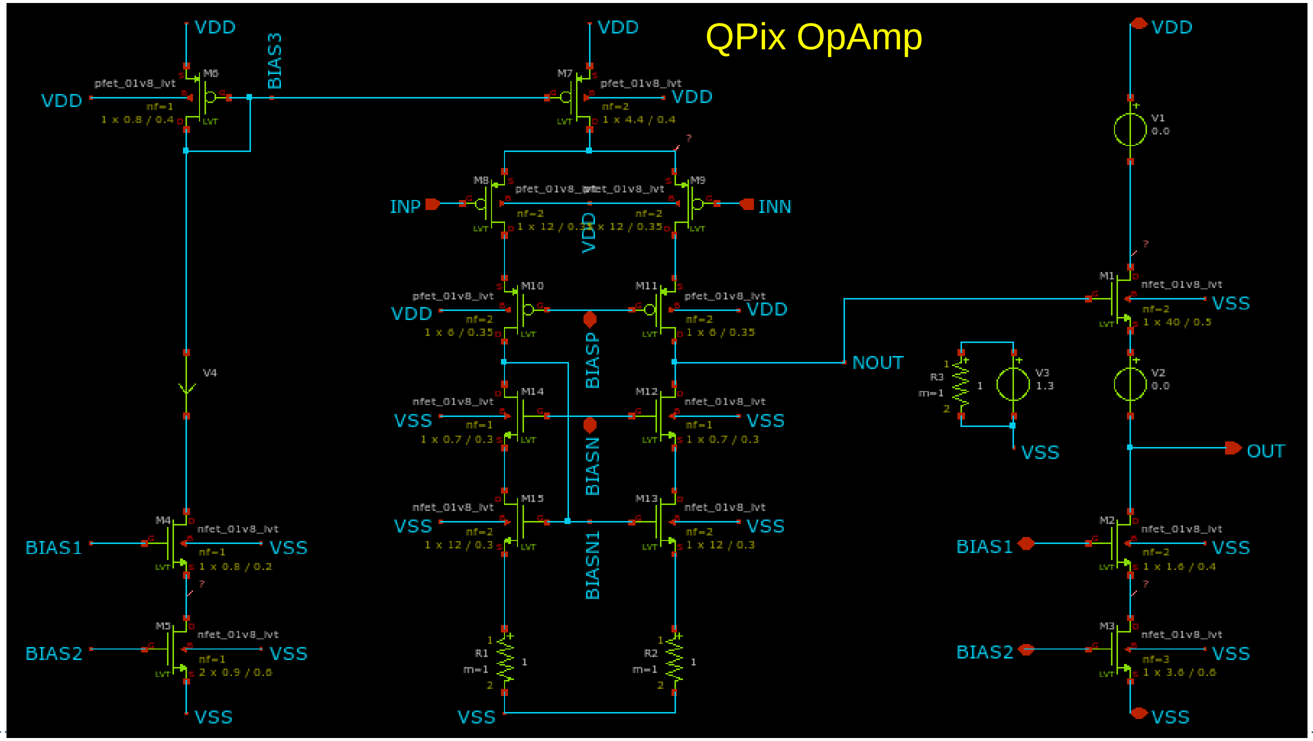
QPix ASIC

130 nm Implementation

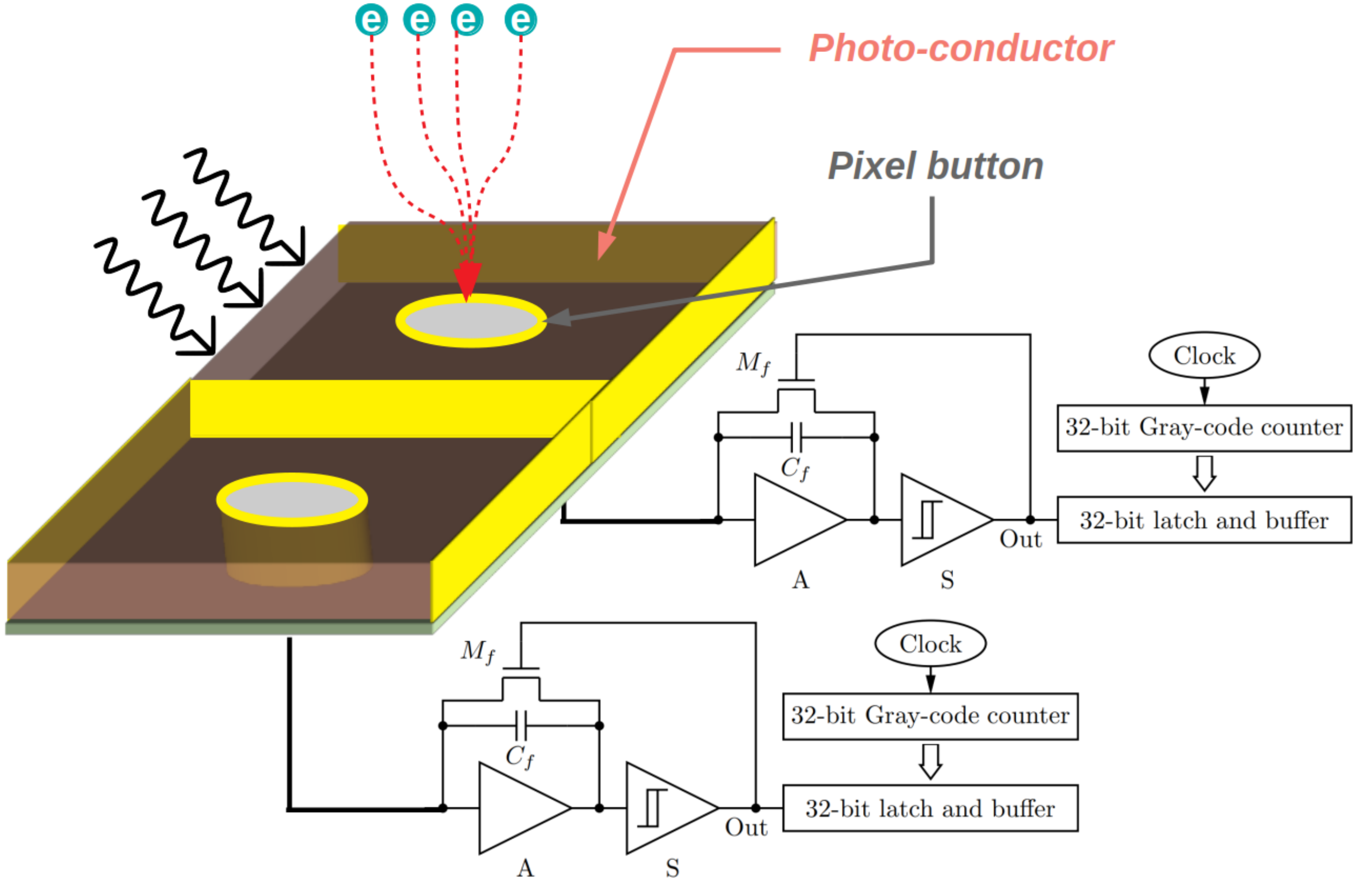
- Using eFabless + Skywater + Google open source process design
- Front-end prototype (UTA)
  - Ring oscillator
  - Relaxation oscillator
  - QPix OpAmp

→ May 2022 submission

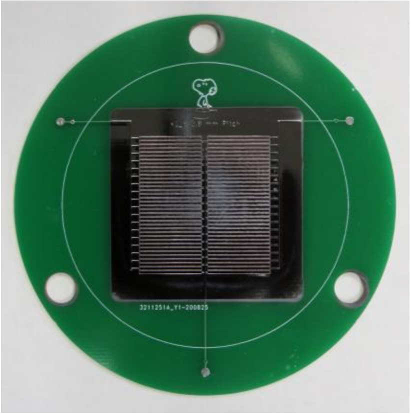




QPix Dual Light-Charge Readout

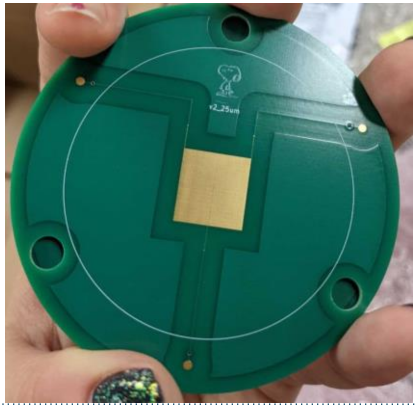


Commercial PCB with 127 μm trace spacing
5 V/μm max field
UTA/ORNL



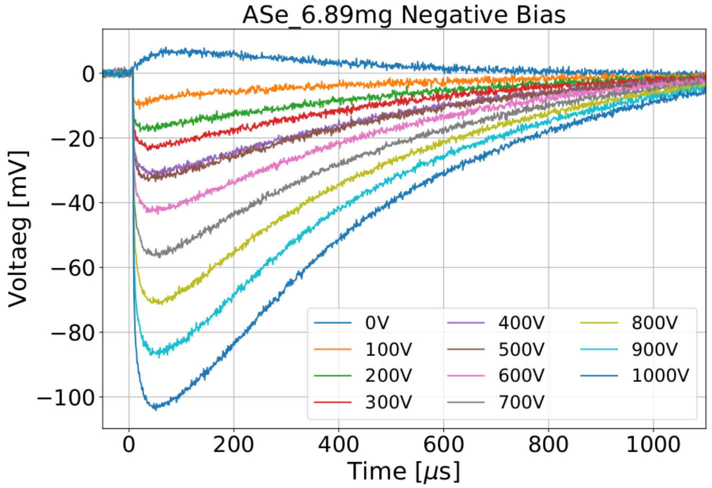
Commercial PCB with 127 μm trace spacing
5 V/μm max field
UTA/ORNL

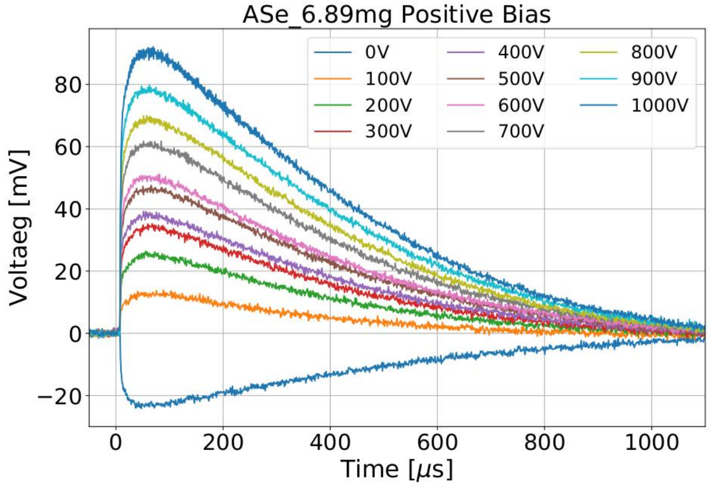
Custom PCB with 25 μm trace spacing
40 V/μm target field
UCSC/UTA/FNAL



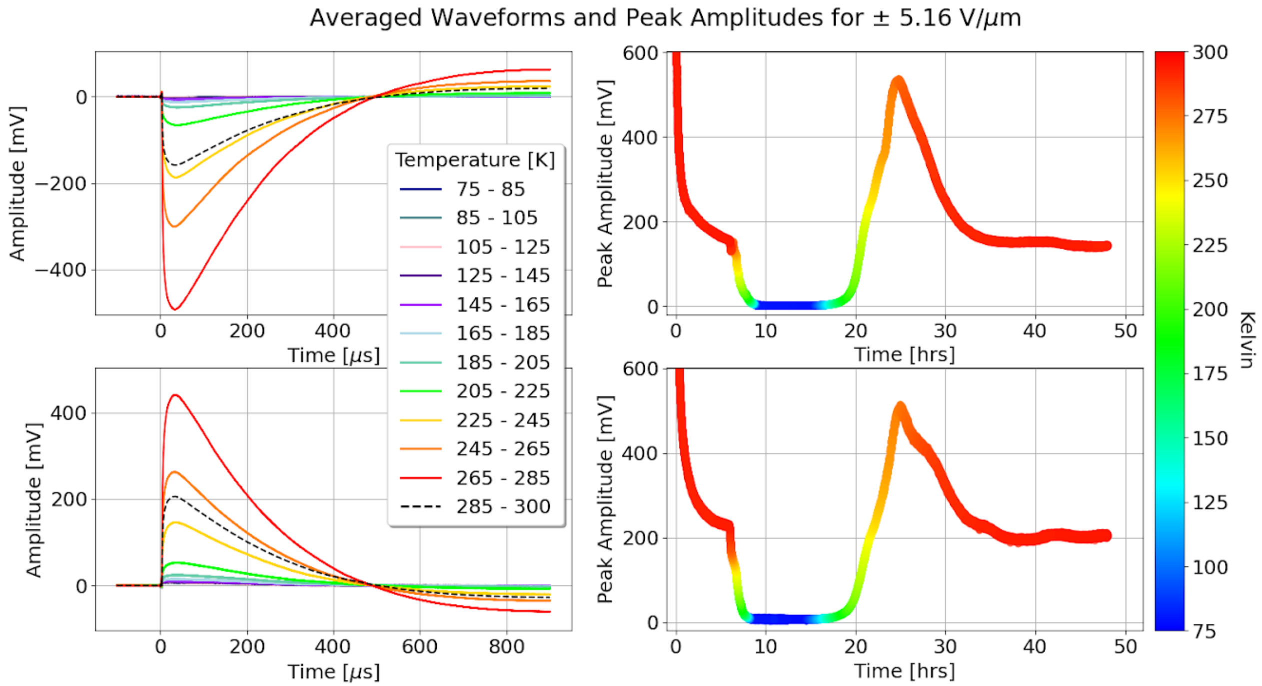
QPix a-Se R&D

Vacuum Tests





Cryogenic Tests



LArPix

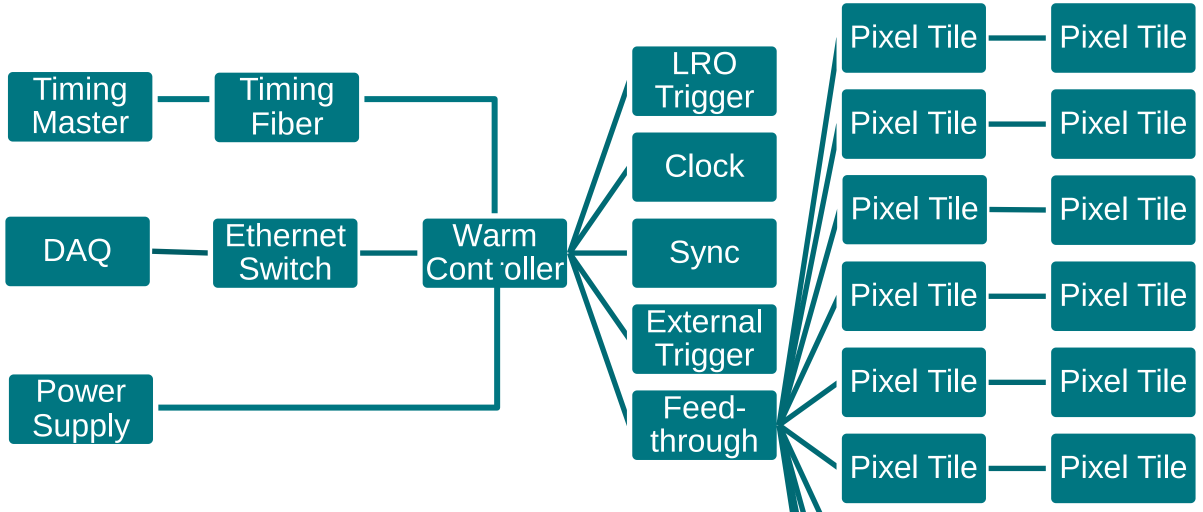
LArPix System Architecture

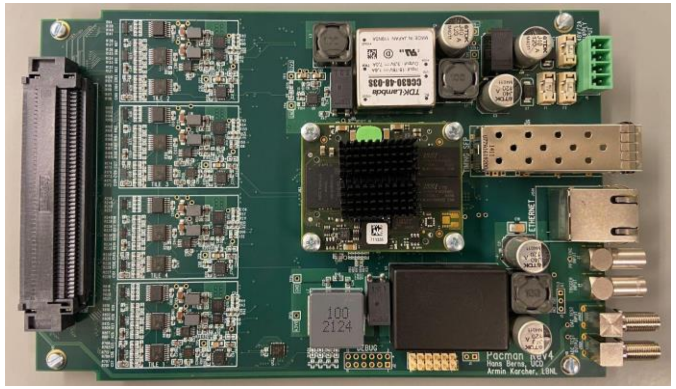
A contained, end-to-end system focused on reliability & robustness

- Limit single-point failures
- Scalable to O(M) channel systems

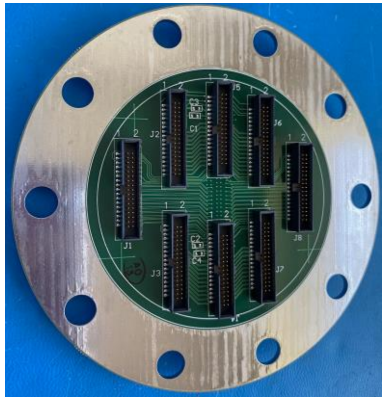
Design features

- Single active component in cryo environment
- Minimal and redundant connections to outside cryostat
- Mechanically and cryogenically robust

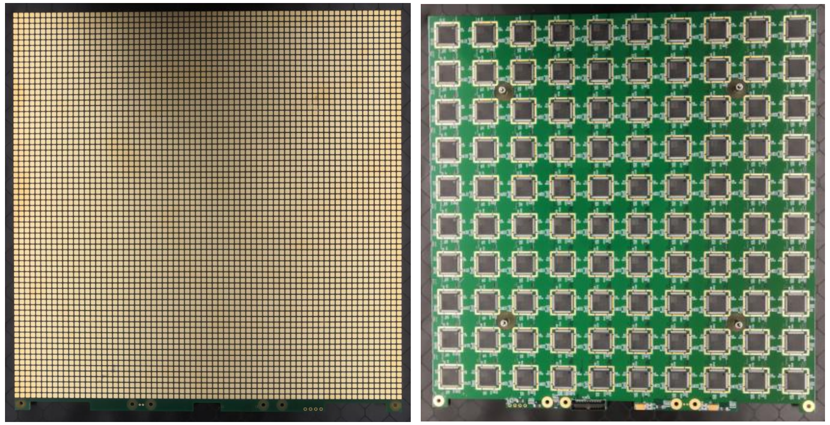




PACMAN Warm Controller



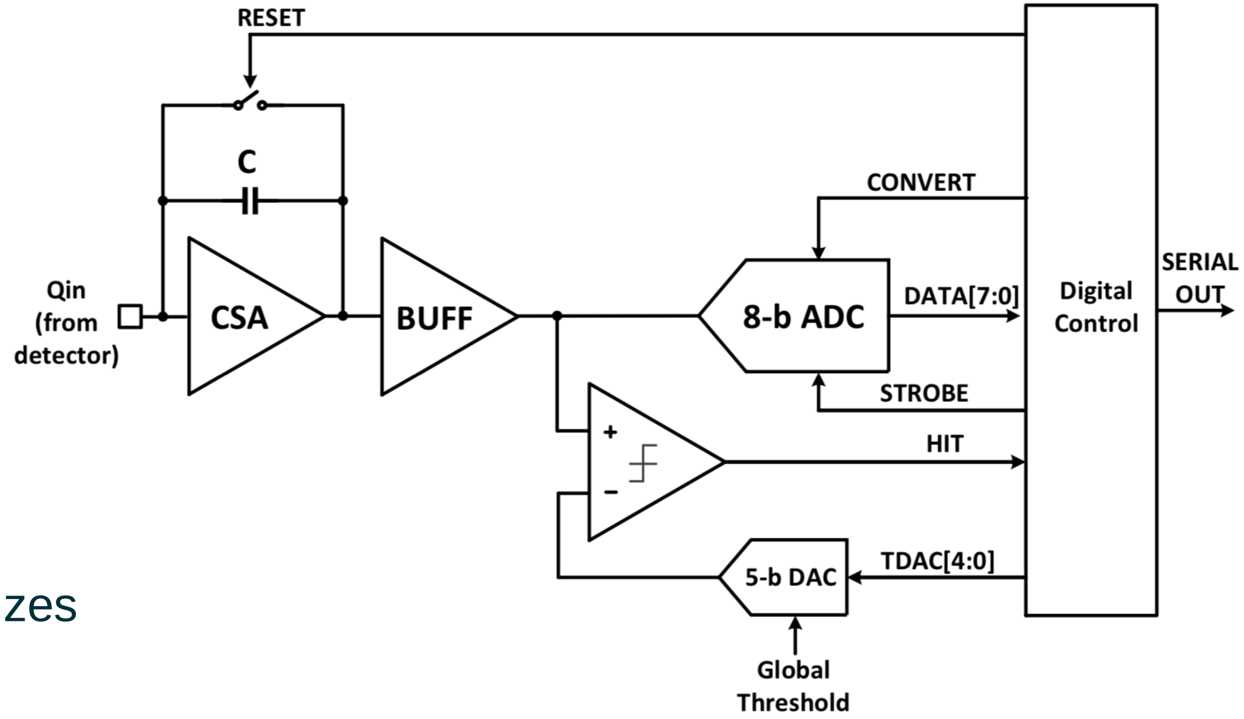
Feedthrough



32 cm by 32 cm anode PCB tile

LArPix ASIC Concept

Low-power, integrating amplifier with self-triggered digitization and readout

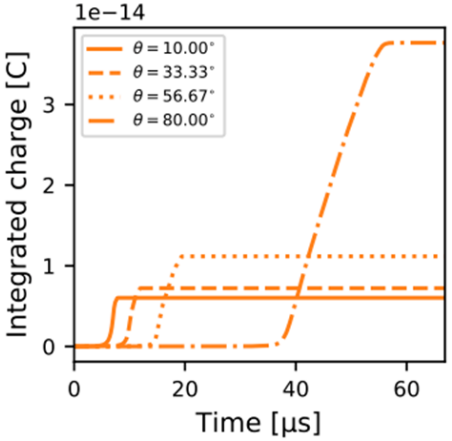


Pixel dormant until signal exceeds tunable threshold

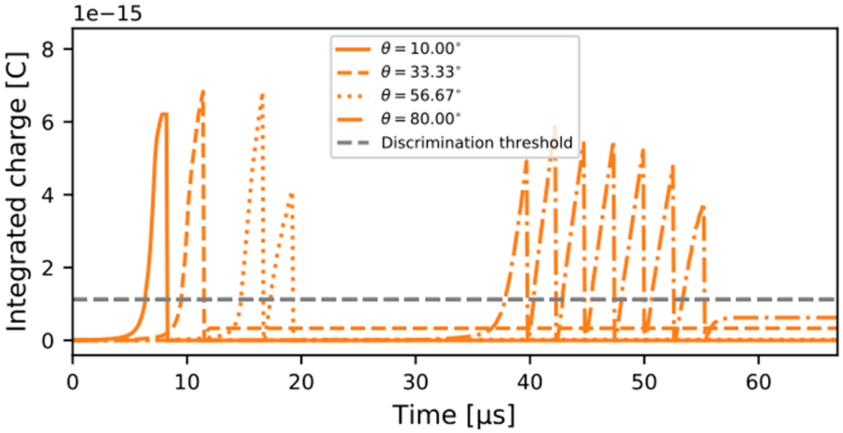
- Integrates charge for ~3μs (~4 mm drift), then digitizes
- Ready for next signal

Pixels are continuously active

- Serial I/O data rate is slow (~5 Mb/s per channel) to limit digital power
- Modest data volumes: ~1 MB/s per square meter of anode in surface cosmic flux

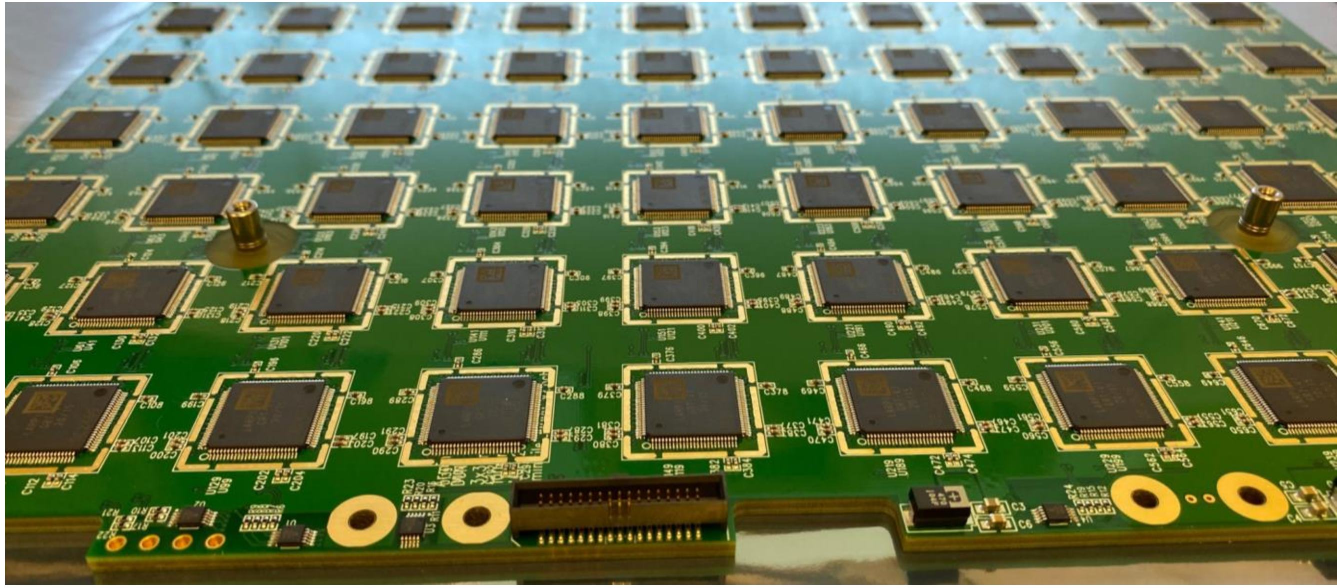


Simulated front-end charge integration



Incorporation of buffering, ADC sampling, and digitization

LArPix ASIC Implementation



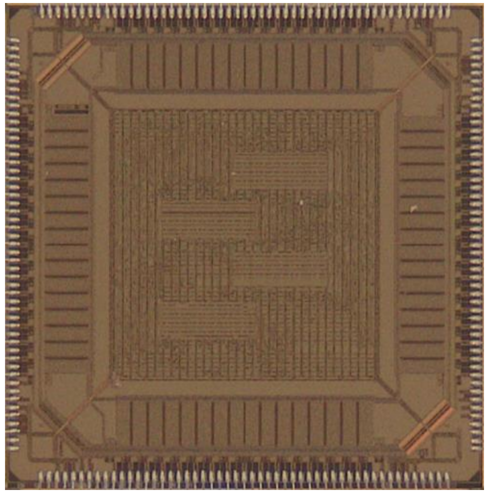
LArPix ASIC

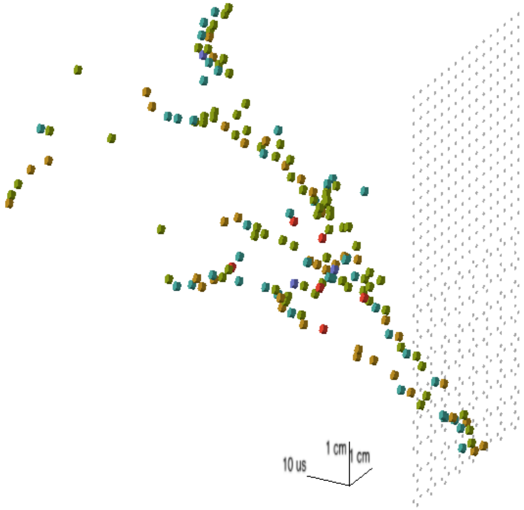
- 64-channel CSA with self-triggered ADC
- Includes amplification, digitization, and readout
- Implemented in 180 nm; migrating to 130 nm

Design drivers

- Low power — *O(100 μW) / channel*
- Low leakage — *< 5 e- / 500 μs*
- Low noise — *850 e- ENC*
- Digital multiplexing — *O(1k) pixels / I/O channel*

LArPix-v2b ASIC





LArPix-v1 recorded cosmic EM shower

“LArPix-v2: a commercially scalable large-format 3D charge-readout scheme for LArTPCs”
publication in preparation

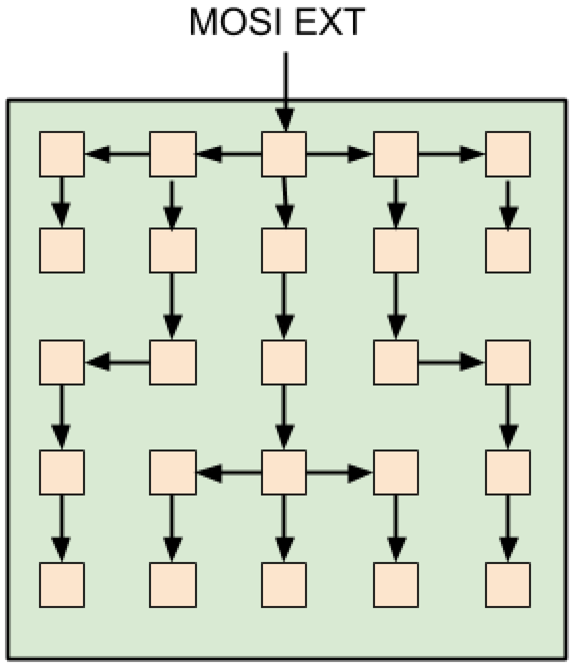
Hydra IO

Dynamic I/O routing

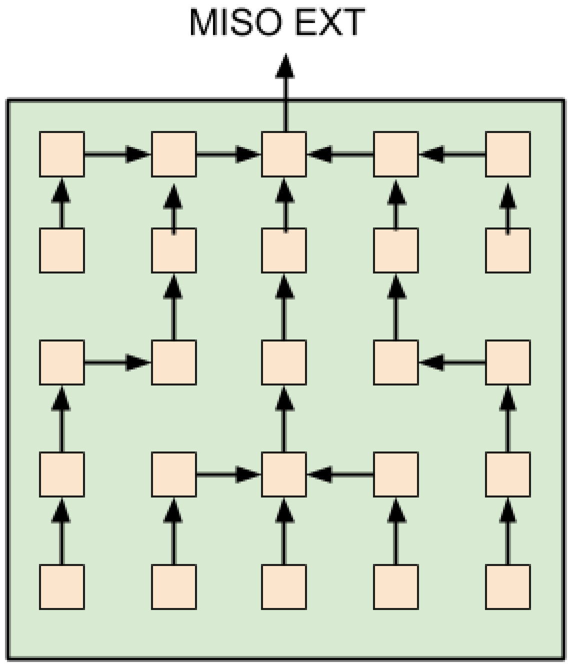
AD-HOC NETWORK OF READOUT APPLICATION-SPECIFIC INTEGRATED CIRCUITS FOR RELIABLE DETECTOR INSTRUMENTATION
U.S. Patent Application Ser. No: 63/140,434

- I/O can occur between any neighboring chips on pixel tile
- Network constructed by explicitly connecting neighboring ASICs in a determined fashion

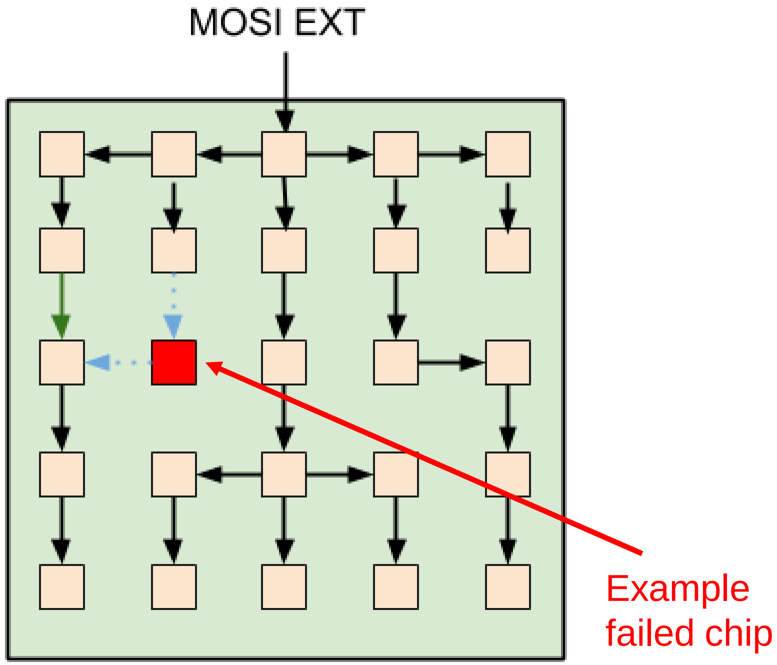
Realized and exercised with LArPix-v2



Upstream configuration commands



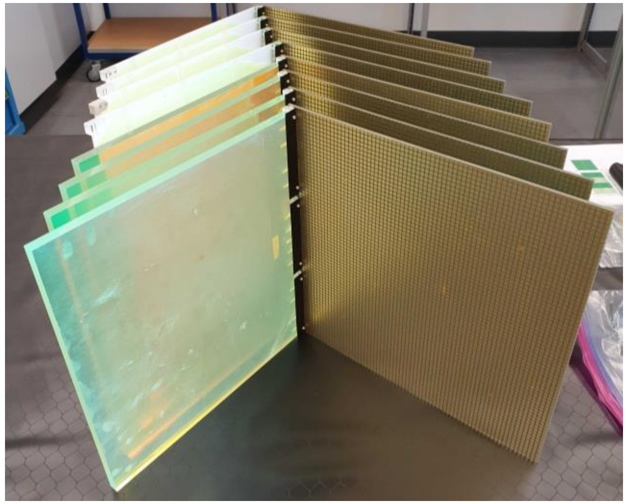
Downstream data flow



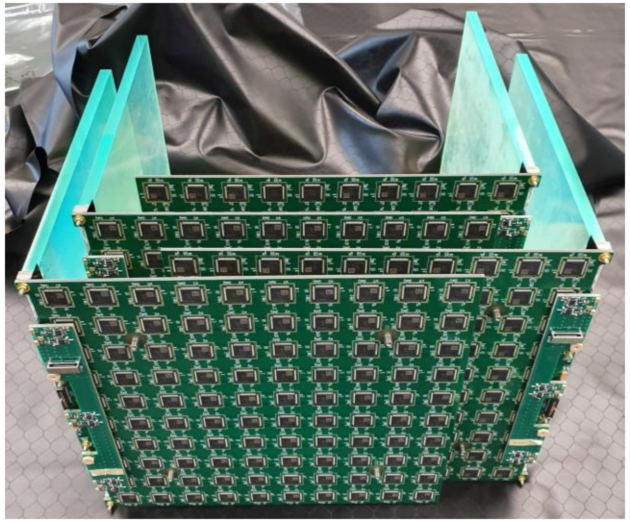
Network reconfigured to avoid failed ASIC

System Prototyping

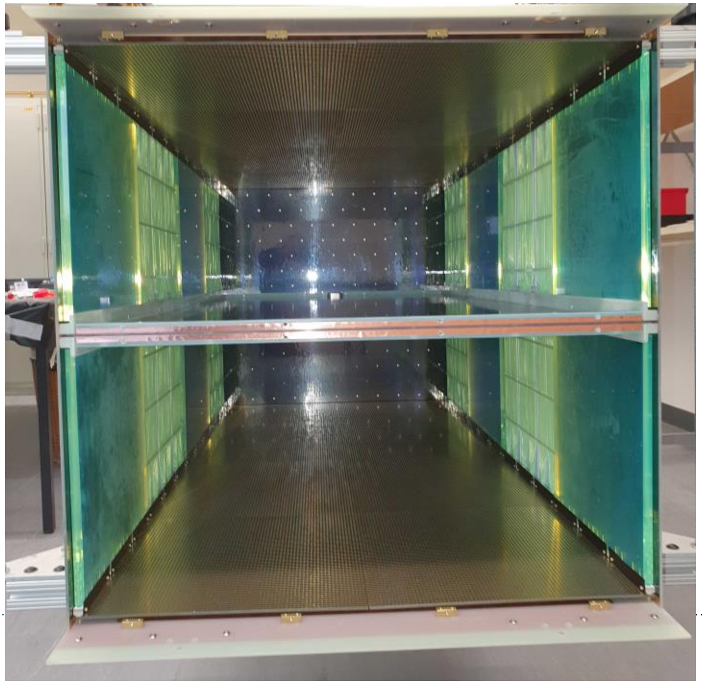
- All production and assembly performed by industry
- Individually tested O(10k) ASICs, O(100) pixel tiles
- Two ton-scale TPCs built and tested



Single pixel tile & light module assemblies



One anode, fully-assembled



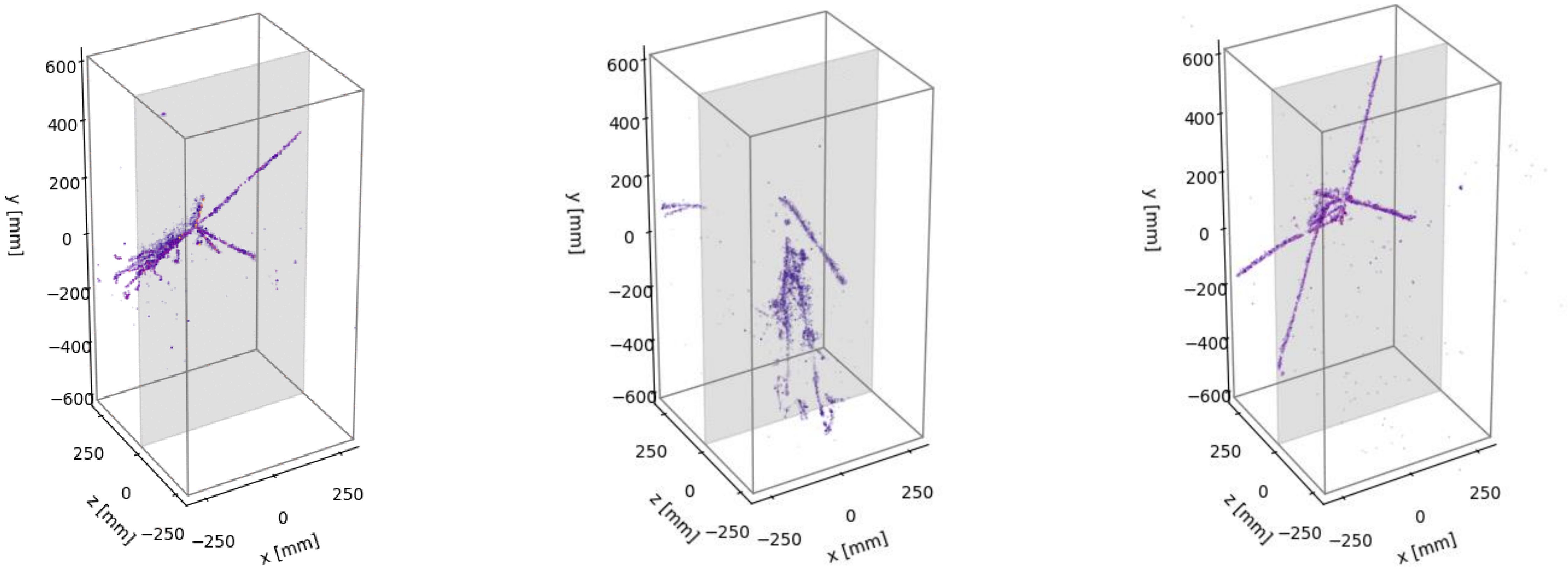
Two anodes installed inside field cage

Fully-assembled LArTPC module

System Prototypes

Raw data

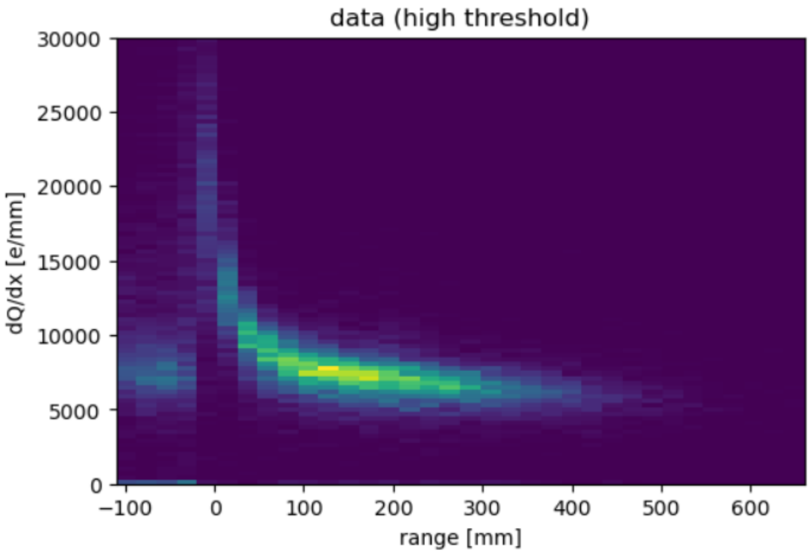
- Successful deployment and operation of two O(100k) channel systems – *>100M cosmic ray events recorded*
- Improved tracking threshold – *O(100 keV)/pixel*
- Quick-turn industry fabrication at competitive cost – *O($0.10/channel) at large O(10 M) channel system*



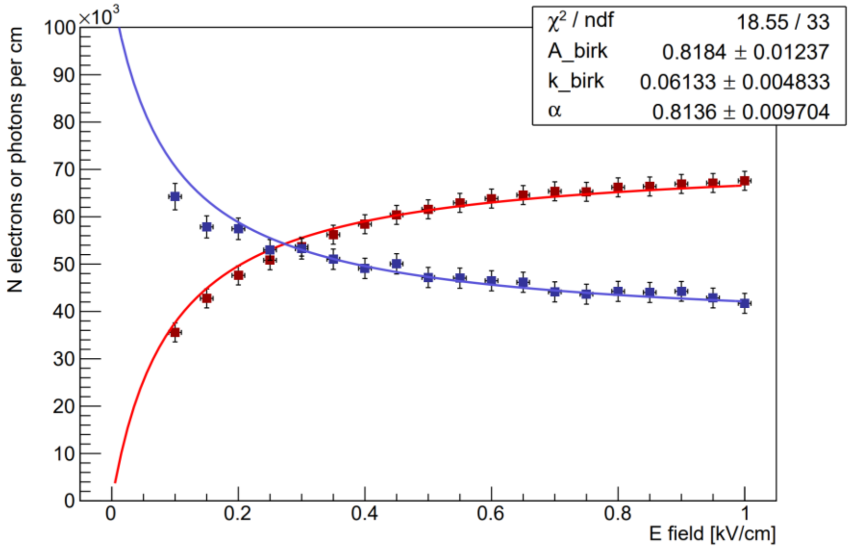
Physics Studies

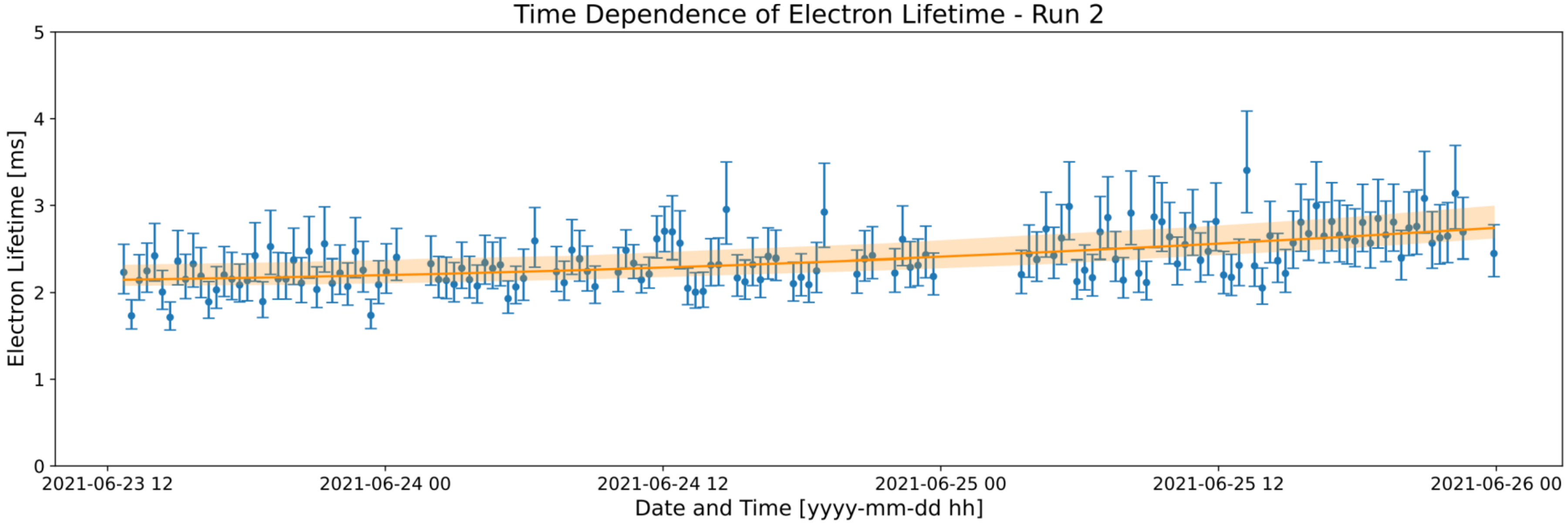
"Performance of a modular ton-scale pixel-readout liquid argon Time Projection Chamber"
publication in preparation

Stopping muon energy loss



Charge-light anticorrelation

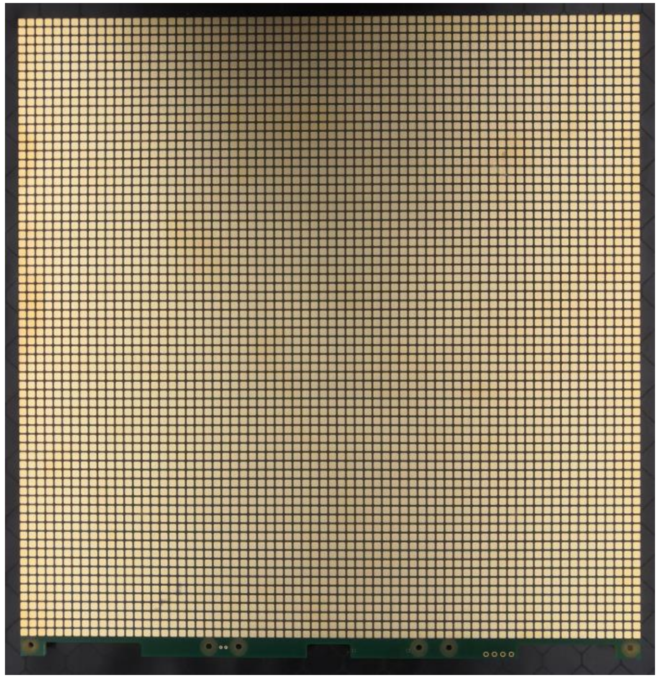




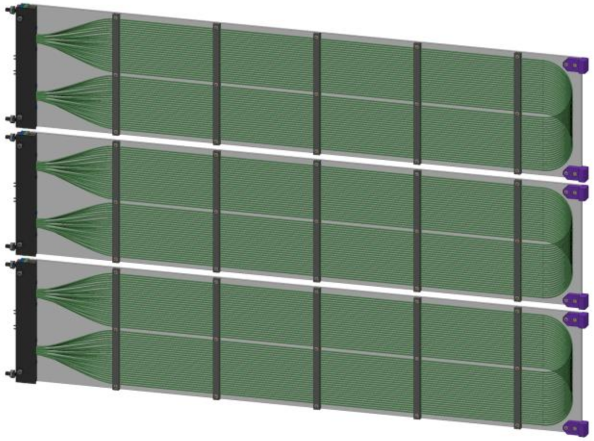
LAr purity electron lifetime

LightPix Concept

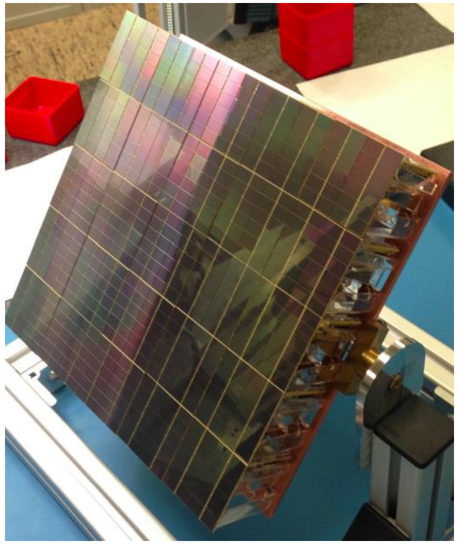
- Low-power cryogenic-compatible scalable ($>10^6$) SiPM readout electronics at very low system cost
- Adapting existing LArPix system architecture
  - Shared cabling, feedthrough, warm electronics
  - LightPix ASIC re-uses majority of LArPix design, but replaces ADC with TDC
- Provide a path for highly-granular photodetection systems for very large detectors



Replace pixel pads with SiPMs



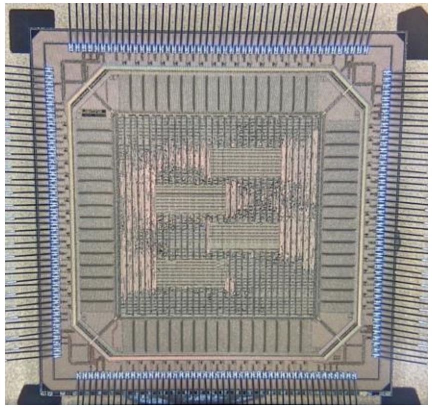
Example of light trap SiPM detector format *LCM*



Example of direct SiPM detector format *DarkSide-20k*

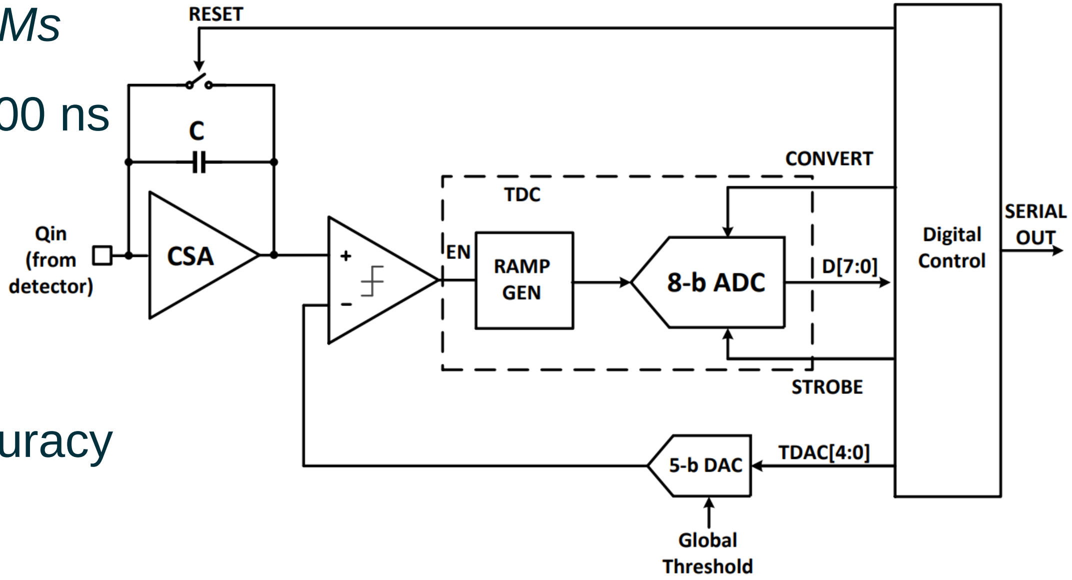
LightPix ASIC Implementation

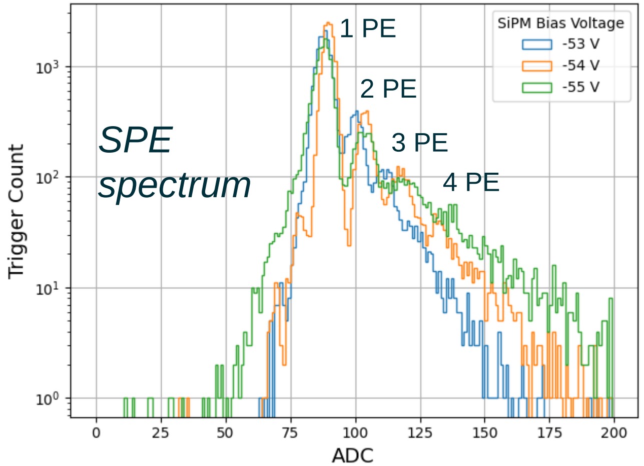
LightPix-v1b ASIC



LightPix-v1b TDC evaluation for SPE from commercial 3 mm x 3mm SiPMs

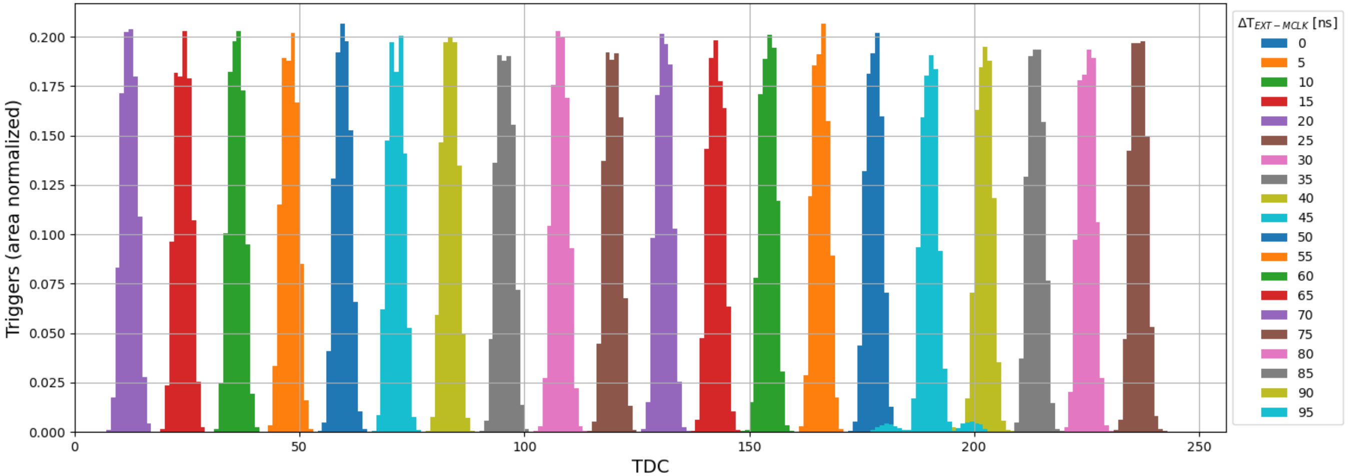
- Linear to <1 ns over the full 100 ns timing range
- < 1 ns jitter
- < 2 ns time-walk bias
- < 1 ns RMS global timing accuracy





LightPix-v2

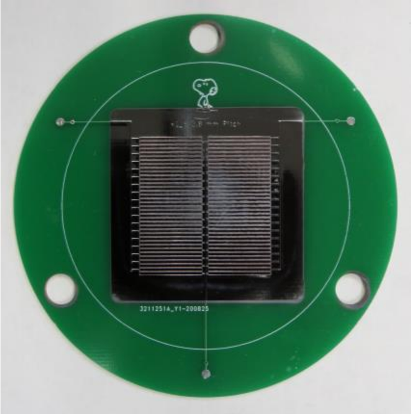
- Dual TDC/ADC functionality in single ASIC – design complete, awaiting production

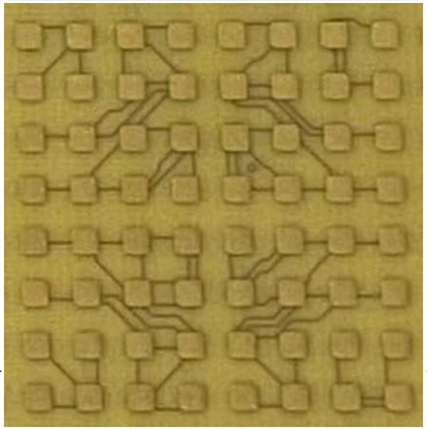


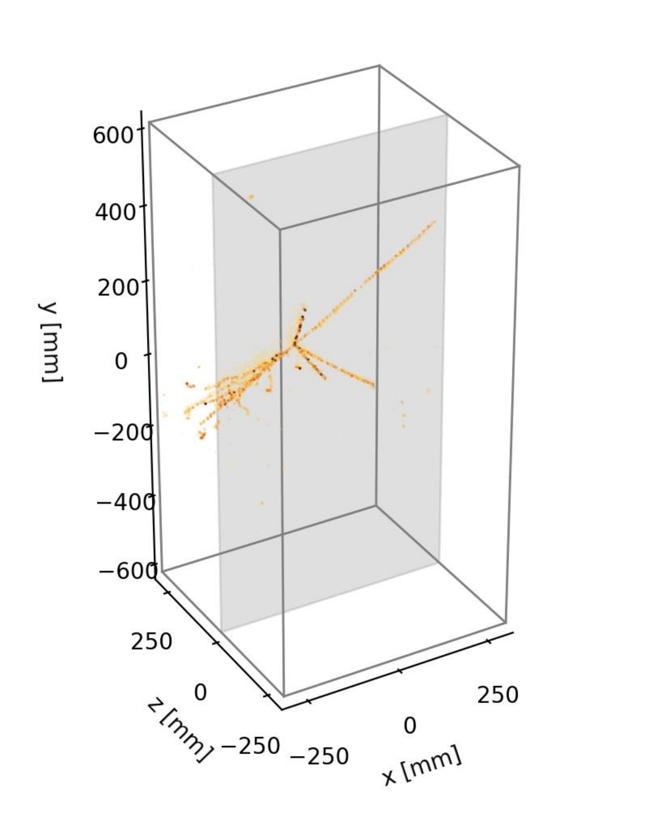
TDC output versus test pulse time offset

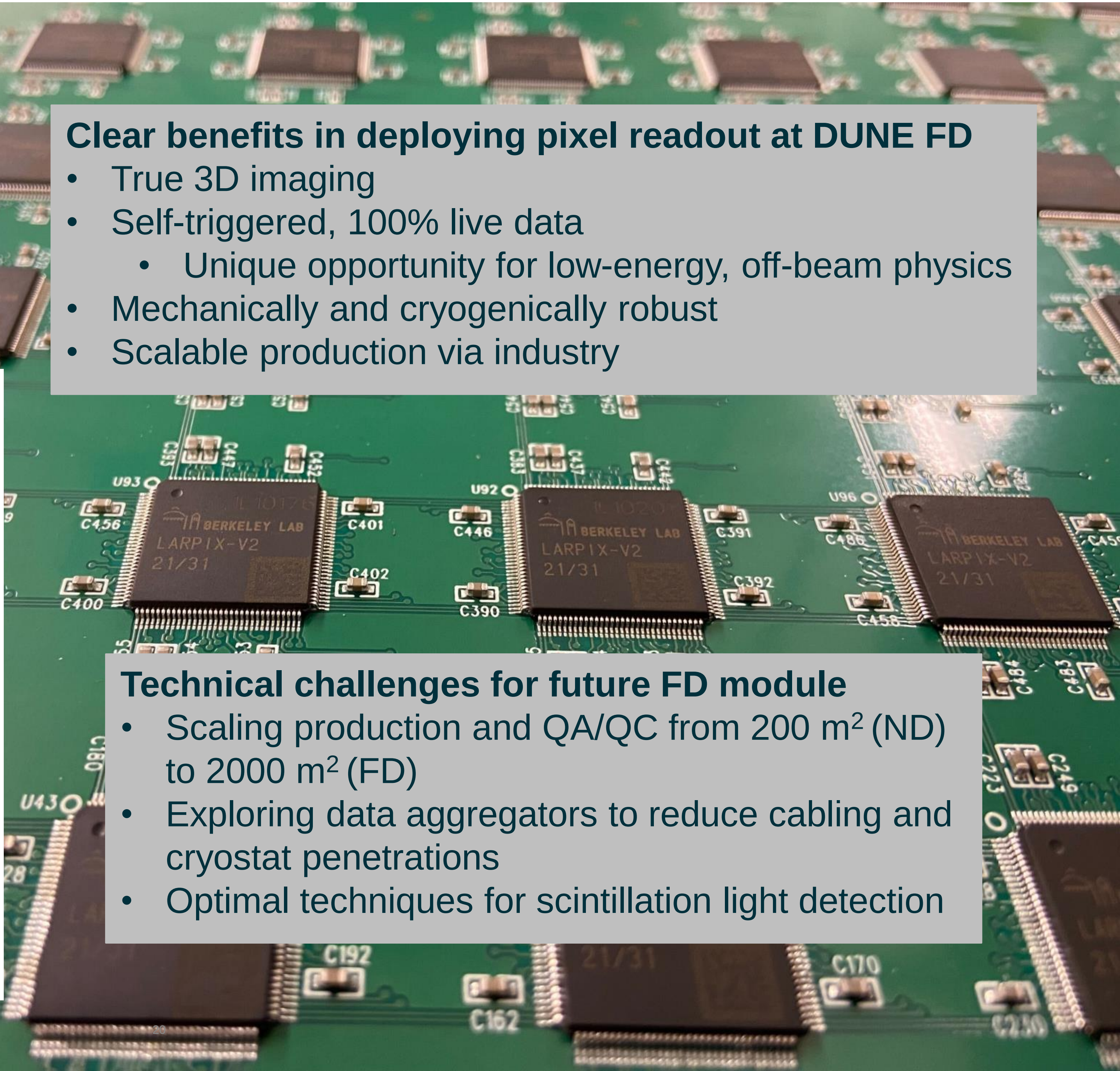
Summary

There are two existing efforts (QPix and LArPix) actively working to realize pixel readout technology for DUNE FD implementation









Clear benefits in deploying pixel readout at DUNE FD

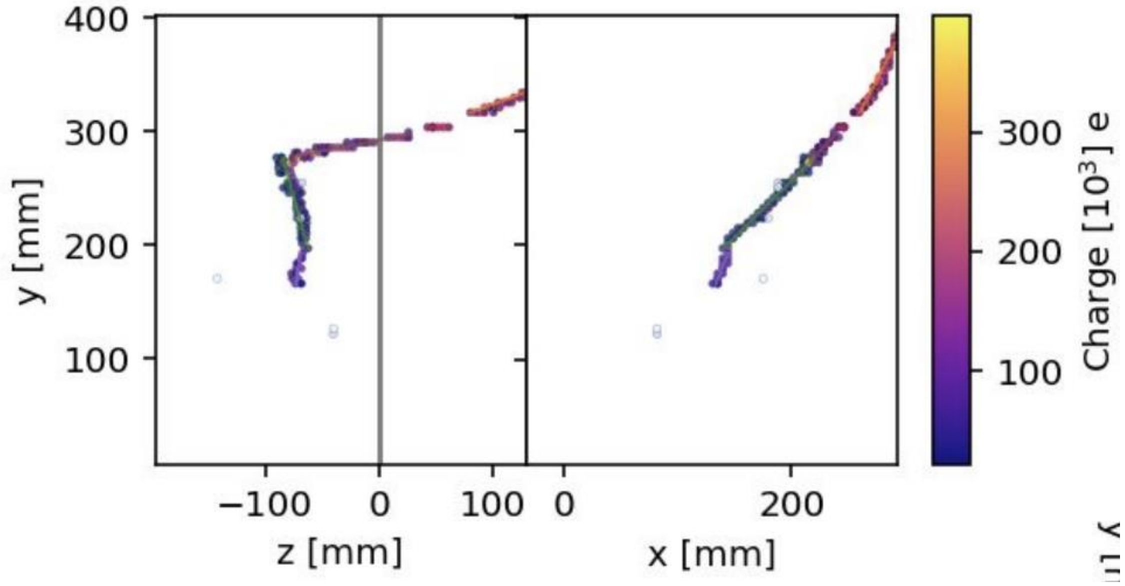
- True 3D imaging
- Self-triggered, 100% live data
  - Unique opportunity for low-energy, off-beam physics
- Mechanically and cryogenically robust
- Scalable production via industry

Technical challenges for future FD module

- Scaling production and QA/QC from 200 m^2 (ND) to 2000 m^2 (FD)
- Exploring data aggregators to reduce cabling and cryostat penetrations
- Optimal techniques for scintillation light detection

Backup Slides

Observation of positron decay

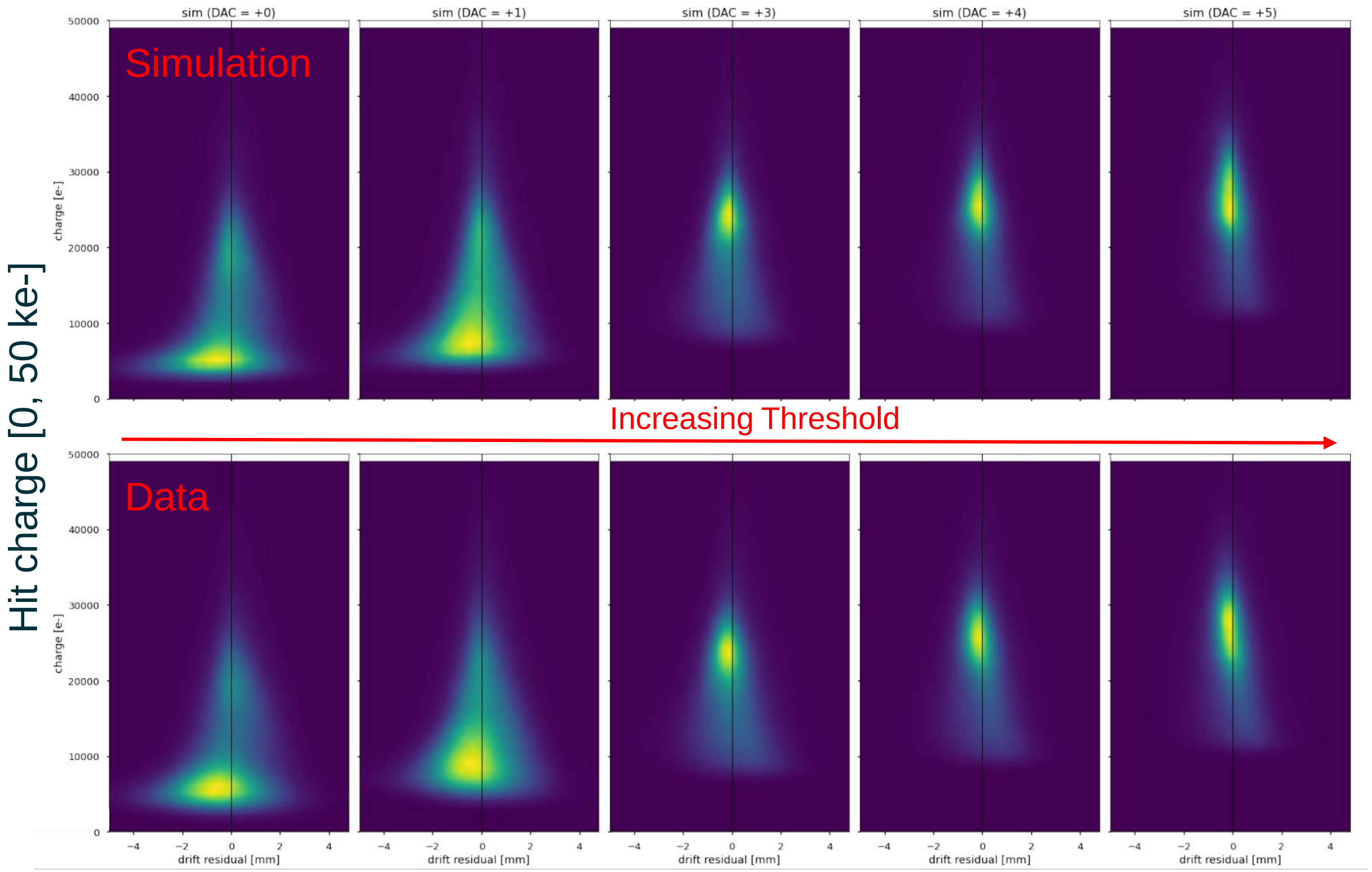


Pixel response validation

Pixel trigger response versus threshold (data versus MC)

- Detailed ASIC front-end charge response simulation using GPU-optimized algorithms

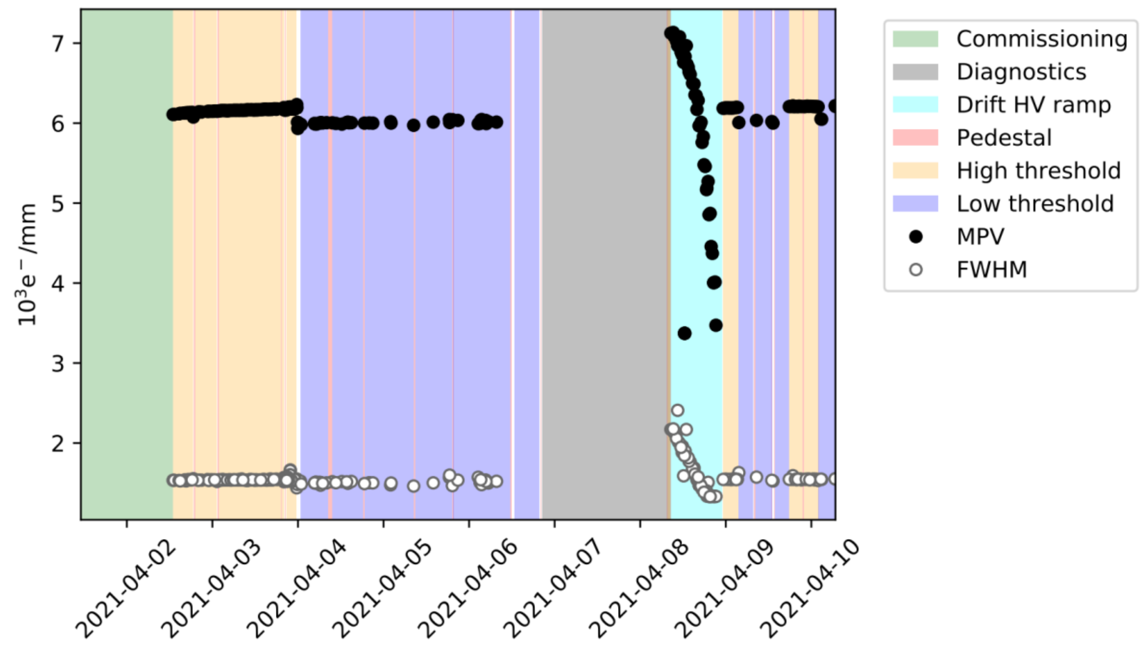
- To first order, good data-simulation agreement in channel threshold crossing time and charge measurement



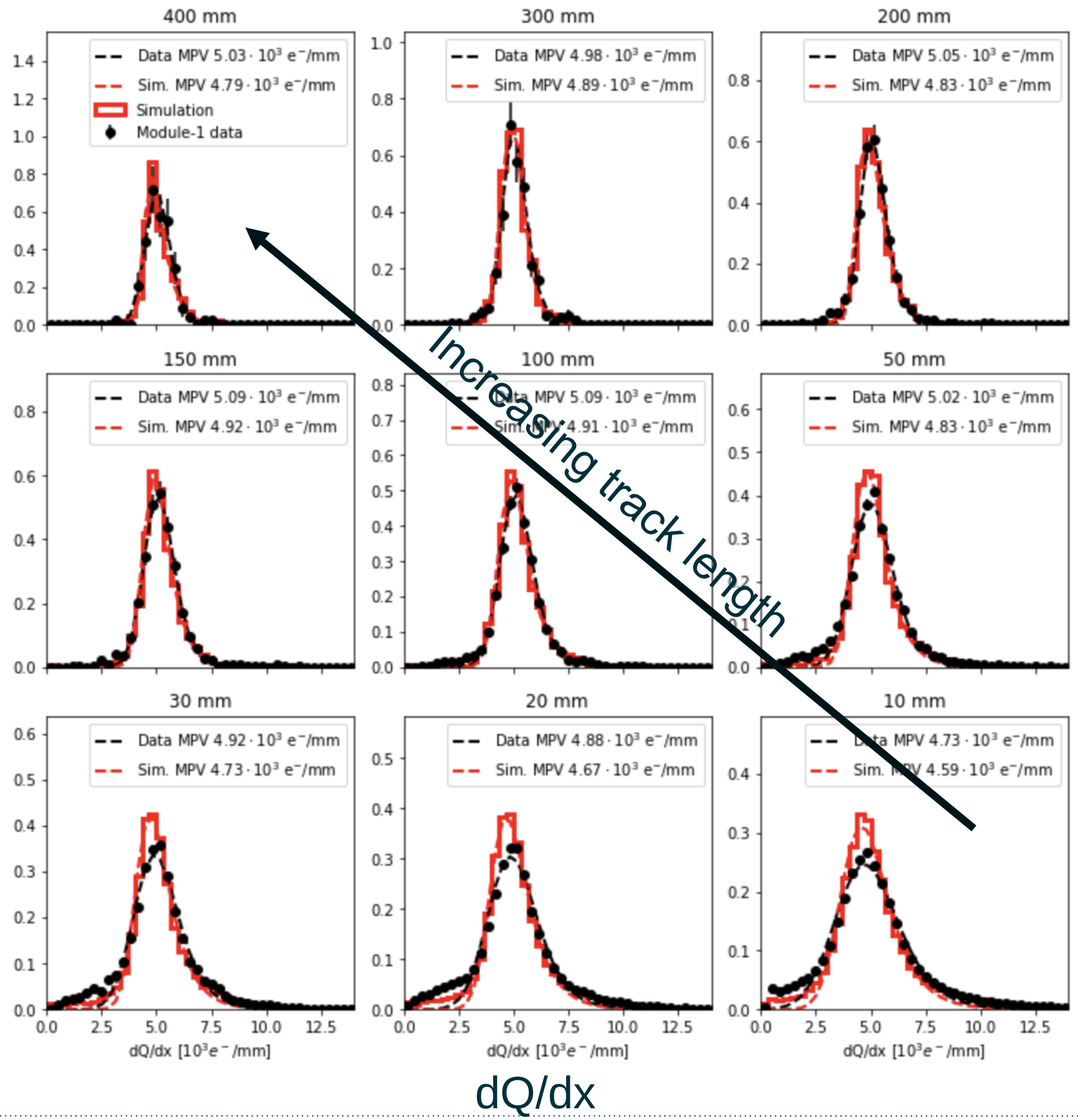
Trigger time relative to track time [-3, 3 μs]

"Highly-parallelized simulation of a pixelated LArTPC on a GPU" publication in preparation

Track-level Cosmic Ray Analysis



- Pixels are continuously active (>100M cosmic ray events recorded)
- Serial data packets stream out of system as channels self-trigger
- MIP response is consistent with expectation and stable throughout data taking



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