

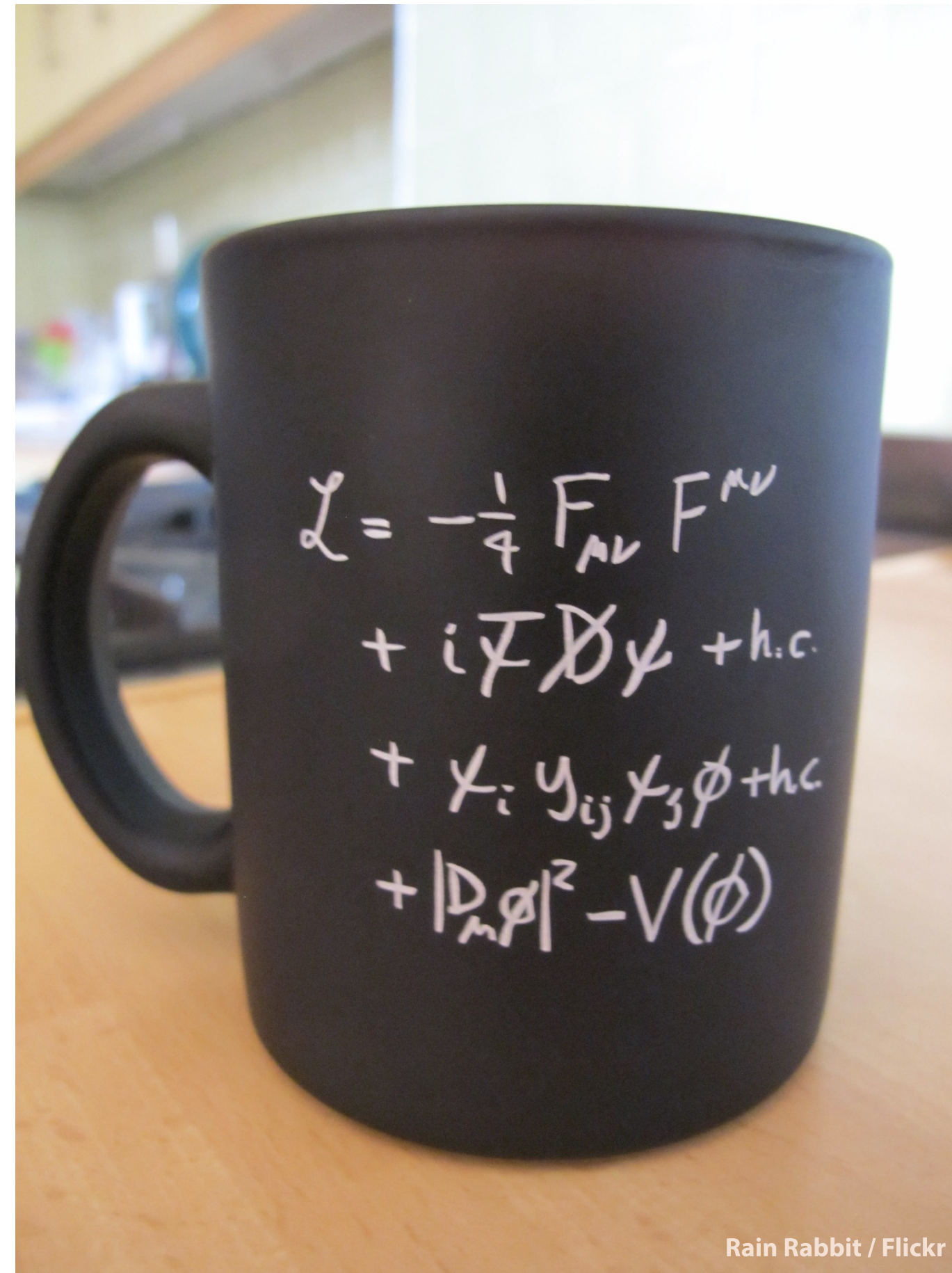
Computational challenges for multi-loop collider phenomenology

- Computational Frontier -

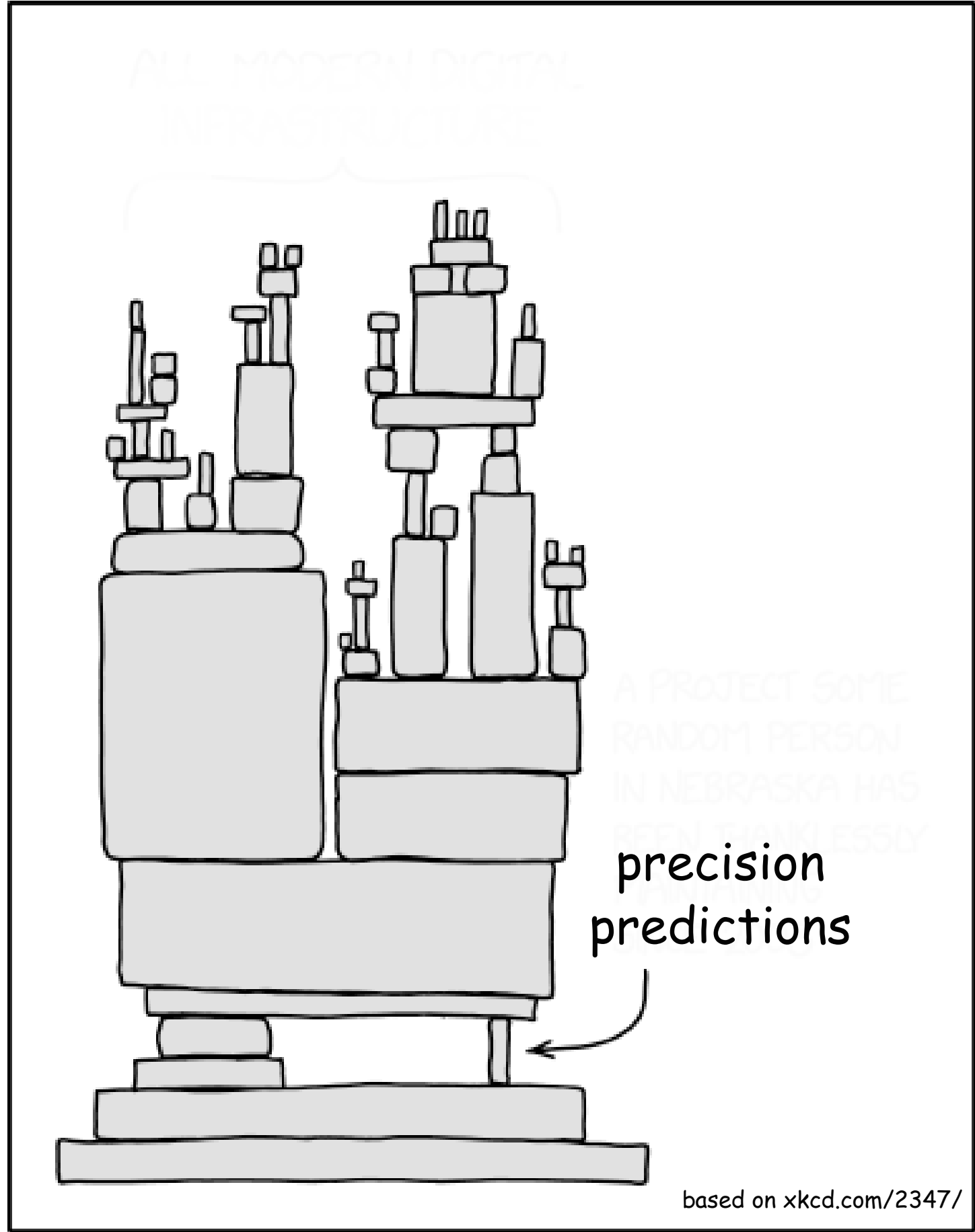
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based on arXiv:2204.04200



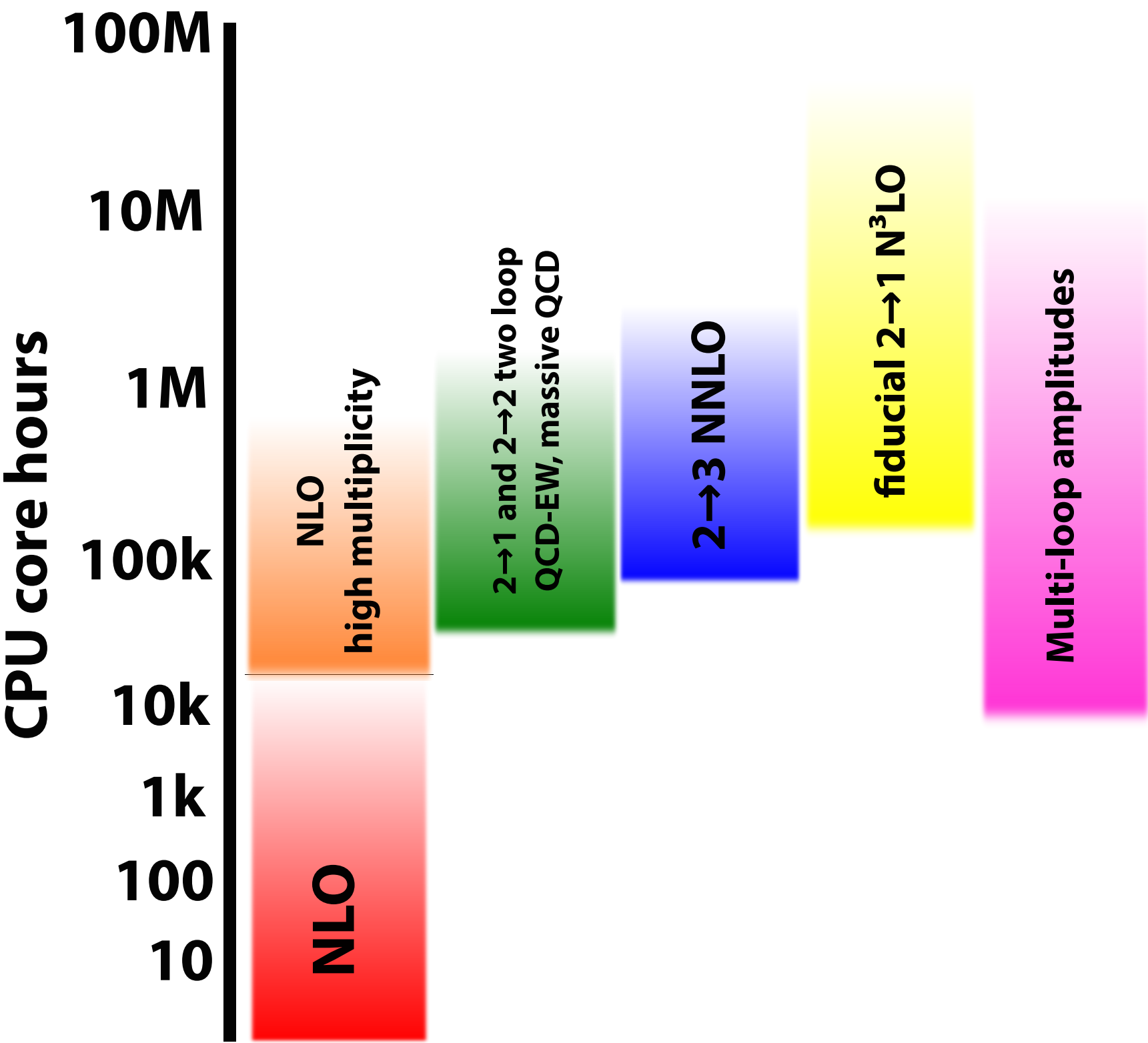
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Multi-loop era: HPC is now standard and a requirement



We surveyed 53 recent state-of-the-art calculations



arXiv:2204.04200

Atypical HPC resource requirements

- most parts CPU dominated (efficient use of GPUs unclear)
- other parts memory dominated (> 1 TB necessary)
- flexible job runtimes (virtualization snapshotting?)

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The worker nodes detail:

- HPE ProLiant XL270d Gen10
- Intel(R) Xeon(R) Gold 6248 CPU @ 2.50GHz
- 8x Nvidia V100-SXM2-32GB with NV-Link
- 768 GB Memory
- InfiniBand EDR connectivity

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Computational challenges for multi-loop collider phenomenology

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- LHC/HL-LHC requires percent level precision for wide range of processes (N^3 LO)
- Shift to significant use of HPC resources (currently $\mathcal{O}(1M - 10M)$ core hours per project)
- Numerical and semi-numerical methods on the forefront, we forecast significant rise
- Atypical resource requirements: CPU dominant; large memory; flexible runtimes
- For U.S. to not lose international competitiveness: hiring decisions
- Advocate for public, open-source, well-documented tools and results

