# Enabling capabilities for infrastructure and work force in Electronics and ASIC design


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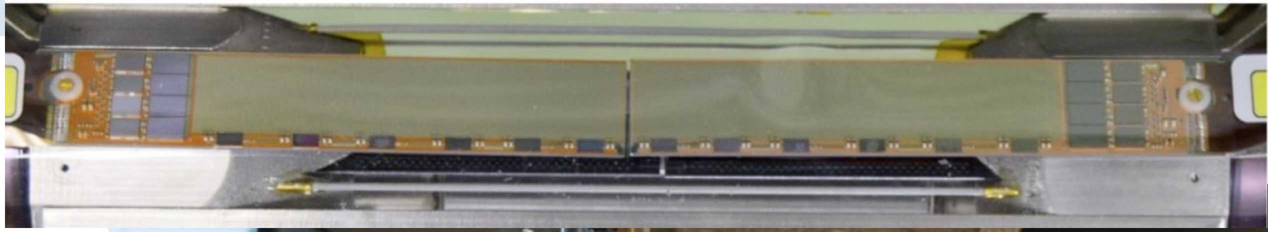
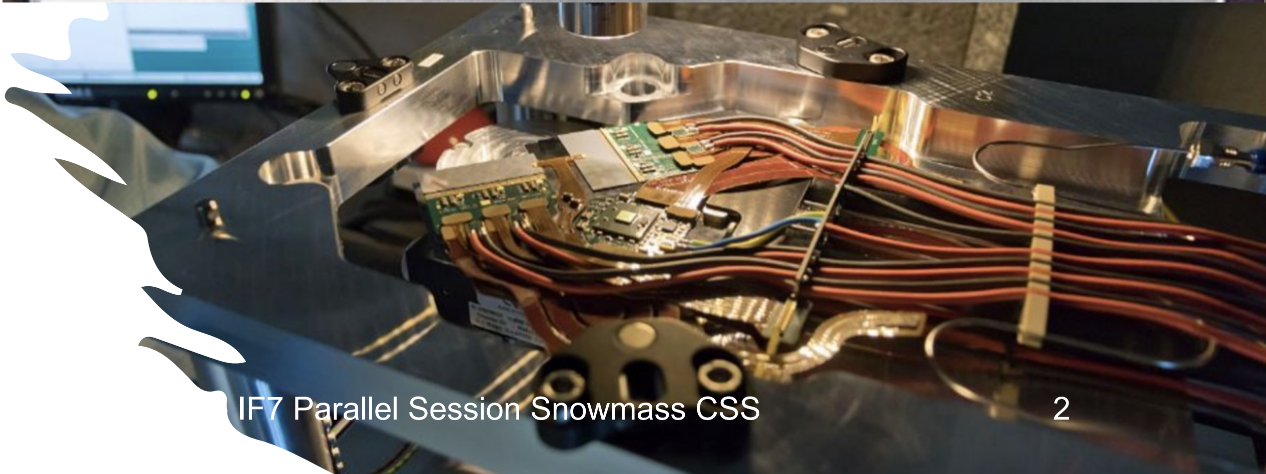
# The ASIC revolution





- Availability of microelectronics has revolutionized modern instrumentation:
    - Improvement in noise performance due to sensor readout integration
    - Smaller feature sized imply better radiation resistance
    - Smaller feature size allow complex DSP to be integrated in front-end ASIC
- Moving into the future performance can scale up considerably, provided that:
    - Shared design tools are implemented
    - Knowledge preservation is maintained
    - Education and retention of the needed work force is achieved

# Future needs

- Experiments planned for the mid-term and long-term future require:
  - Operation at cryogenic temperature
  - Operation in extreme radiation environments
  - Rapid processing of large amount of data of high complexity: the use of artificial intelligence/machine learning techniques should be exploited as much as possible

# ASIC for HEP: the next generation

| Foundry | Broker | Processes | MPW | Dig Cells | Technology |
|---|---|---|---|---|---|
| TSMC | IMEC | 250nm | yes | yes | CMOS |
| | and | 180nm | yes | yes | CMOS |
| | MUSE | 130nm | yes | yes | CMOS |
| | | 90nm | yes | yes | CMOS |
| | | 65nm | yes | yes | CMOS |
| | | 40nm | yes | yes | CMOS |
| | | 28nm | yes | yes | CMOS |
| Global Foundries | Direct | 22nn FDX | yes | yes | CMOS |
| | | 55nm | yes | | CMOS |
| | | 130nm | yes | yes | CMOS |
| Intel | Mosis | 22nm | yes | yes | FFL |
| TowerJazz (sub-div. Intel) | Direct | 350nm | No | yes | BiCMOS |
| | | 180nm | yes | yes | BiCMOS |
| | | 65nm | yes | yes | BiCMOS |
| Skywater (OA PDKs) | Direct | 130nm | yes | yes | CMOS |
| | | 90nm | yes | yes | CMOS |
| Specialty Foundries | | | | | |
| Xfab(www.xfab.com) | Direct | HV 1um, 0.6um | yes | | |
| | | HV 350nm | | | |
| | | HV 180nm | yes | | |
| | | 1um | yes | MLM | CMOS&MEMS |
| | | .8um | yes | MLM | Sensors RF |
| | | .6um | yes | MLM | SiC & GaN |
| | | 350nm | yes | MLM | 3D integration |
| | | 180nm | yes | MLM | MicroFluids |
| Lfoundry (www.lfoundry.com) | Direct | 150nm | yes | yes | CMOS |
| | | 110nm | | | HV LDMOS 80-200V |
| | | | | | Opto |
| | | | | | RF |

Many technologies and feature sizes planned, increasingly costly⟹ need to optimize development cycles

Application to HEP experiments require operation in non-standard environments [high radiation or cryogenic temperatures…]: characterization of the technologies in realistic environments is key

# Leveraging on government supported foundries

- ❑Synergies with **DOE-NNSA, DOD**, NGA, NSA, NASA

Shared radiation requirements

- ❑MESA facility at Sandia Lab
- ❑MIT Lincoln Lab

Secure access for 'mission critical' tasks 350 nm→90 nm

# FPGAs in HEP

- Traditionally FPGA utilized in DAQ boards between front-end and online computers
- As complexity increases, several opportunity arise:
  - Flexible architectures for data concentration
  - Clustering algorithms, possibly including machine learning or artificial intelligence
- Dominant industrial partner Intel/Xilinx
- Training on synthesis with RTL languages, [Verilog, VHDL] & other high-level interfaces
- Collaboration between HEP laboratories and universities with shared resources and knowledge, development of shared libraries & standardization of approaches are important

# Simulation and common infrastructure needs

- To optimize R&D cost, more detailed design verifications needed:
  - Sophisticated CAD tools are needed to verify electrical performance, in harsh environmental conditions:
    - Stringent timing requirements for HL-LHC detectors
    - Harsh radiation environments for HL-LHC detectors: effects of TID and SEU rates need to be assessed
    - For LAr neutrino detectors operation in cryogenic environment
- Shared designs: collaborative efforts using repositories and version control (GIT,cliosoft)
- Shared repositories allow knowledge retention and broaded educational platform [online tutorials, IP common designs]

# Commonly used tools

| Platform | Tool | Description |
|---|---|---|
| Cadence | | |
| | Virtuoso | schematic capture and layout editor |
| | NCverilog | previous verilog simulator |
| | Xcelium | current verilog simulator |
| | Spectre | SPICE analog simulation |
| | Genus | synthesis of gate-level logic from RTL |
| | Conformal | Logical equivalence checker |
| | Joules | RTL-based power estimator |
| | Liberate | Liberty (timing) file for PnR |
| | Innovus | Floorplan; Place and Route |
| | Voltus | Power simulations |
| | Assura / PVS | one of several DRC/LVS tools |
| | Tempus | timing signoff |
| Siemens | | |
| | Calibre | widely used DRC/LVS |
| | Eldo / Eldo Premier | SPICE analog simulator / fast SPICE |
| | ADvancedMS | Mixed-mode (analog and digital) simulator |
| | Questa (Modelsim) | RTL-based digital simulator |
| | AFS | Fast SPICE |
| | Tanner Suite | Low-cost design flow |
| Synopsys | | |
| | HSpice | SPICE simulations |
| | FineSim | fastSpice for full chip simulations |
| | DC Compiler | RTL synthesis |
| | IC Compiler/IC Compiler II | Floorplan, Place & Route |
| | PrimeTime | Timing signoff |

# Developing ASIC designer workforce

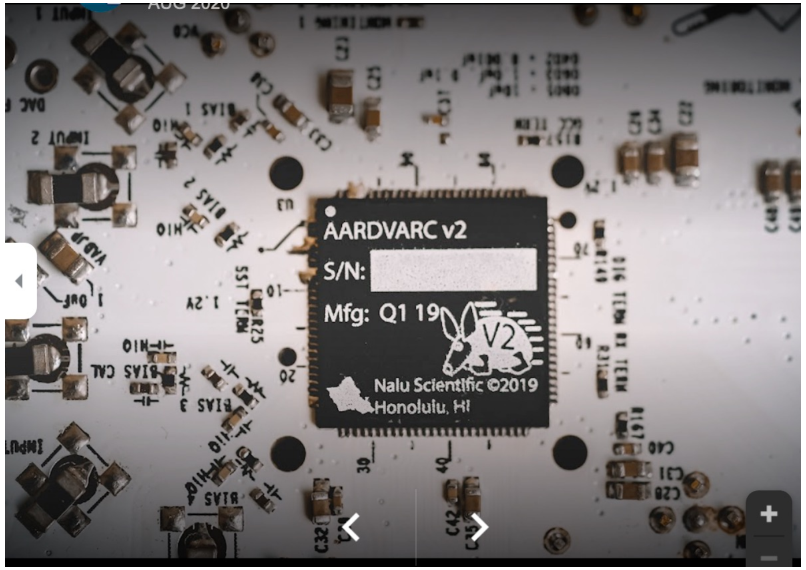
- We need to **educate** and **retain** a broader and more diverse instrumentation work force
- DOE sponsored traineeship programs:
  - HEPIC (high energy physics integrated circuits): several California universities (UC Santa Cruz, UC Davis, Stanford) and national laboratories (SLAC, LBL…)
  - TRAIN-MI (High energy  physics instrumentation traineeship): curriculum in instrumentation and research opportunities
- BRN recommendation:  ”**such skilled personnel are highly sought after by industry and maintaining a pipeline of students and early career engineers and scientists with these skills is essential**”

# Develop and retain ASIC designer workforce: new ideas

- ❑Expand virtual component of existing programs to broaden access
- ❑Expand collaborative programs between laboratories and universities on generic R&D efforts and workforce training without restrictions to being work associated with a lab-sponsored project
- ❑Broaden access to these education tools to students and junior researchers from universities with less established programs

# Collaboration with industries

Nalu Scientific




- ❑SBIR (Small Business Innovation Research) & STTR (Small Business technology transfer) enable the most capable domestic small business to engage in federally supported R&D and development of new products in collaboration with HEP researchers.
  - ❑HEP scientists can develop the instruments of the future
  - ❑Commercialization and broader use is achieved in synergistic fashion

# Towards a US R&D program

- ❑Examples: CERN R&D
  - ❑WP2.1 [Alice ITS3 as a main driver $\Longrightarrow$ access to TowerJazz 65 nm process]
  - ❑28 nm forum – platform to develop the technolofy for the future
- ❑Establishing a US based R&D program would facilitate:
  - ❑Stabilization of designer work force in between projects
  - ❑Reduce the development time of new architectures
  - ❑Improve and broaden the training of young scientists
  - ❑Foster innovation through collaborative efforts between universities and laboratories
- ❑Suggestions:
  - ❑Scalable pixelated detector systems (cryogenic environment LArPix)
  - ❑ps timing architectures for high radiation environment operations
  - ❑…

# Conclusions and recommendations

- ❑Resources should be identified to support:
  - ❑Consolidation and broader availability of design tools, technology modeling and basic IPs in a well documented web-based interface accessible to the US HEP community
  - ❑Broaden educational opportunities for young scientists interested in ASIC designs
  - ❑Establishment of RD efforts connecting national laboratories and universities to develop the microelectronics needed for future experiments (ASIC & hybrid circuit designs, FPGA algorithms and integration in the readout architecture of complex systems)
- ❑Community convergence on shared designs and collaborative efforts needs the identification of agreed-upon design and verification tools