Community Summer Study

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IF07: Electronics for Fast Timing

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Electronics for Fast Timing

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Picosecond timing and 4D detectors

- Timing resolution increasingly important for reconstruction in high-luminosity colliders
- Background rejection for dark matter searches and neutrino detectors
- 4D detectors (e.g. Muon collider)
- Enabled by advancement in:
  - Fast electronics
  - Fast detectors

Signal and Noise

$$\sigma_t \approx \sigma_n \frac{\delta V}{\delta t} \approx t_r \frac{noise}{signal}, \sigma_n^2 \approx \frac{C_L^2(4kTA)}{g_m T_a}, \sigma_t \approx \frac{C_L}{\sqrt{g_m t_a}} \frac{\sqrt{t_a^2 + t_d^2}}{signal}$$

In a system dominated by noise-associated jitter, we want to:

- Maximize S/N
- Minimize risetimes (amplifier and detector)
- Maximize g_m
- Minimize capacitance
- (cool the system)

Complications in segmented detectors:

- Non-uniform pulse shapes
- δrays, landau fluctuations, and track angle can all affect pulse shape and resolution
- Non-uniform weighting fields

These variations might be large enough to require full waveform digitization (especially in calorimetry)

Fast Timing Sensors

see Simone Mazza presentation:
https://indico.fnal.gov/event/22303/contributions/246183/

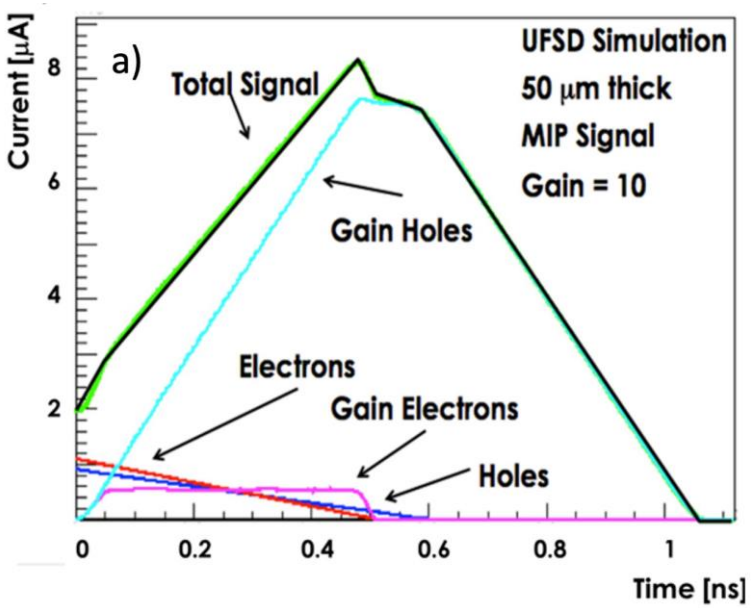
Sensors: Ultra-fast Silicon

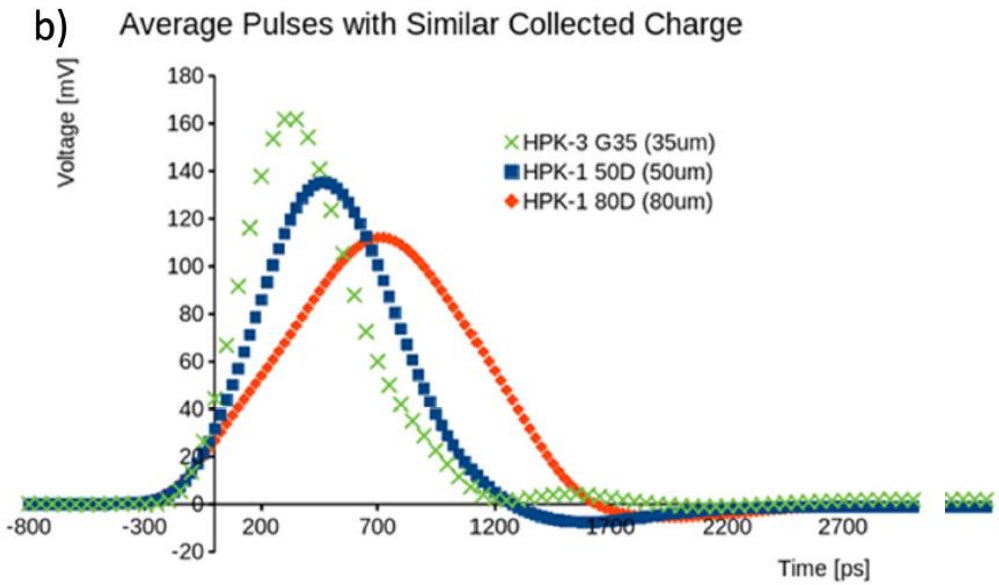
No internal gain (e.g. 3D sensors)

- Limited signal so they must maintain the fast rise time of the electron collection

Internal gain (e.g. LGAD)

- Internal gain boosts hole signal gain by x10-20
- Rise time and signal height depend on detector thickness
- Both rise time and signal height depend on detector thickness
- Landau factor limitation favors thinner sensors



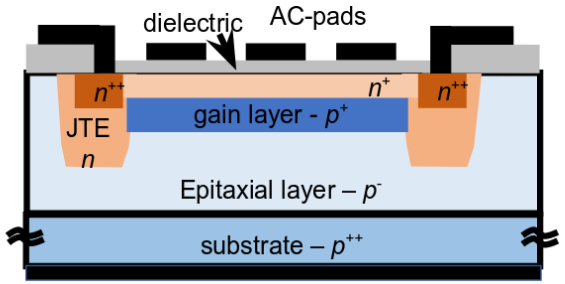


Sensors: LGAD

- Both CMS (ETL) and ATLAS (HGTD) are developing large-scale timing layers based on LGAD of 50 µm thickness and 1.3 mm pitch.
- Readout ASICs optimized for sensor capacitances of ~5 pF and ~35 ps time resolution at a power of ~ 5 mW/channel
- The next generation of LGAD will require a position resolution of 5-10 um, and a typical pitch will be < 500m, in addition to a factor 2 improved time resolution
- Ongoing programs for LGAD application at the EIC and PIONEER

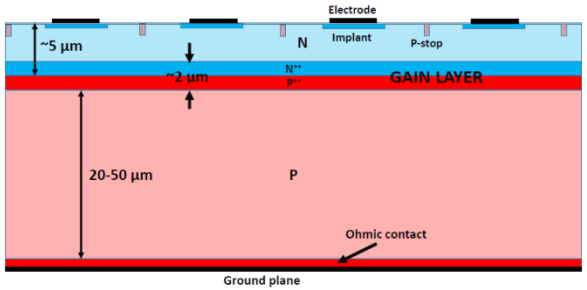
AC-LGAD

- Charge sharing between pixels allows interpolation for position resolution of O(10 µm)
- Lower pad capacitance of 100-200 fF
- Recent test beam demonstrated 5 µm and 30 ps resolution



Deep-Junction LGAD

- High-field p/n junction buried a few microns from the patterned electrodes at the interface
- Small electrodes lead to lower capacitance, with timing resolution comparable to LGAD and fine spatial resolution



Sensors: Micro-pattern gaseous detectors

- Provide excellent time and spatial resolution over large areas
- CERN RD51 has explored both detectors and electronic system that have demonstrated ~10 ps resolution
- The PICOSEC project uses a Cerenkov radiator and a photocathode to achieve 10's of ps resolution.
- Ps-level system resolution of larger scale MPGD readout requires precise clock distribution, integration of fast amplifiers and TDCs as well as integration of waveform sampling systems.
- A Scalable Readout System (SRS and SRSe) has been developed which provides both vertical links between front end ASICs and readout and horizontal links among detector systems
- Snowmass Whitepapers:
  - *Micro Pattern Gaseous Detectors for Nuclear Physics*
  - *MPGDs: Recent advances and current R&D*

Sensors: Pixel Detectors

Silicon sensors with no internal gain can achieve ps-level timing by limiting noise (small input capacitance) and by controlling the pulse shape

- E.g. NA62 Gigatracker achieved 65 ps resolution with 300 um pixel size
- Power density for small pixels is one of the main limitation for fast timing

3D sensors can achieve very fast timing. 3D trenched detectors limit field non-uniformities and have achieved 27 ps resolution

Induced-current sensors: The induced current is instantaneous and can provide a very fast rise current pulse whose magnitude and polarity depend on the pixel weighting field. Pixel detectors with very low load and interconnect capacitance can utilize this initial current pulse to provide both fast timing and detailed information on the track location and angle. Complex pulse shapes.

Sensors: Light Detectors

Cerenkov light and fast scintillators such as LYSO provide intrinsically fast signal sources

- The microchannel plate has reduced the time dispersion due to the electrons travel time through the PMT.
- The **LAPPD** collaboration has further evolved the MCP, with large area, lower cost, and a choice of anode structures (pixelated, with charge sharing or charge division, or capacitively coupled)
- LAPPDs are now in limited production and have demonstrated time resolution less than of 50 ps

Semiconductor-based photodetectors such as **SPADs** and **SIPMs** can provide 10 ps-level time resolution for scintillation light and charged particles

- Developments such as digital and **3D SIPMs** can achieve improved capabilities, position, and time resolution by replacing the analog summing node with digital micropixels

Other photodetector technologies under study capable of ps resolution include semiconductor **quantum dot-based devices**, and **ZbO:X ceramics**

Calorimeters

Electromagnetic and Hadronic calorimeters have different requirements electronics (prompt and with well defined shape, vs slower with substantial energy and spatial fluctuations).

→Time resolution required depends on the application and range from sub-ns to a few ps.

See whitepaper: *Precision Timing for Collider Experiment based Calorimetry*

Electronics challenges include:

- Very high system dynamic range
- Achieving ps resolution in large, distributed multi-channel systems
- System interconnection with preservation of time information
- Time to Digital Conversion (TDC design)
- Local processing and utilization of the signal and transmission of the results
- Waveform digitization and parameter extraction, particularly for dual readout calorimeters where much information is encoded in the waveform itself.

Fast ASIC R&D

a non-exhaustive example list

SiGe Amplifiers

- UCSC and Anadyne, Inc collaborated on a SiGe readout IC with 10ps resolution for 5fC signal at 0.5 mW/channel.
  - Preamplifier and TOT discriminator suitable for low repetition rate and quiescent power
  - A constant-fraction (CFD) discriminator would be more suited for rates > 100 MHz. But CFD loses pulse height information, which can be useful for highly segmented detectors
- Process node: diminishing returns for transistors > 25 GHz when dealing with 1-2 GHz signals typical of ultra-fast silicon detectors. For BiCMOS processes, the speed of the CMOS backend for digital signal processing might be a more important consideration (130/90/65 nm)
- Monolithic silicon pixel sensors in SiGe HBT technology from University of Geneva have also demonstrated < 50 ps resolution.

Full digitization ASICs

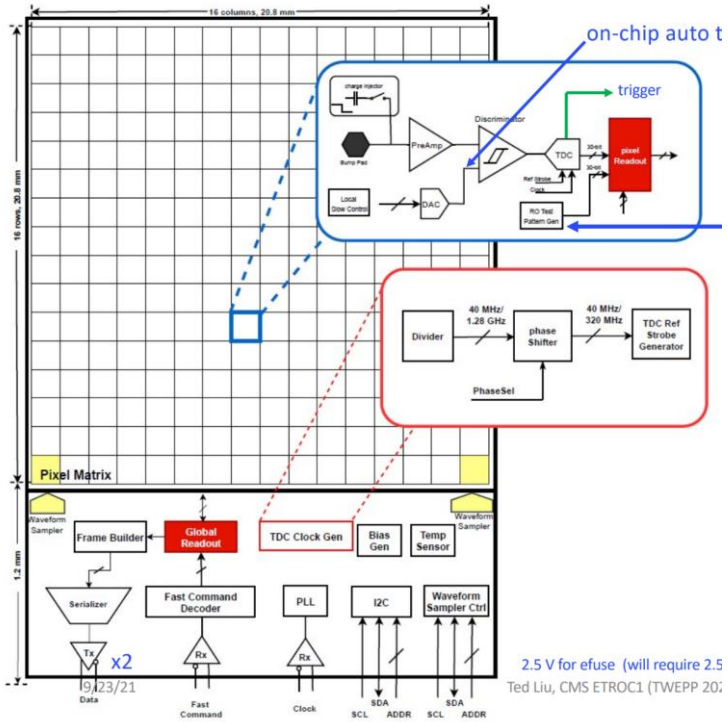
- Waveform digitization useful when timing precision affected by pile-up, time-walk, baseline wander, and shape variation; as well as environmental factors (e.g. temperature, sensor aging and radiation)
- UCSC and Nalu Scientific collaborating on the design of a high-channel density and scalable radiation-hard waveform digitization ASIC with embedded interface
  - V1 (Jan22) designed for 50 µm AC-LGADs. Later versions will target 20 µm.
  - Input TIA to be tunable to accommodate different sensors.

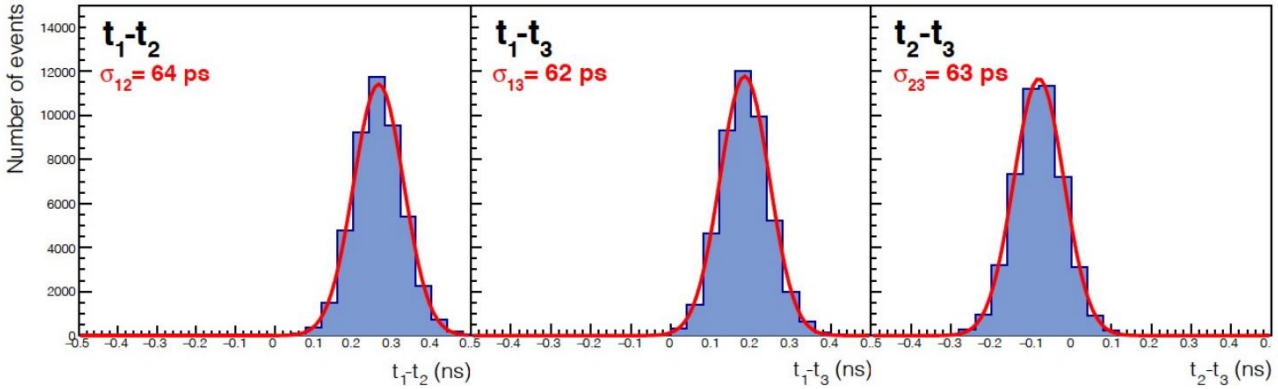
FAST ASIC family (INFN)

- Family of ASICs in 110 nm CMOS for UFSD readout
  - TOFFEE (2016), FAST1 (2018), FAST2 (2020), FAST3
  - Target resolution of 25 ps, rates up to 200 MHz, optimized for input capacitance of 3-6 pF
  - FAST3 will have 32 channels, resolution < 40 ps, TOA and TOT

ETROC (Fermilab, SMU)

- 65 nm, 16 x 16 channel, reticle–size ASIC for CMS Endcap Timing Layer (LGAD)
- Time resolution of 40-50 ps per hit (30 ps per track with two timing layers). < 60 ps at 3000 fb^{-1}
- TDC is required to consume less than 200 µW for each pixel at the nominal hit occupancy of 1%
  - To meet the low-power requirement, the ETROC team uses a single delay line for both the TOA and the TOT measurements without delay control
  - A double-strobe self-calibration scheme is used to calibrate TDC bin size under process, temperature, and power supply voltage variation
  - The TDC has a precision of 5.6 ps (TOA) and 10.4 ps (TOT) with non-linearity correction





From preliminary analysis of the data from ongoing beam test at FNAL, the time resolution of each LGAD+ETROC1 layer has reached:

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)} \quad \sim 42 - 46 \text{ ps}$$

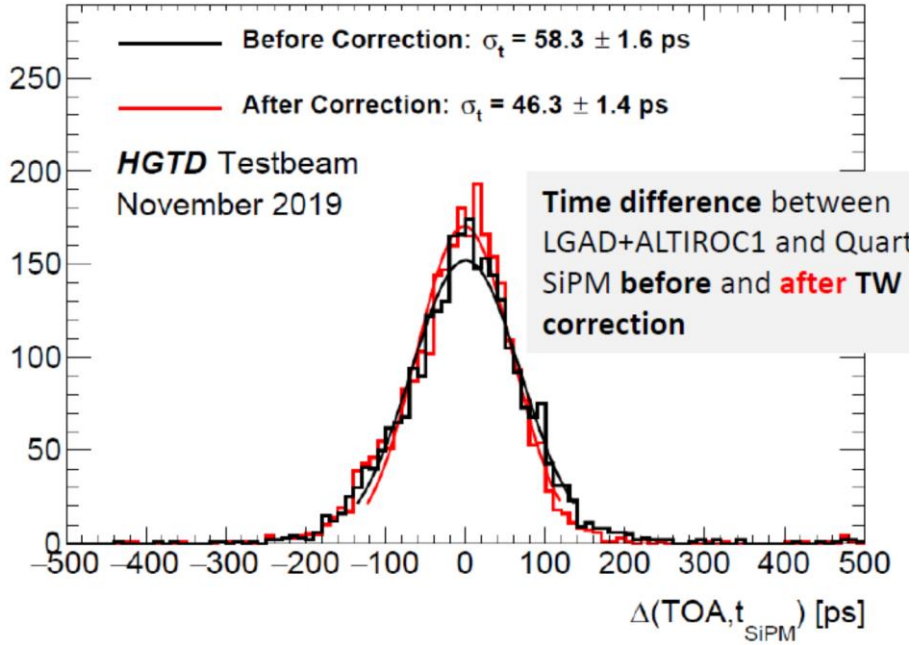
(with LGAD HV=230V for all three channels)

This measured time resolution includes all four contributions in the table

ALTIROC (Omega, SLAC, SMU)

- 130 nm, for ATLAS High-Granularity Timing Detector (HGTD)
- 25 ps time resolution, with 25 channels
- Each channel integrates an RF preamplifier, followed by a high-speed discriminator and two TDCs for TOA and TOT measurements, as well as a local memory
- The TDC, designed by SLAC, is based on a Cycling Vernier Delay Line with a resolution of 20 ps and a maximum range of 2.5 ns (7 bits dynamic range).

Altiroc1_V2: TEST BEAM measurement



ASIC	Technology	Pitch	Total Size	Power	TID tolerance
ALTIROC	130 nm	1.3 mm	19.5 x 19.5 mm^2	5 mW/ch	2 MGy
ETROC	65 nm	1.3 mm	20.8 x 20.8 mm^2	3 mW/ch	1 Mgy
RD53A	65 nm	50 um	20 x 11.6 mm^2	< 10 uW/ch	5-15 MGy

FCFD0 - Fermilab Constant Fraction Discriminator ASIC

Goals:

- Develop a robust fast-timing discriminator for fast detectors
- Time resolution of 30 pS or better
- Appropriate for use in IC pixels
- Easy to use: one measurement per hit, no corrections required
- Stable: no repeated calibrations and threshold adjustments
- Very low dead-time after a hit (~ 25 ns)
- Prototype tailored to LGADs, but concept applicable to other UFSD

Approach:

- Adapt the Constant Fraction Discriminator (CFD) principle for a pixel – when a CFD is paired with a TDC, one time measurement gives the final answer. System is ready again for another measurement soon after.
- Modify the classical CFD approach to eliminate the need for pixel-by-pixel trimming or compensation
- Design an on-chip charge injection circuit that can deliver a wide range of charge pulses
- Implement an on-chip time-to-voltage converter with precision of ~ few ps to enable easy measurement of discriminator output delay and jitter.

Results:

- Recently tested with CMS LGADs, measured 20 ps with laser. Results with beta source coming soon.

Technology-related ASIC developments

TSMC 28 nm CMOS:

- CERN R&D WP5 has promoted the selection of 28nm CMOS node as the next step in microelectronics for HEP designs,
- based on performance, but also availability and costs of MPWs.
- Twice as fast and allows 4-5x circuits densities than 65nm.
- SLAC has started the design of TDCs in 28nm technology node with target resolutions of 10-50 ps.

GF 22nm FDSOI:

- Used extensively by Fermilab for cryoelectronics for both Quantum projects as well as cryogenic detectors
- Small geometry, high F_t and F_{max} , high self gain and high current efficiency of FDSOI makes it a good candidate for fast timing.
- Fermilab recently prototyped a 22nm cryo TDC for 5 ps resolution and >10ns range (7b fine, 10b coarse), <0.5mW

3D integration:

- This technology enables micron-level interconnections between layers of sensors and thinned electronics and deployment of heterogeneous stacks of sensors and readout. Smaller capacitance and interconnects translates into faster timing, smaller power

Monolithic LGADs:

- While modern CMOS technologies offer a wide range of possibilities and seem compatible with most of the LGAD process and front-end, some customizations appear unavoidable, for example the addition of the gain layer. LGAD variants, such as AC-LGADs, should also be compatible

R&D directions

Foundry Access

- Foundry access and process qualification must be an integral part of R&D for fast timing (CERN model)
- With 28nm bulk CMOS likely becoming the default choice for the next decade, a large collaborative effort for process and IP developments in this node, along the RD53 model, will be highly beneficial for the community.
- Many applications will continue to require different processes, e.g.
  - SiGe for high-speed,
  - FDSOI for high speed and cryogenic operation,
  - epitaxial and high-voltage processes for MAPS,
  - and legacy nodes for cost and simplicity.
- Valuable ability to work with some Foundries on process optimization.
  - HR-MAPS with Tower
  - CCD development with MicroChip
  - 90nm Skywater/MIT-LL

Front-end amplifier

- Design and optimization is critical for fast timing
  - S/N → jitter
  - Power consumption
  - Input capacitance
  - Etc
- Emphasis on Trans-impedance amplifiers (TIA) to preserve the fast current signal (vs. charge sensitive readout)
  - Careful design considerations for stability and current draw
  - Design depends on radiation, operating temperature, and process parameters
- Experienced analog designers will continue to be at a premium

Digitization

- Depends on the signal source and characteristics
  - E.g. standard LGAD has short signals with uniform weighting field → TOA and TOT sufficient
  - Signals from segmented detector or AC-LGAD more complex → multiple thresholds or waveform digitization

- Time-to-digital converters (TDC):
  - There are a number of established architectures (delay lines, multi-phase clock systems, Vernier, time-to-amplitude) to be adapted for HEP applications and emerging processes
  - Linearization algorithms can alleviate TDC non-linearity and minimize power

- TDC design must continue to improve in precision and power consumption
  - Current ETL and HGTD TDCs serving mm^2-scale pixels. Future pixelated detectors might require 1000x increase in density → TDC per pixel might not be practical
  - R&D for system design with resource sharing for fast time tagging will be required

Signal Processing

- Simultaneous position and timing resolution
  - Detectors with intrinsic charge division, such as AC-LGAD, will have both variable pulse height and shape as function of position
  - Pixels with thickness/pitch > 1 experience varying pulse shapes as a function of electrodes and position
- For ultimate timing resolution, these effects must be compensated, either on or off detector
- Opportunity to employ novel and emerging solutions like ML (front or back-end circuits)

System Design

I/O:

- a highly granular detector may only be able to send Time-of-Arrival(TOA) and perhaps Time-over-Threshold(TOT) with the TOT capability dictated by crossing interval and occupancy. A longer interval between events per may allow more complex per pixel information, from multiple thresholds to waveform digitization.

Power:

- noise and rise time requirements for fast timing require more power
- Correction for δ-rays, non-uniform ionization, and weighting fields requires complex processing

Large area:

- Most sub-75 ps systems demonstrated to date have been in small, well constrained systems or beam tests

Clock distribution:

- CERN White Rabbit: sub-ns accuracy and ps precision of synchronization for large distributed systems
- Optical transceiver can have several ps/degree delay variation. Techniques have been developed for 1 ps resolution for Xilinx Ultrascale transceiver.

Formidable challenges exists, but not insurmountable towards the grand challenge of ps timing

Conclusions

- Detectors and electronics are in a mutually supportive "arms race" moving toward ps resolution for HEP experiments.
- Rapidly evolving device scaling, 2.5 and 3D integration, digitization and TDC schemes, increased data bandwidth, new front and back-end designs and innovative machine learning algorithms will all contribute.
- New fast signal sources such as LAPPDs, SIPMs and LGADs, induced current detectors, and micropattern gas detectors complement the electronics capabilities
- Ultimate time resolution will require a detailed understanding of the experimental environment, optimization and matching of the signal source and front-end, compensation for variations in pulse shape, and utilization of all available information in a pixelated sensor.
- Future experiments may require local filtering of complex events based on time and space information.
- Ultimately, we may employ ASICs using sophisticated 3D architectures incorporating adaptive algorithms and machine learning techniques embedded in on-detector and triggering systems.