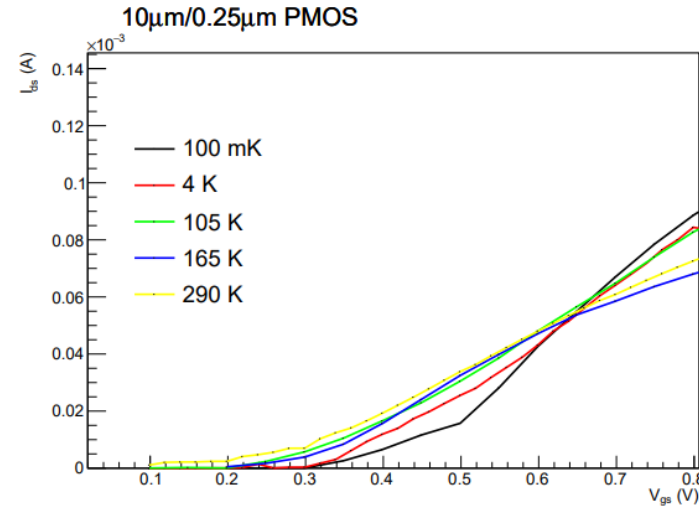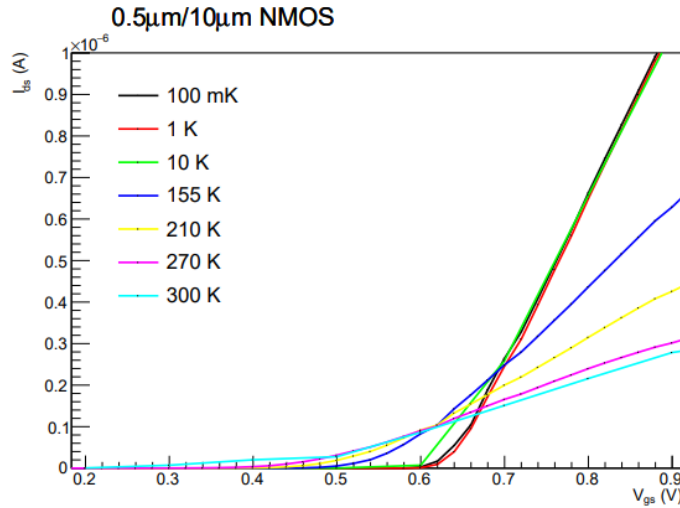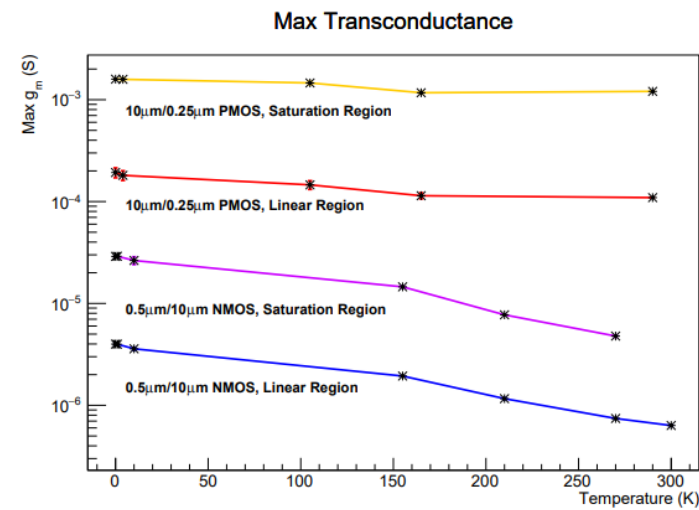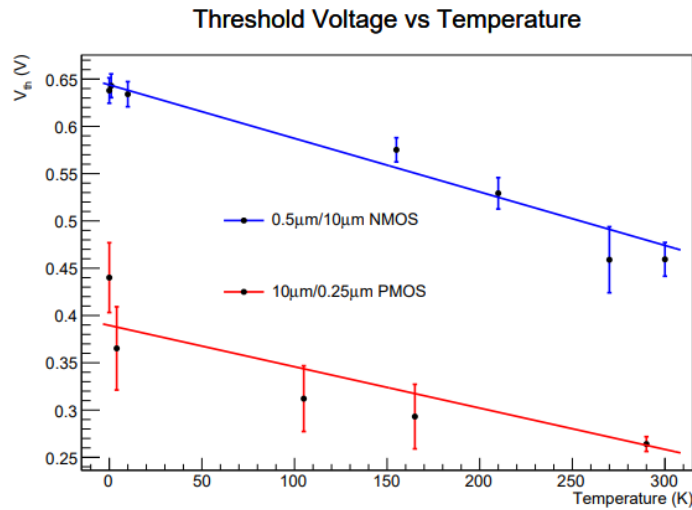# IF07: Cryogenic Readout

180nm CMOS

Gary Varner on behalf of the white paper 7 group

**Snowmass CSS
21-JUL-2022**

Increasingly important

- **Cryogenic sensors**
- **Large liquid nobel detector readout**
- **Quantum computing**

- **Read out increasingly large channel counts at the noise limit, where power is a serious constraint**

- **White paper focuses on 2 aspects:**
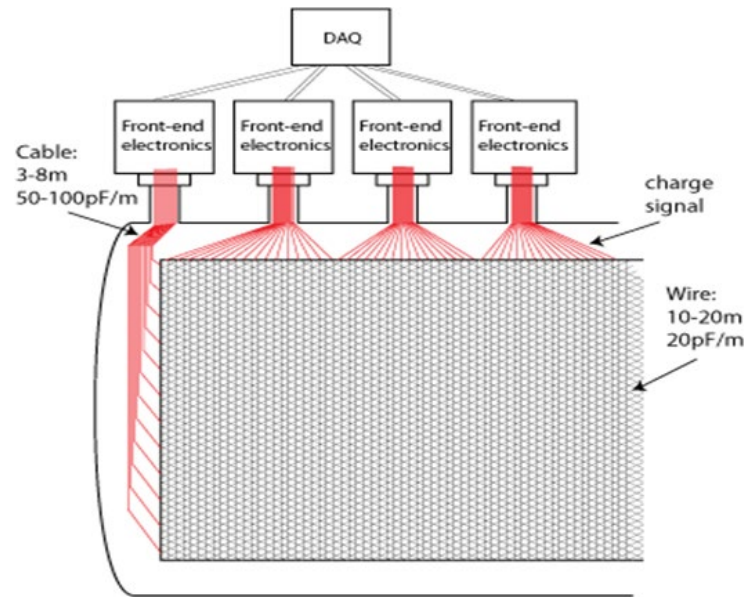 - ❏ **Deep cryogenic (sub-Kelvin)**
  - ❏ **Liquid noble gas**

Issues with Cryogenic design and long-term operation

- **Dominance of tunnel conduction**

- **Freezing of charge carriers**

- **Degradation or destruction due to hot carrier effects**

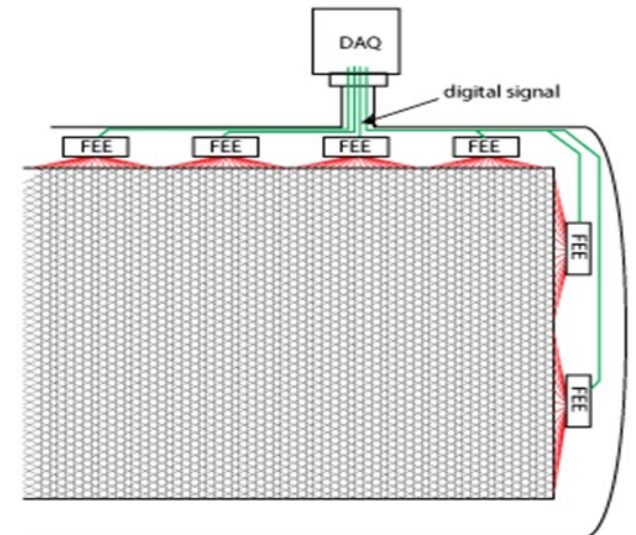- **Vendor-provided models usually only reliable down to -40C**

DUNE Far Detector – Scaling & Low Noise
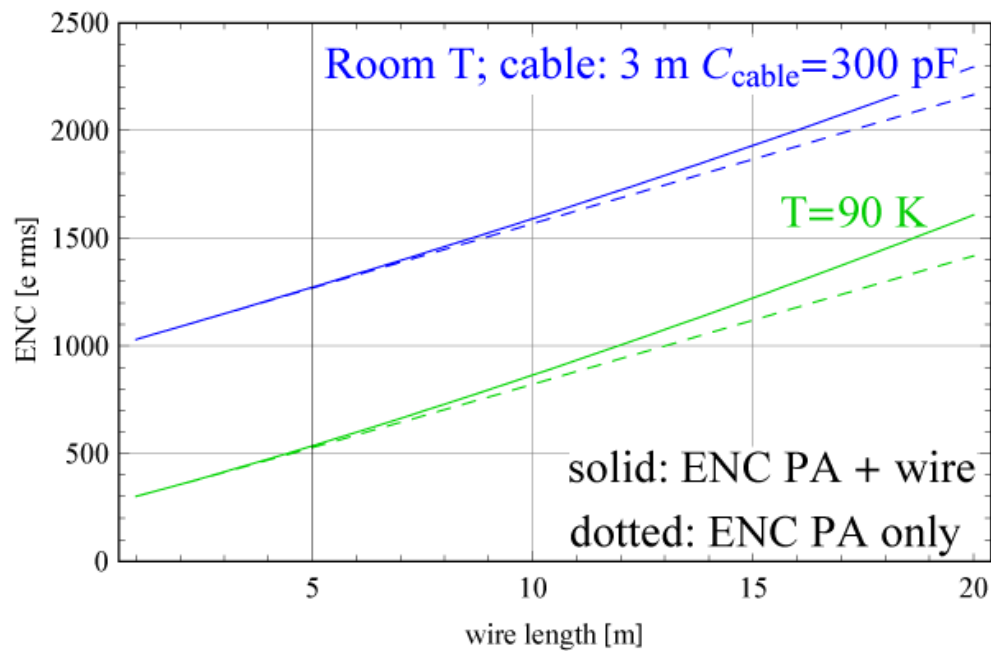
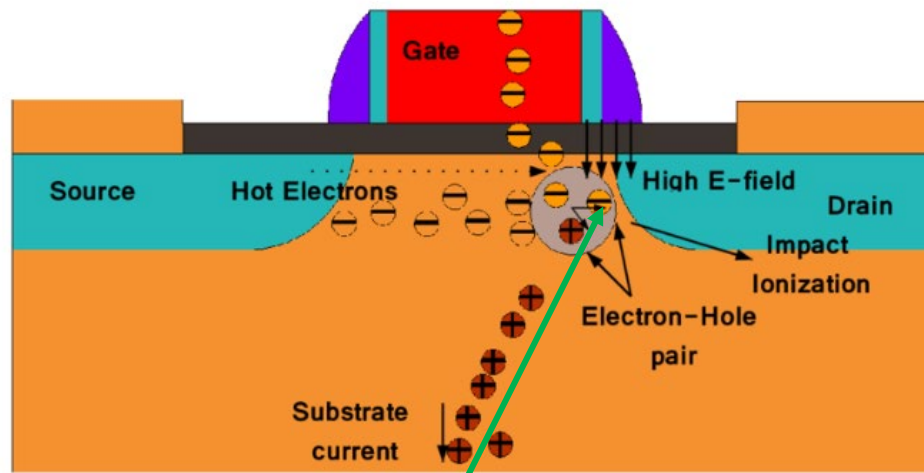**Warm Electronics**

Cold Electronics

JINST 15/T08008

Immersing CMOS electronics in LAr greatly reduces the cabling capacitance, allowing lower achievable noise, and serves as an **enabling technology** for DUNE

Key Electronics Challenge: Long-Term Reliability

Reliability and biasing drift

E. Afacan Thesis, 2016

"Hot" carriers cause
early device aging

- BNL and FNAL conducted lifetime studies and developed design guidelines to assure long-term reliability

- UPenn and FNAL developed a cryogenic compatible standard cell library for 65nm CMOS

LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling

Shaorui Li, Jie Ma, Gianluigi De Geronimo, Hucheng Chen, and Veljko Radeka

- **Fortunately easy to mitigate: reduce VDD & / || increase min. L**

Some current and future developments

- **Impossible to be exhaustive**

- **To give some flavor of current/future design efforts**

- **Along the 2 themes chose to highlight in the white paper**

- **Though will swap order**

DUNE Near Detector technical challenge

The DUNE ND will experience ~10M neutrino events per year. Below is a simulation of neutrino pileup in the ND from a single beam pulse (each color indicates a separate neutrino interaction) not including neutrino background.
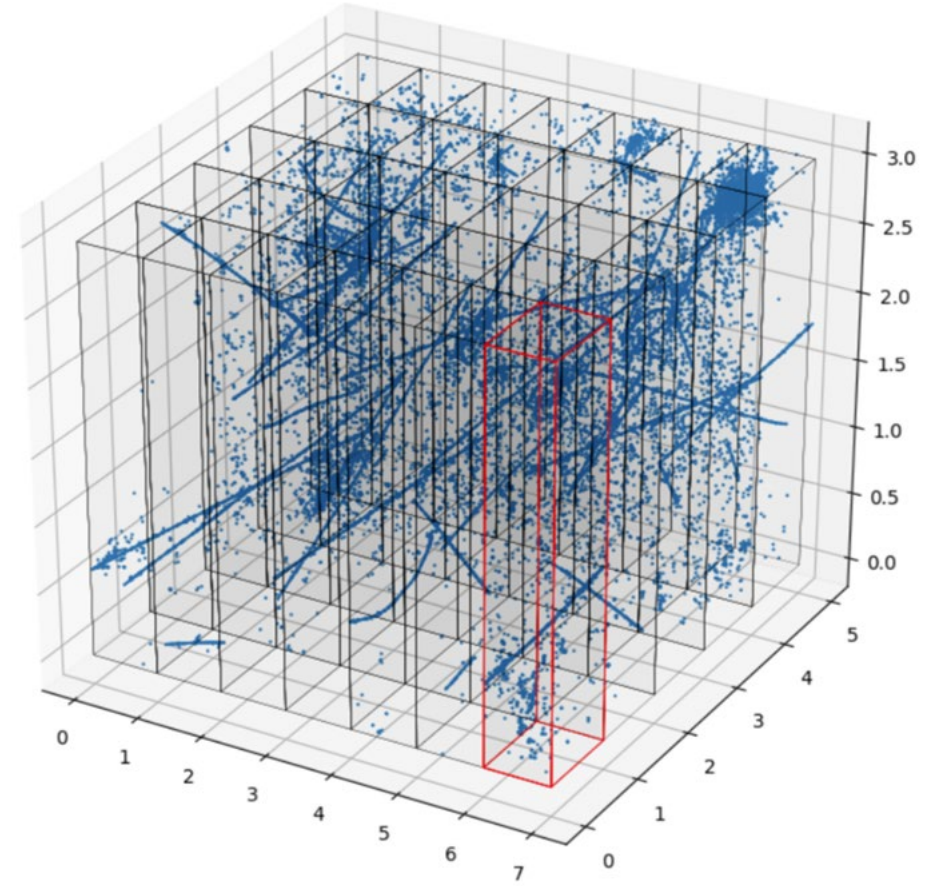

Approximately 50 neutrino interactions per beam spill

LArPix – Liquid Argon Pixel ASIC

Approach: Integrating Amplifier with Self-triggered Digitization and Readout

- 64 channels per ASIC
  - Charge Sensitive Amplifier
  - Discriminator (self trigger)
  - ADC (per channel)
  - Digital Control logic
- Global control logic
- 2k FIFO
- On chip references and bias currents
- Only decoupling capacitors needed
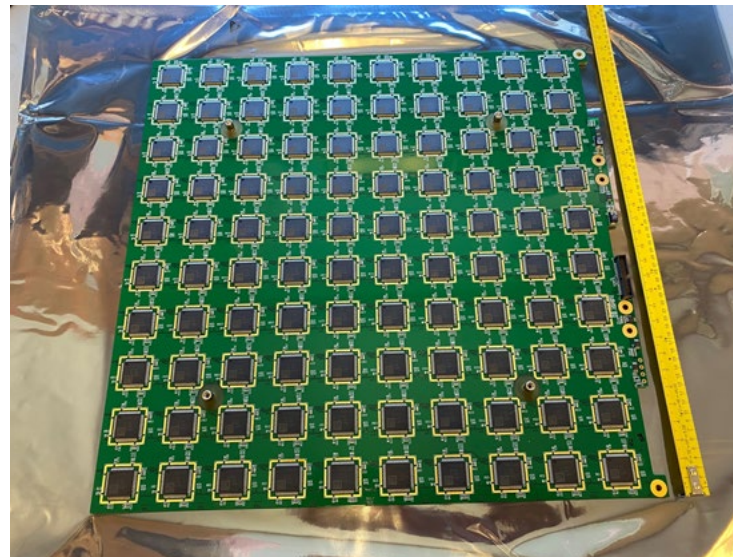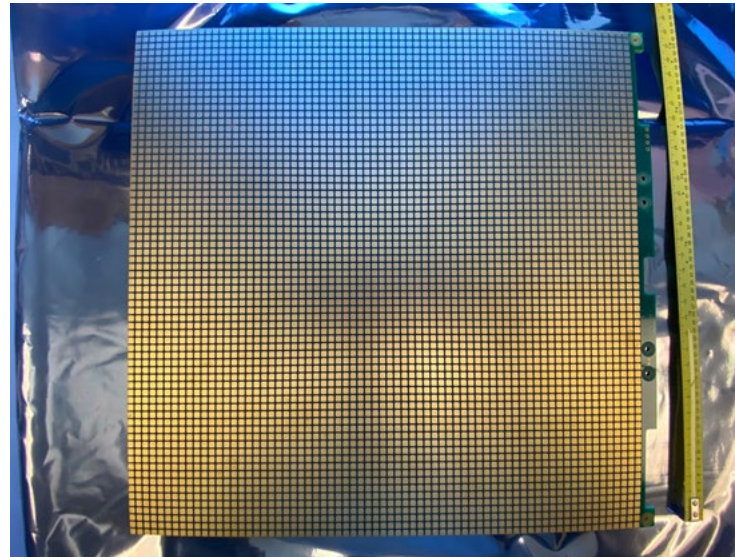- Immersed in Liquid Argon (-200° C)
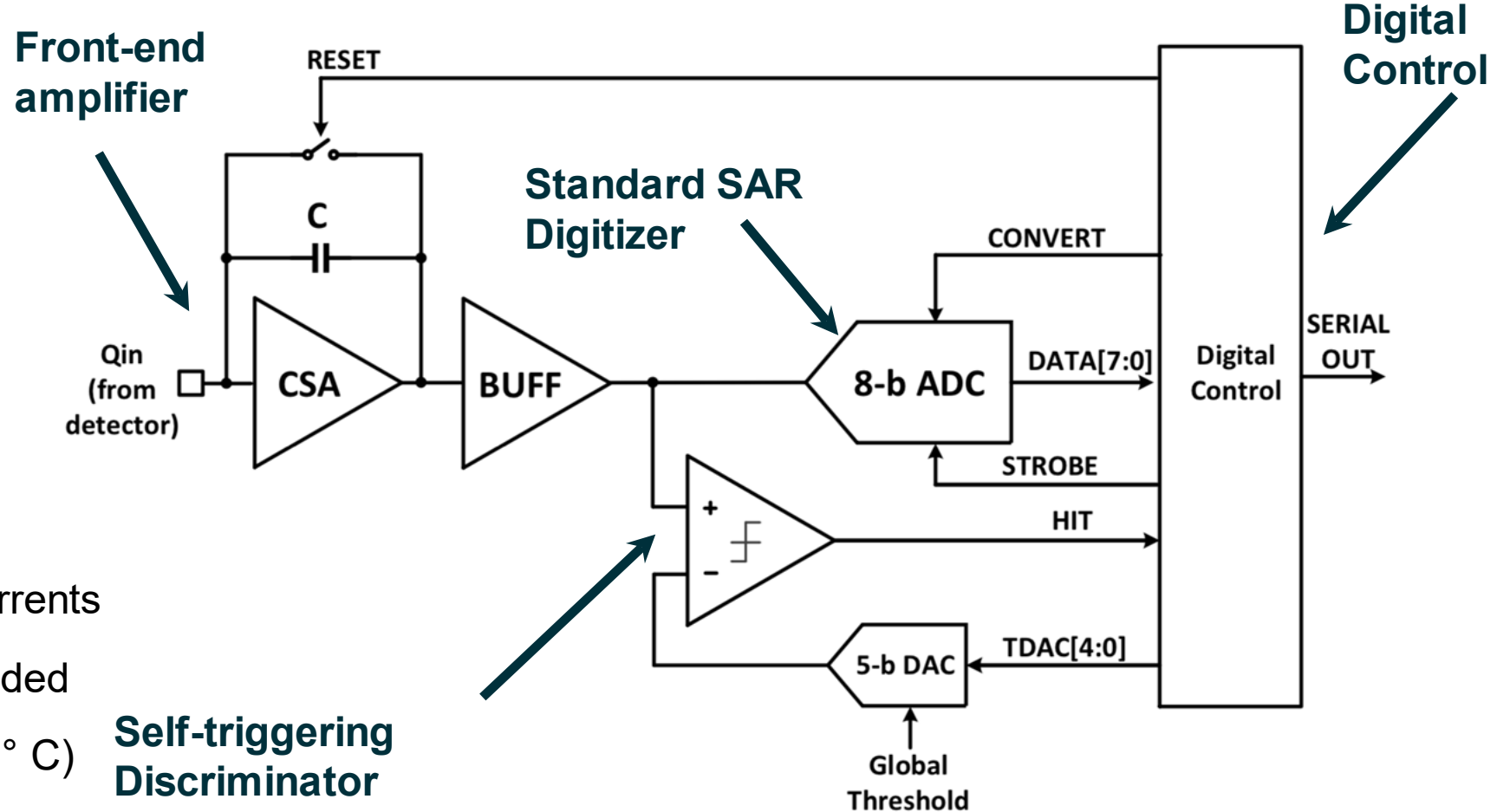
Achieve low power: avoid digitization and readout of mostly quiescent data.

8

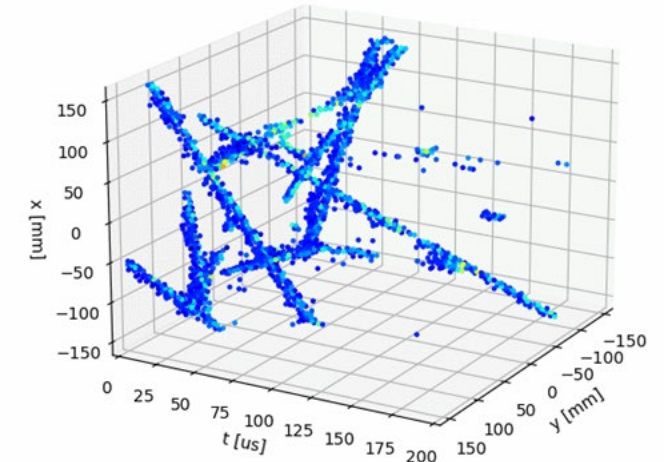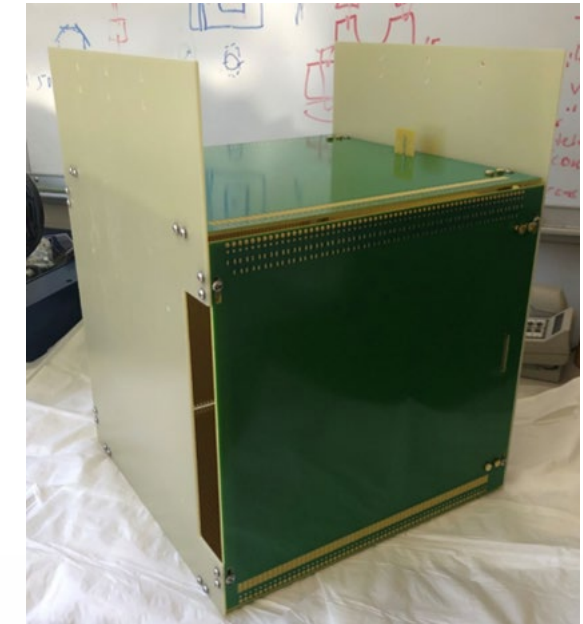# LArPix: Pixelated LArTPC Readout for DUNE Near Detector

Prototype tiles have 100 LArPix ASICs
(30 cm by 30 cm)
ND Tiles will scale to 160 ASICs/tile
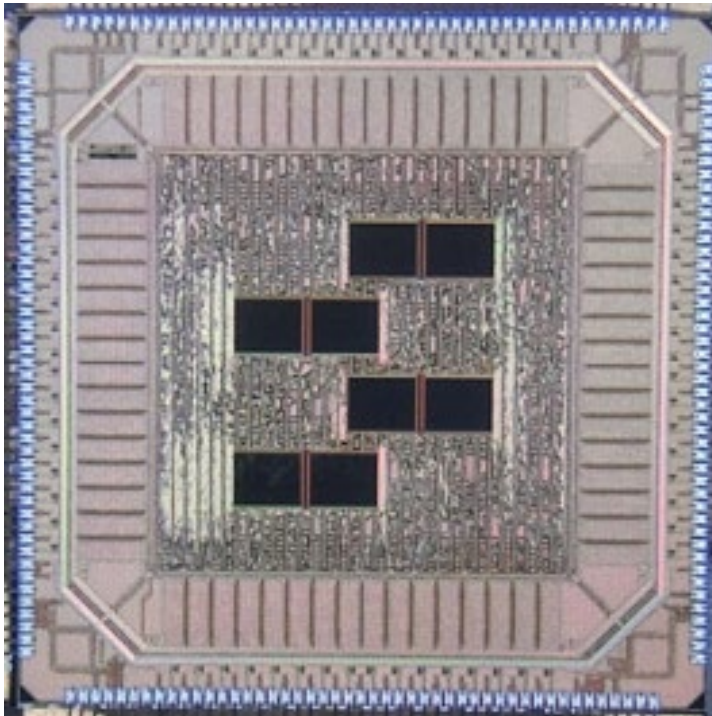
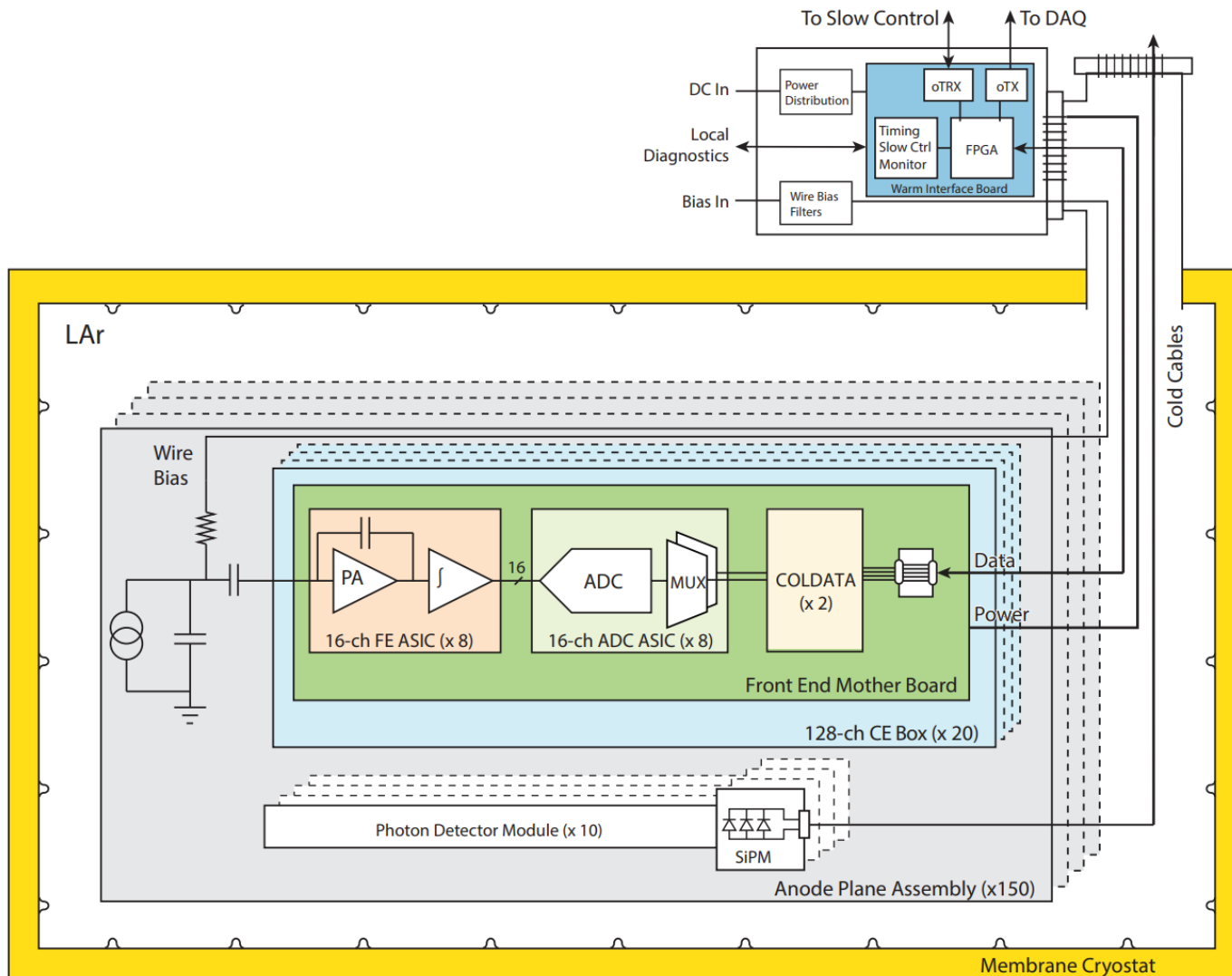64 Channel LArPix ASIC (25 mm^2)
180 nm CMOS

10x10 Pixel Tile

8 events

The DUNE Far Detector Electronics
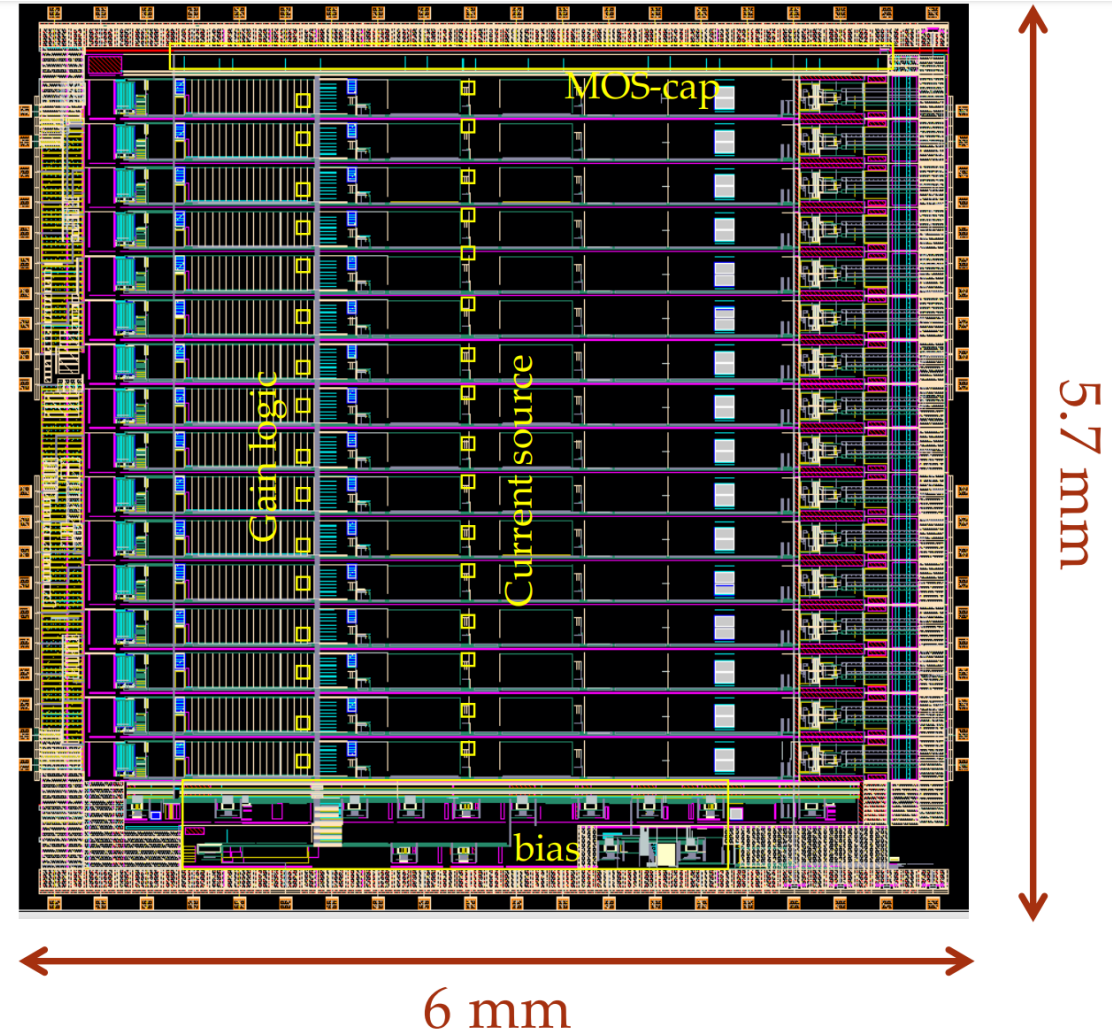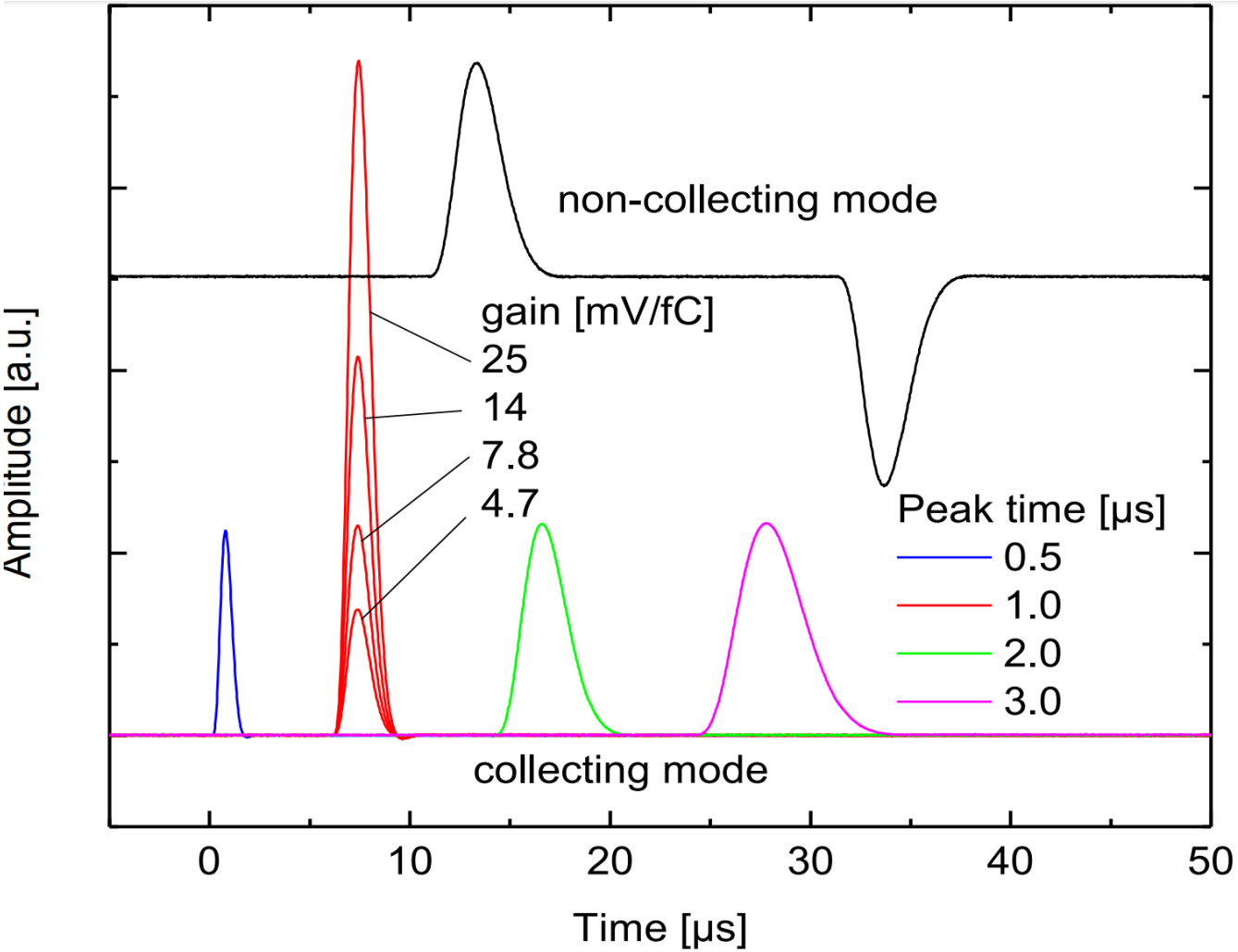

JINST 15/T08010

Charge collection system uses 3-chip solution

- LArASIC – 16 channel preamp

- Cold ADC – 16 channel ADC

- COLDATA – data aggregator and high-speed digital communications
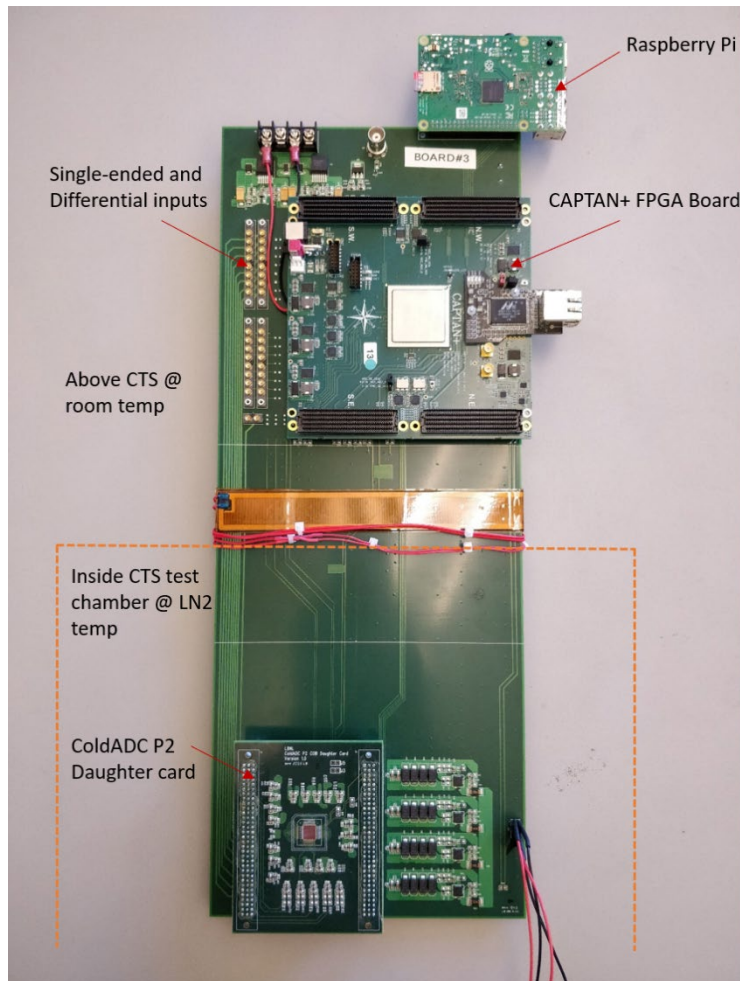
All chips are immersed in LAr and have a 30-year required lifetime

24000 LArASIC, 24000 ColdADC, and 6000 COLDATA ASICs are required to instrument a Far Detector Single-Phase Module
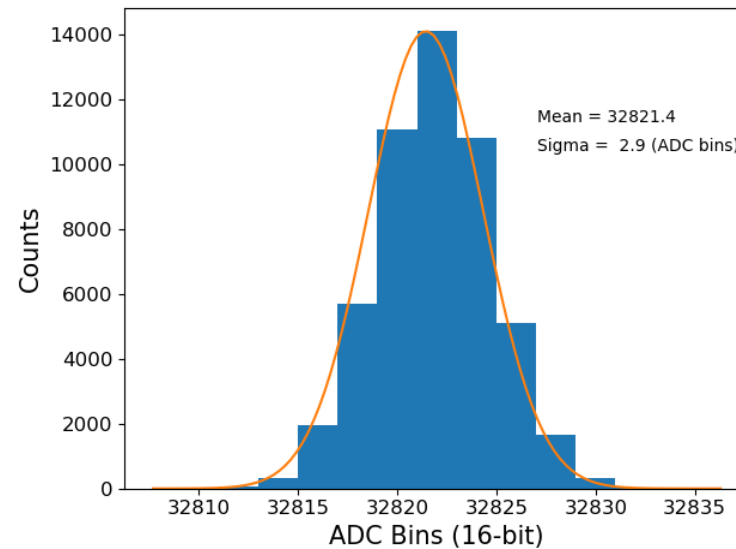
DUNE Far Detector (LArASIC)
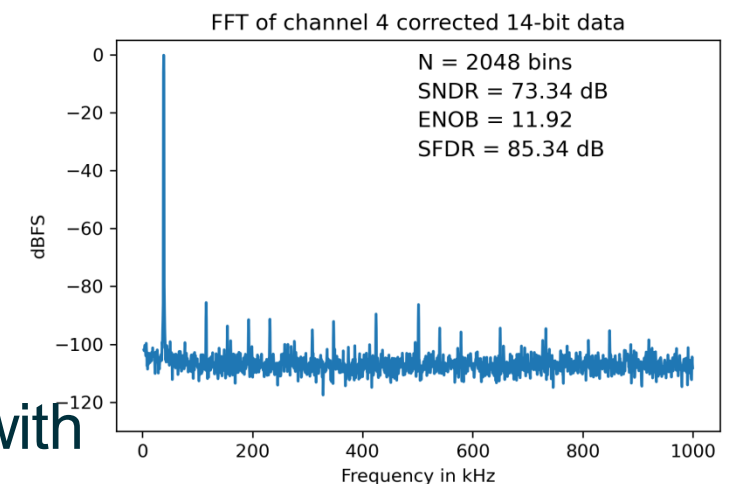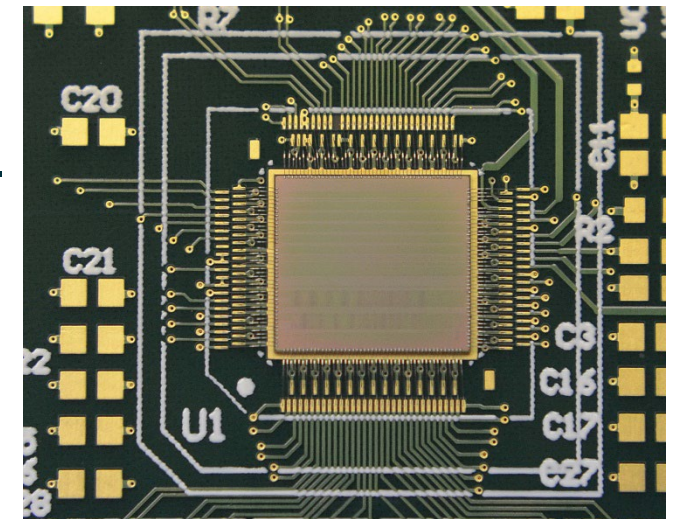
ColdADC: Low-Noise Digitizer for DUNE Far Detector

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

65 nm CMOS

Raspberry Pi

Single-ended and Differential inputs

BOARD#3

CAPTAN+ FPGA Board

Above CTS @ room temp

Inside CTS test chamber @ LN2 temp

ColdADC P2 Daughter card

16-Channel 2 MS/s digitizer with 12b ENOB at LAr temperature (-200 °C). Joint project with FNAL and BNL.

Mean = 32821.4
Sigma = 2.9 (ADC bins)

Measured noise = 130 µV-rms

Designed for 30-year reliability with custom cold simulation models

FFT of channel 4 corrected 14-bit data

N = 2048 bins
SNDR = 73.34 dB
ENOB = 11.92
SFDR = 85.34 dB

CRYO ASIC

System-on-chip (SoC) charge readout for noble liquid TPC experiments

- **Architecture with combined analog & digital functions**
  - Signal pre-amplification with channel multiplexing, A/D conversion, encoding, and serialization
- **Optimized for cryogenic operation (i.e., LAr - 87 K, LXe - 160 K)**
  - Chip designed using custom models developed at SLAC
  - Characterization of 130 nm CMOS at cryo temperatures
- **On-chip supply regulation**
  - No external active components (low background)
- **Small chip size (7 mm x 9 mm) with a minimal number of I/Os**
- **Power scaling mode to reduce overall power consumption**
- **Designed for reliability and testability**
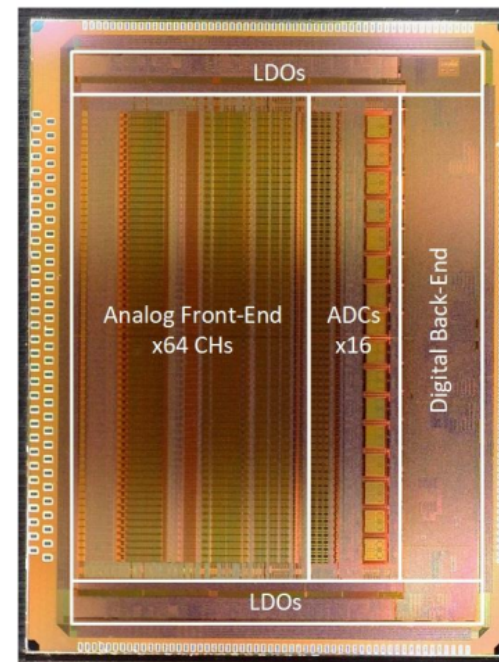
Chip Size: 7mm x 9mm
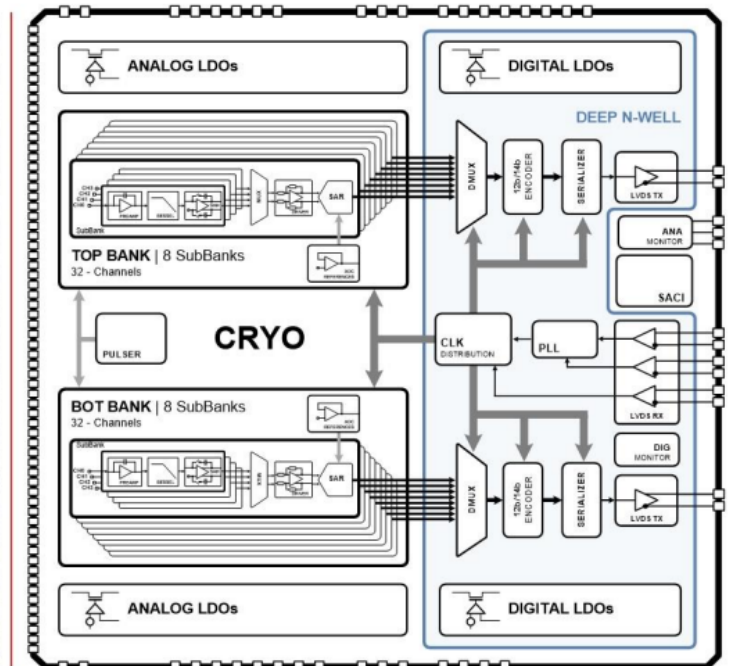
Qpix ASIC

- **"least action" principle of electronics readout**

- Charge from a pixel (In) integrates on a charge sensitive amplifier (A) until a threshold ($V_{th} \sim \Delta Q/C_f$) is met which fires the Schmitt Trigger which causes a reset (M_f) and the loop repeats
- Measure the time of the "reset" using a local clock (within the ASIC)
  - Basic datum is 64 bits
    - 32 bit time + pixel address + ASIC ID + Configuration + …
- Take the **difference** between **sequential** resets (Reset Time Difference = RTD)
  - Total charge for any **RTD = ΔQ**
- RTD's measure the **instantaneous current** and captures the waveform
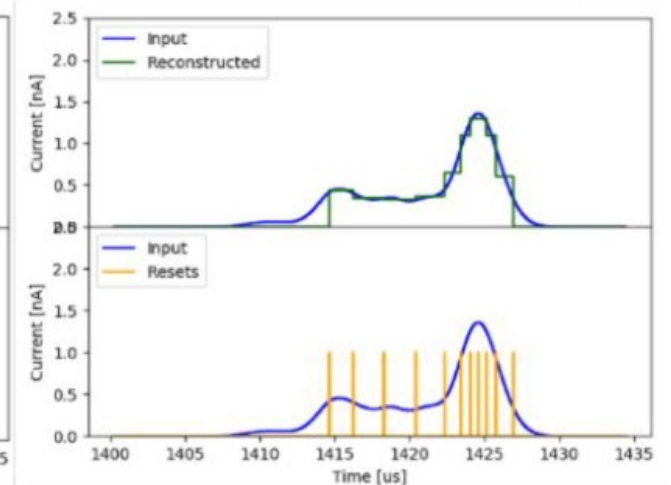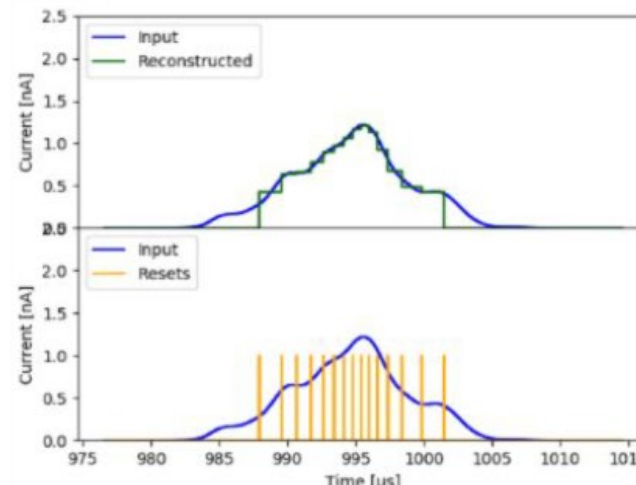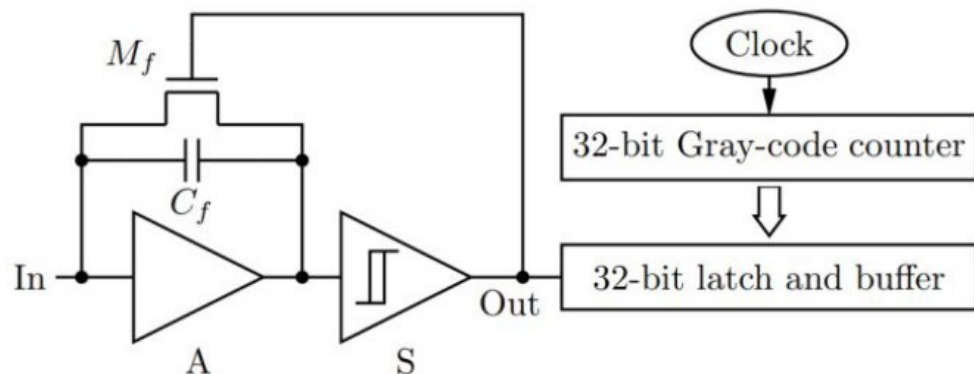
Quantum cryoelectronics projects

## Deep cryogenic electronics on advanced technology nodes (GF 22 FDX)

- Cryogenic modelling for development of 4K process design kit for GF 22 FDX with EPFL, Synopsys & GF

- **Quantum Science center** (National Quantum Initiative center led by ORNL)

  Ion trap based Quantum Simulator: Cryoelectronics Controller – Low noise, high speed, high voltage DACs

- Compact Optical Atomic Clocks: Room temperature, integrated control **Joint DOE-DOD project** with MIT LL

- High speed cryogenic ADCs at 4K with **Industry**

- Cryo-picosecond TDC for SNSPD readout with JPL and Caltech (Quantum Communication).

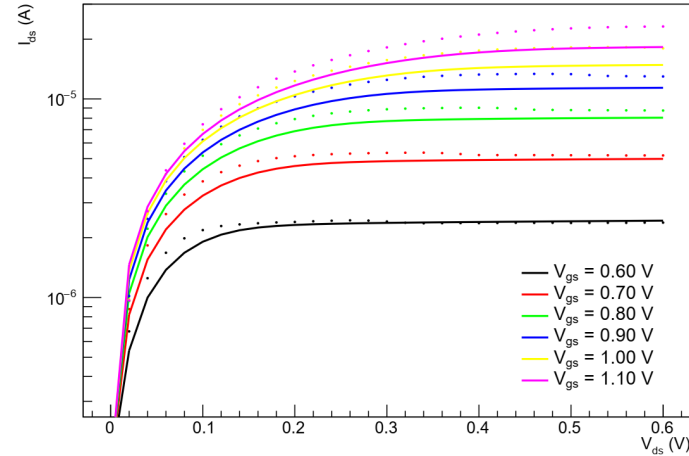Superconducting electronics: TWPAs and JPAs for ADMX-BREAD using a super conducting fab

🔷 **Fermilab**

15
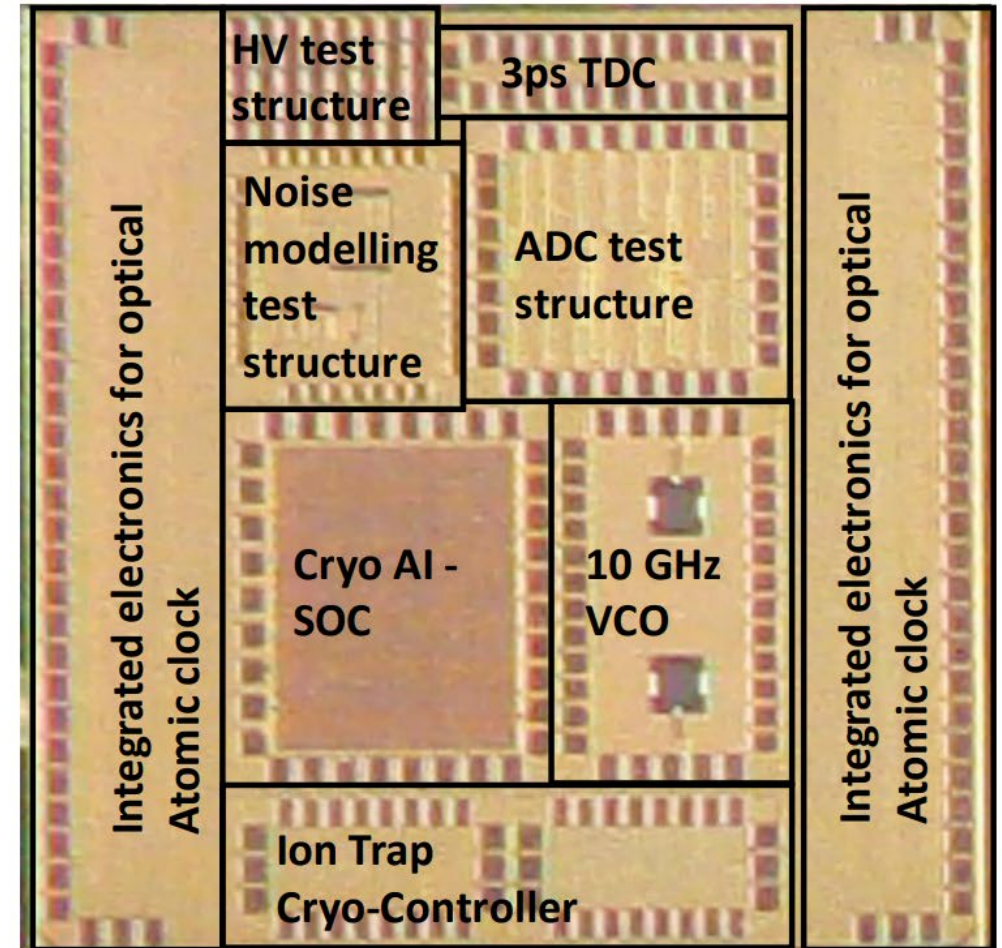
CryoCMOS

Focus is on quantum sensor readout
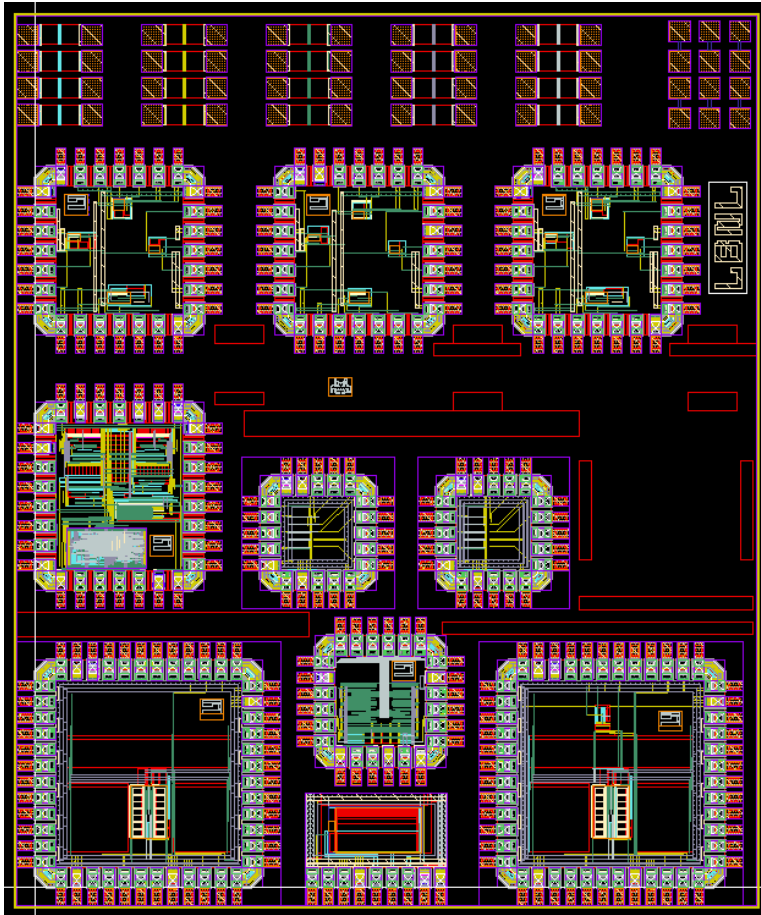
0.5µm/1.2µm NMOS at 100 mK

0.5µm/0.5µm NMOS at 100 mK
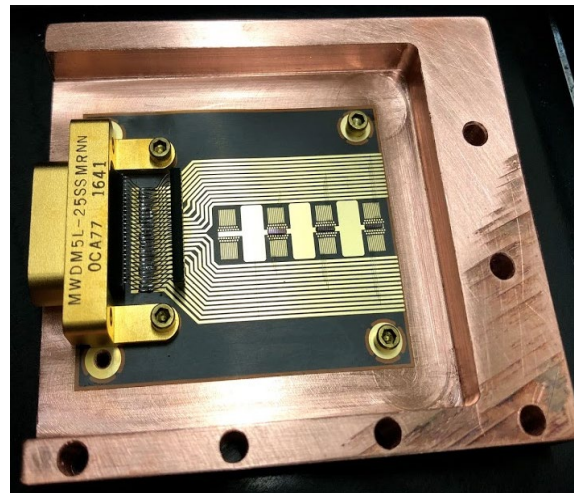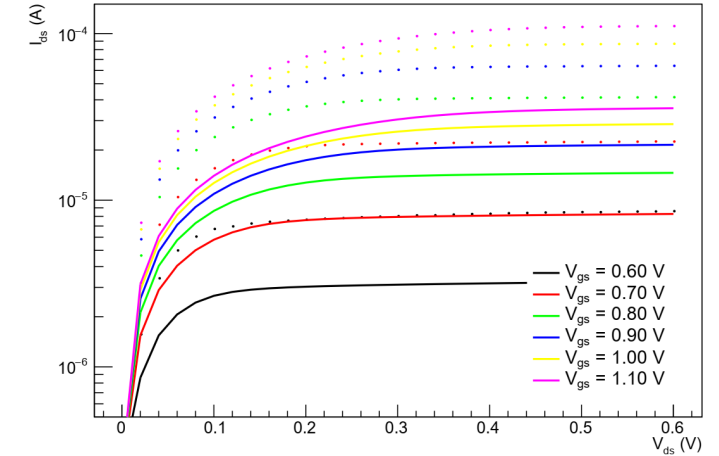
Test setup compatible with temperatures down to approximately 10 mK

Increasingly important to do system modeling/optimization

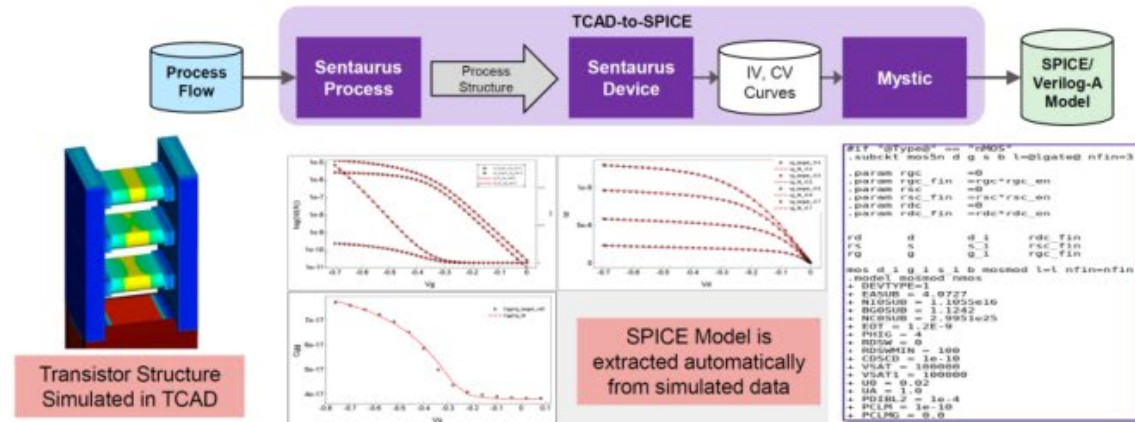## SC and cryo-CMOS modeling and extraction

In collaboration with Synopsys
- SC electronics models (MIT, FNAL)
- cryoCMOS models (FNAL, EPFL)
- Prototyped a test structure for 1/f noise measurement

Now simulating CMOS + xTron + SNSPD

TCAD-To-SPICE Sub-Flow Extracts SPICE Model From TCAD Before Wafers Are Available

Mystic extracts SPICE or Verilog-A compact model from Sentaurus Device Output

TCAD-to-SPICE

Process Flow → Sentaurus Process → Process Structure → Sentaurus Device → IV, CV Curves → Mystic → SPICE/Verilog-A Model

Transistor Structure Simulated in TCAD

SPICE Model is extracted automatically from simulated data

Apologies if didn't cover

申し訳ございません

Cryogenic Readout – (not really a) Summary

- **Increasingly important in a quantum world**

- **CMOS behavior changes significantly from the extrapolated values provided in typical PDKs**

- **Need to characterize each new technology node**

- **Good news is that once appropriate scaling taken into account, we know how to do the rest**
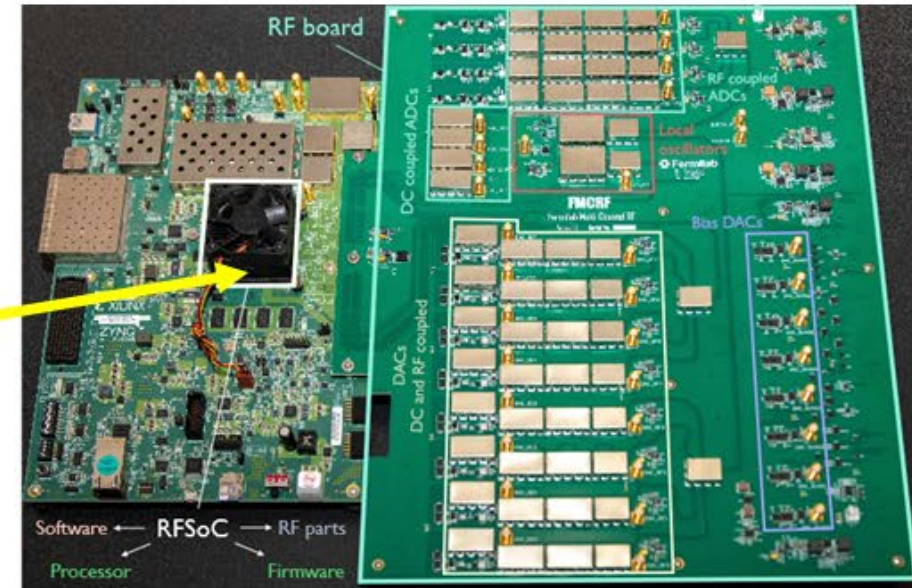
- **Great opportunities to advance the science (next slide)**

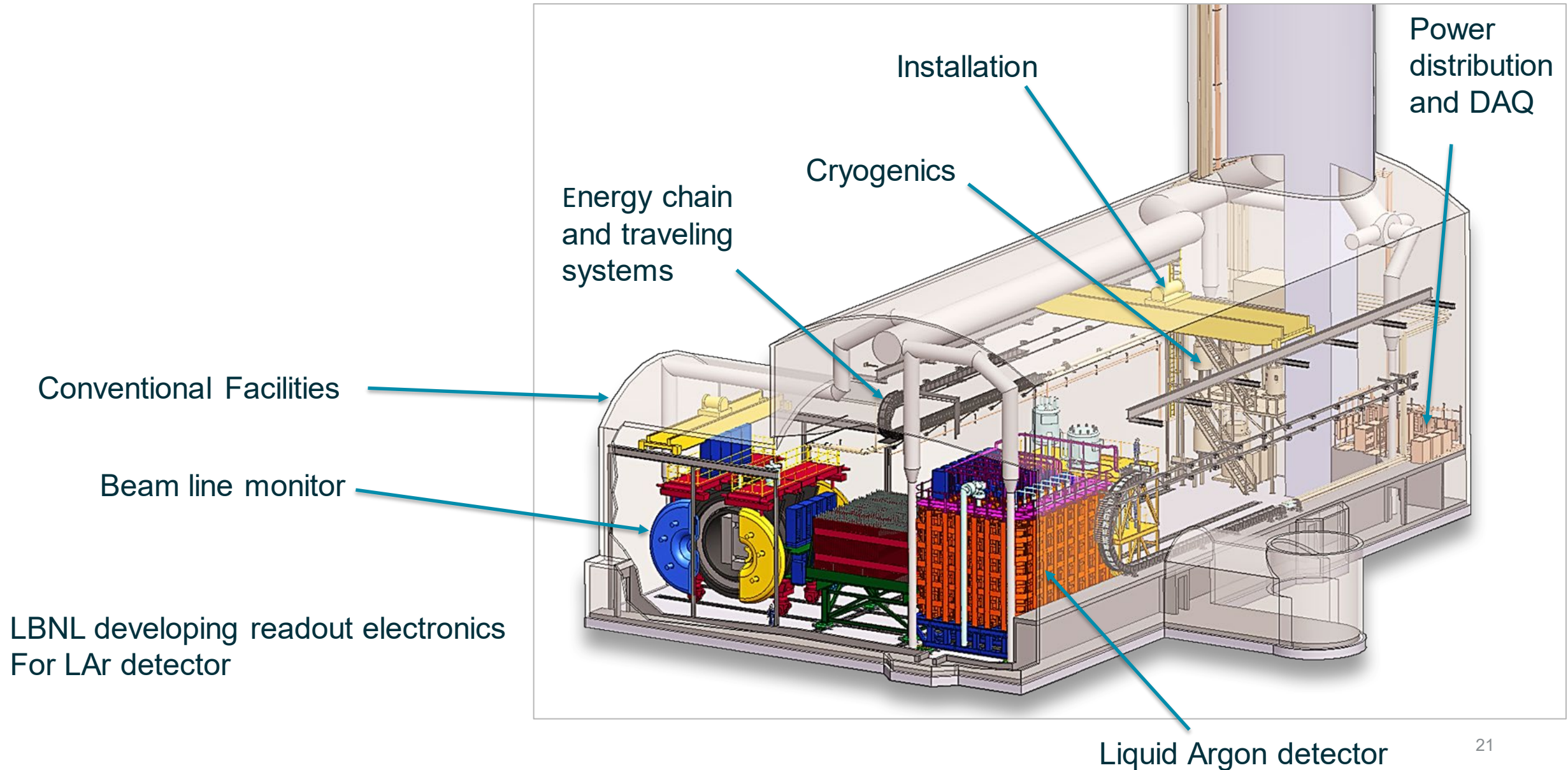# Backup Slides

Replaces ~$1M, full rack, off-the-shelf → with $20K, single pair of boards

RFSoc
FPGA

DUNE Near Detector

Installation

Power distribution and DAQ

Cryogenics

Energy chain and traveling systems

Conventional Facilities

Beam line monitor

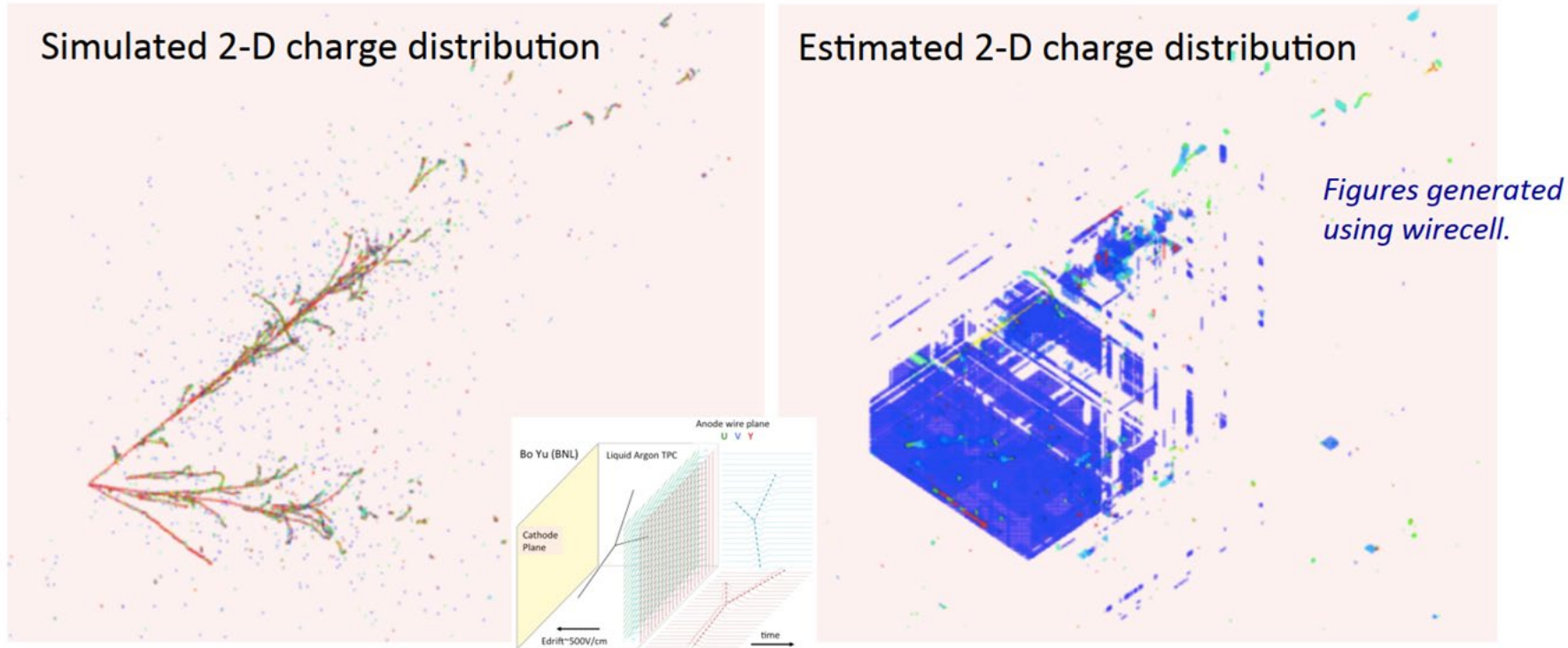LBNL developing readout electronics
For LAr detector

Liquid Argon detector

Key Near Detector technical challenge

The much larger Far Detector (FD) uses a conventional wire-based liquid Argon (LAr) Time Projection Chamber. Electrons generated by neutrino collisions are drifted in an electric field to wire planes in the cold volume.

Simulated 2-D charge distribution

Estimated 2-D charge distribution

Figures generated using wirecell.

3 GeV electron neutrino charge-current interaction in LAr.

When tracks/showers are parallel to anode plane, all signals are simultaneous. This leads to ambiguity which could be a showstopper with the high event rate in the DUNE ND.
Solution: True 3D readout with a pixelated detector immersed in LAr for the DUNE Near Detector.
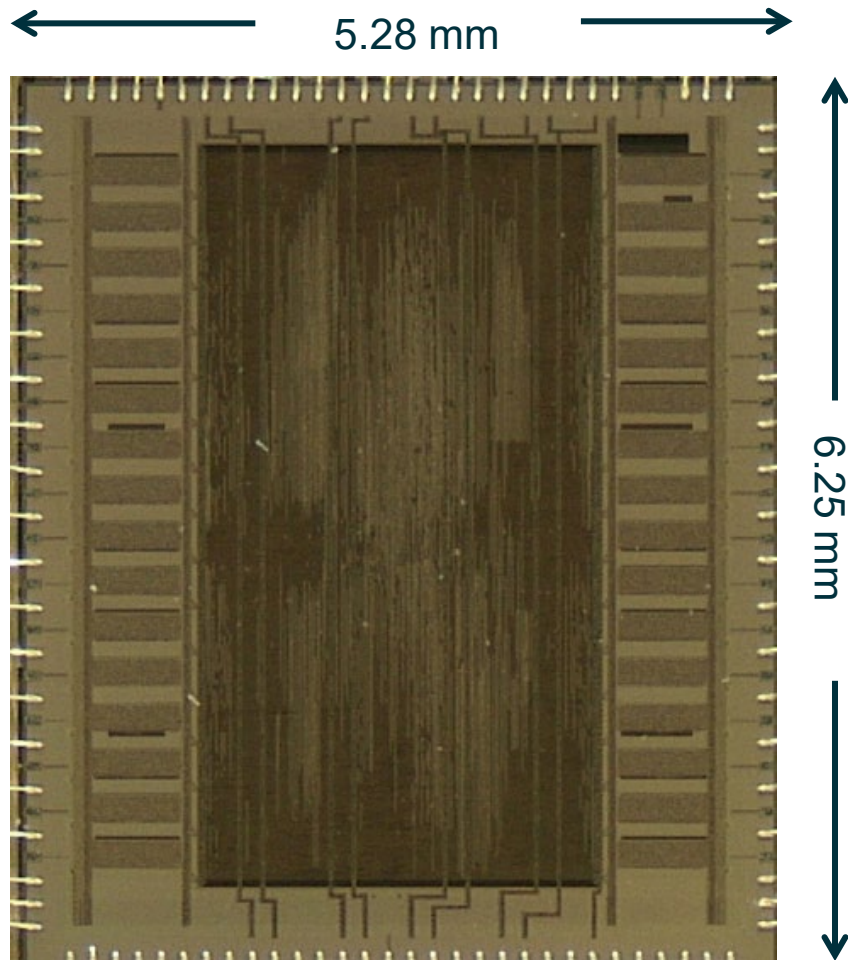
LArPix Pixel Tile
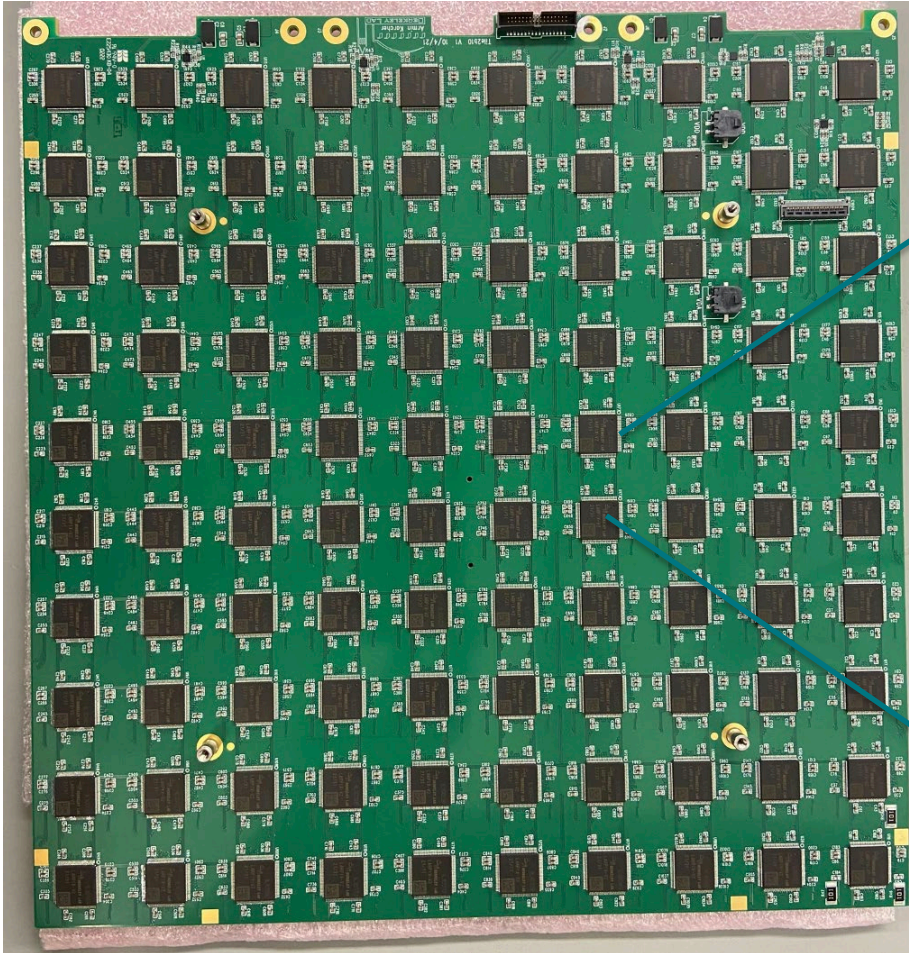
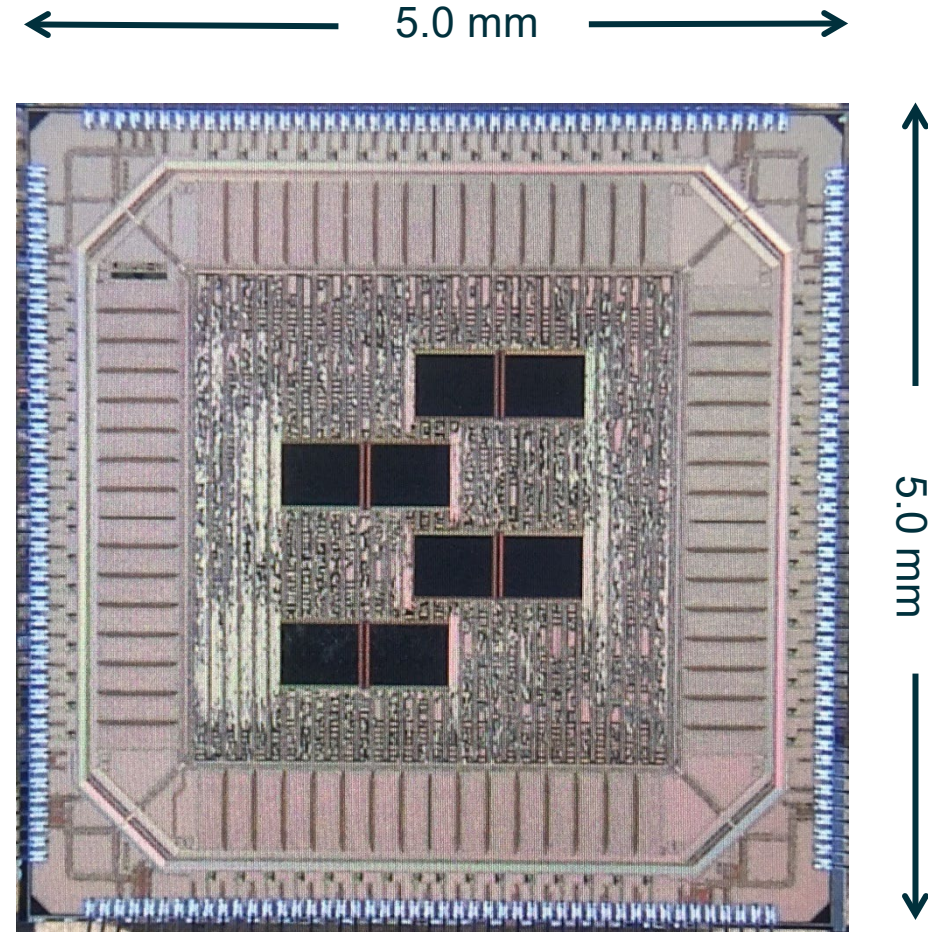Tile with 100 LArPix-v2 ASICs (6400 channels)

Closeup of tile
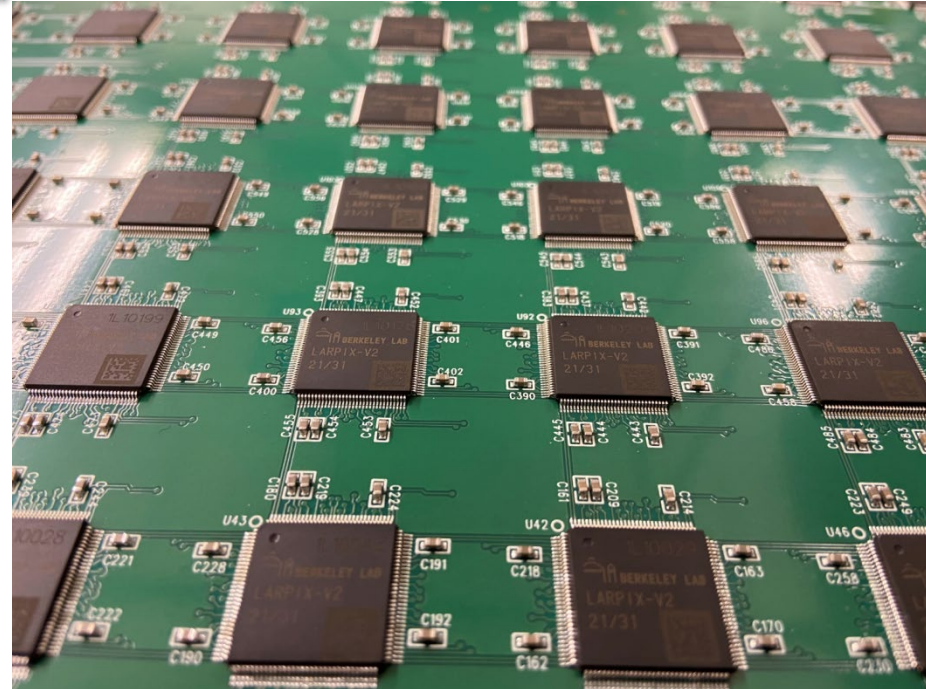
Prototype tiles have 100 LArPix ASICs
(30 cm by 30 cm)
ND Tiles will scale to 160 ASICs/tile

Quick Design Iteration → Continuous Improvement

5.28 mm

6.25 mm
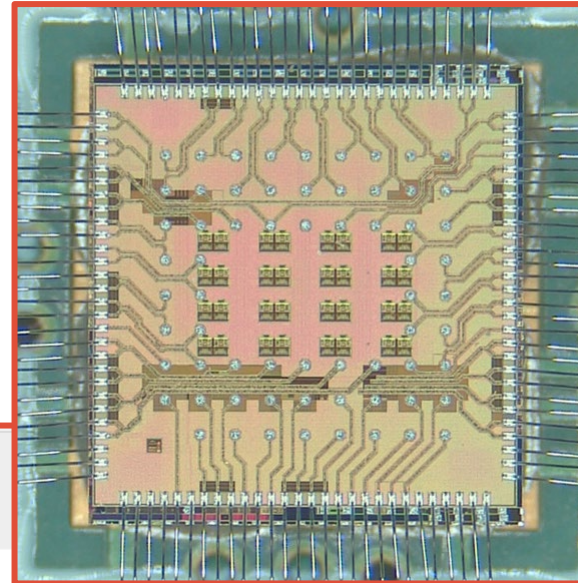
LArPix-v1

32 channels, 33 mm^2

5.0 mm

5.0 mm

LArPix-v2

64 channels, 25 mm^2

PETAL2: Line driver IC for Cryo-EM

Line driver and frame marker for **next-generation real-time, single-electron counting direct detection cameras.**

- Interface with **K3** sensor - a 24 Mpixel CMOS thinned sensor for Cryo-EM

- **35% area reduction,** and

- **40% power reduction** for existing camera assembly

- Goal is sub-1 Å resolution