3D integration prospects for high energy and nuclear physics

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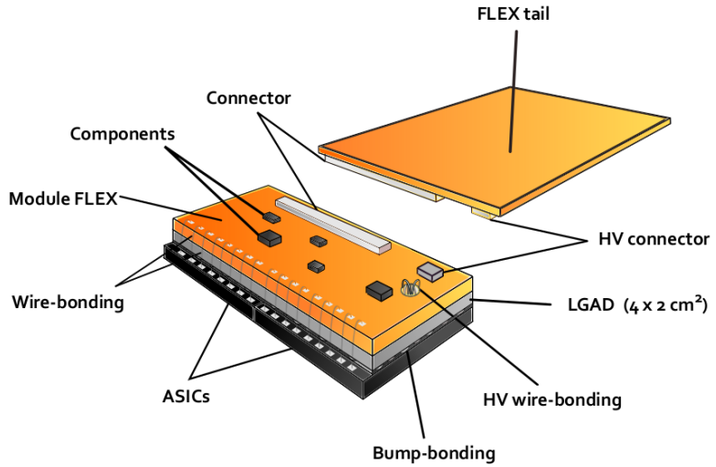
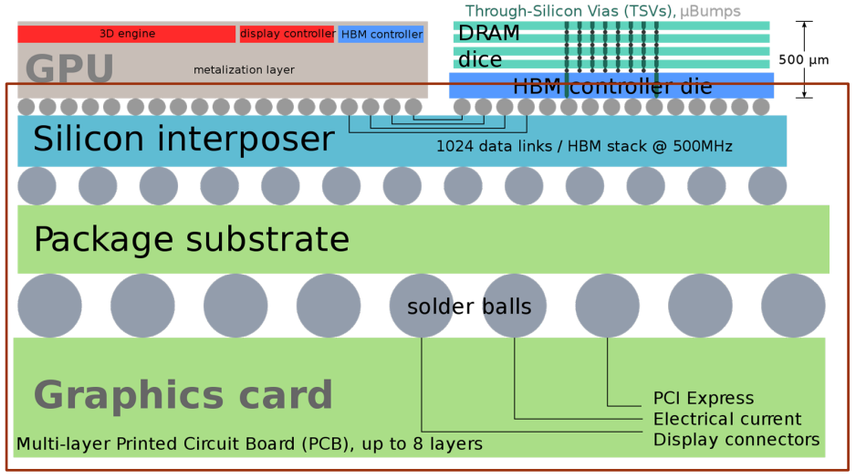
Instrumentation Frontier 03
Snowmass community summer study

Current packaging technology

- As of now sensor to chip integration in HEP have been mostly relying on **bump bonding**
  - (wire bonding as well but that's planar)
- Bump bonding technology is reliable but has its limitations
  - Only works down to 20-50 um of pitch and has issues of yield for fine connections
  - Solder balls increase the input capacitance to the amplifier and the noise
  - Connection is subject to heat stress since it involves different materials
  - Needs silicon interposer for planar connections or side extension of chip for external connections
  - Limits minimum thickness since both chip and sensor need thick enough support wafers
- **Advanced packaging may solve part of these issues**
  - Improving both performance, yield and processing



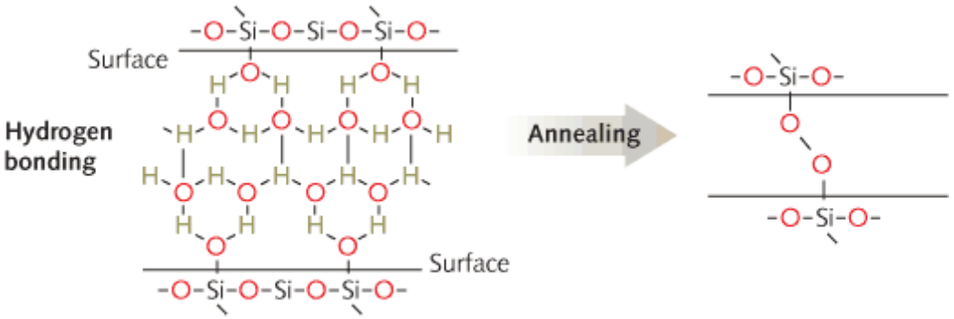
HGTD module (https://cds.cern.ch/record/2719855)

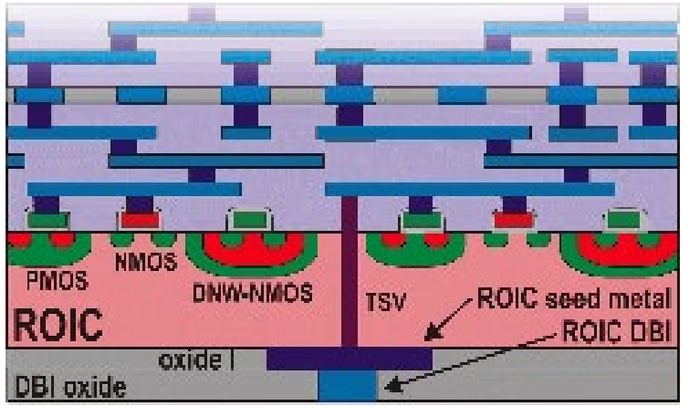


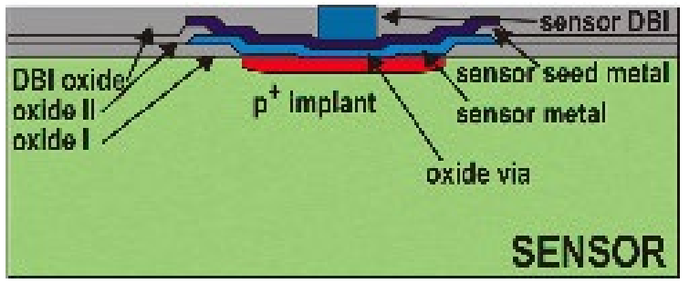
3D technologies

- **3D integration** technology in industry currently allows tight packaging of sensor and chip
  - Or stacks of multiple chips
- Many technologies available
  - **Direct Bonding Interconnect (DBI)** most widely accepted: silicon covalent oxide bonding, copper diffusion bonding
- Can be done for wafer to wafer (w2w) or die to wafer (d2w) assembly
- **Through Silicon Via (TSV)** connections allows to have **multiple planes stacked and connected**
  - With external connections not needing extensions or interposers

Si covalent oxide bonding

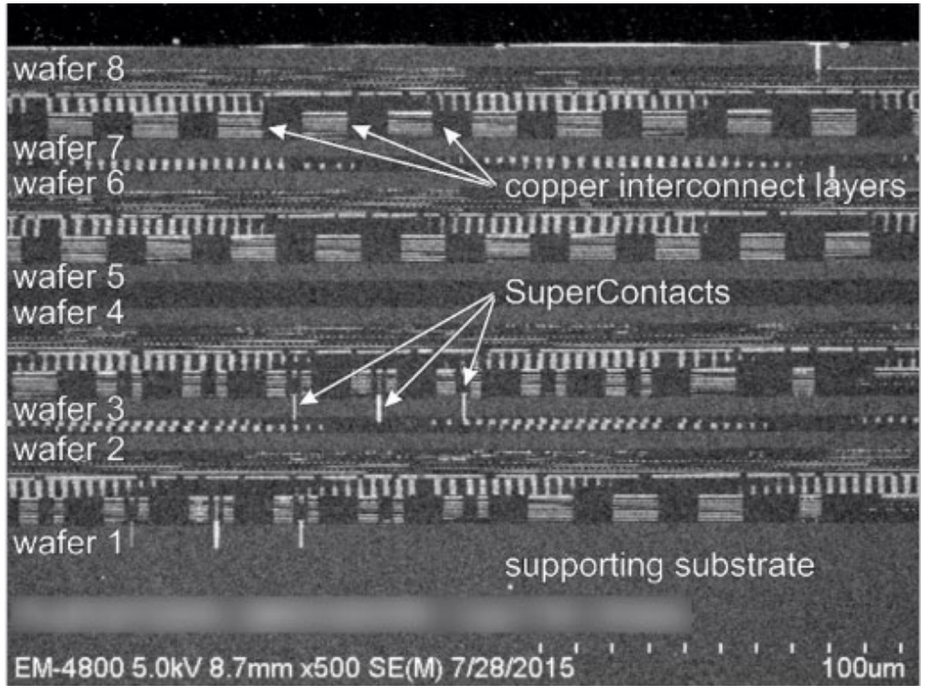






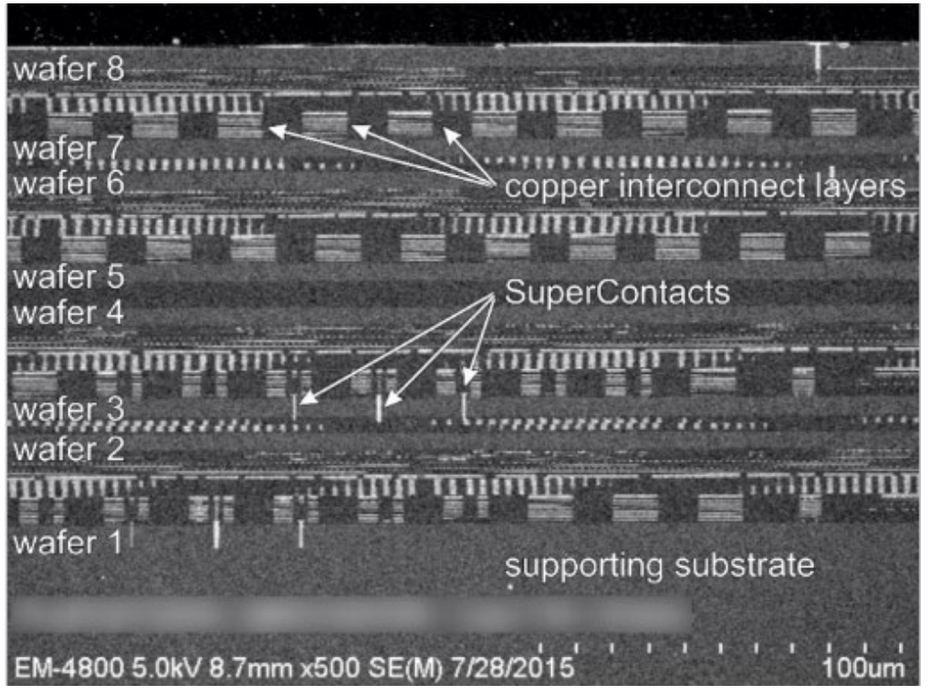
Advantages of 3D integration - 1

- **Less space**: 3D chips can be multilayer and do not need extension or interposers for external connections
- **Very fine pitch** bonding (down to ~3 μm)
- **Better connection**
  - Connections are shorter and faster than in circuit boards with long traces
  - Shorter connections also have reduced dissipated power
  - Eliminates the need for ESD protection on the wiring between chips
- **Better performance**:
  - Reduced input capacitance and lower noise
  - Lowers the parasitic of the interconnect wiring



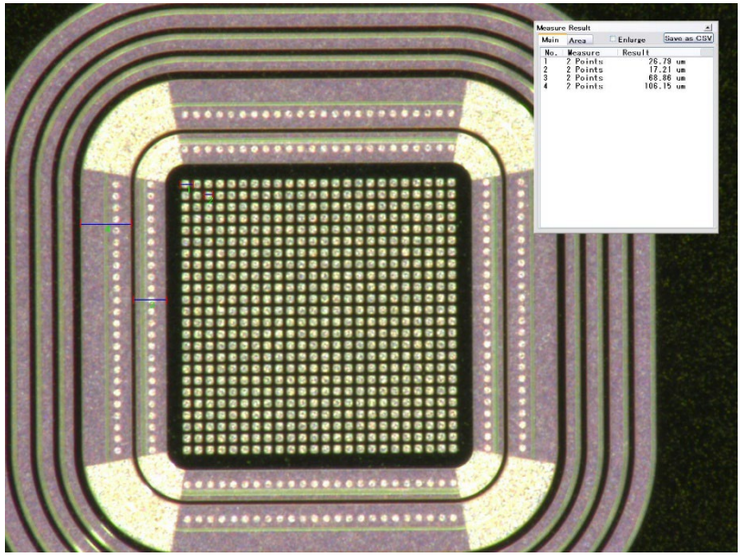
Advantages of 3D integration - 2

- **Layered design**:
  - E.g. sensor + analog electronics + (multiple?) digital electronics
  - Each layer can be manufactured by different producers and assembled
- **Separated optimization:**
  - Separate optimization of sensors and electronics
  - Ability to fabricate a MAPS-type detector with high drift fields and/or amplifying structures of arbitrary thickness in the sensor layer
- **Reduced thermal stress** and **increased heat dissipation** since material is homogeneous
  - Robustness increases as well
- **Integration of heterogeneous materials or different wafer technologies**
- **Reduction of single layer thickness**, after integration all supports can be removed

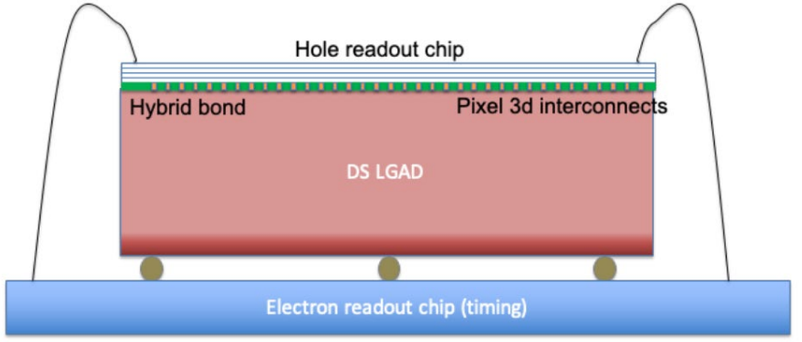


Possible applications in experimental physics - 1

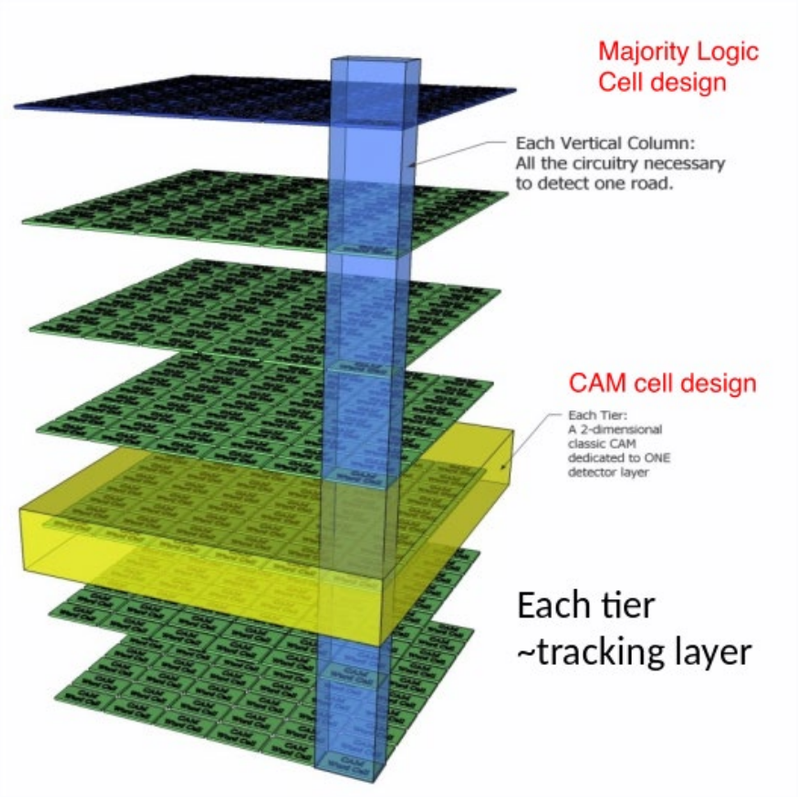
- Many applications for 3D integration can be foreseen in HEP, nuclear physics and photon physics
- **High granularity LGADs**
  - Standard LGADs are limited in terms of granularity, however new technologies can provide segmented LGADs down to less than 50 μm scale maintaining the exceptional time resolution
  - The ultimate goal is to provide readout to LGADs with the ability to reach 10 μm of position resolution and with 10ps of time resolution
- **Double sided and small pixel LGADs** (DOI 10.2172/1841398)
  - Double sided LGAD with gain layer on the electron-collecting side and an array of small (3D-integrated) electrodes on the hole-collecting (anode) side.
  - Cathode will provide timing and Anode will provide depth an position with high precision. This reduces the power needed for timing measurements.
  - Anode also provides total collected charge for position resolution or the current pulse shape to measure the depth of the charge deposition at the pixel position.
- **3D integrated SiPM** (DOI 10.1109/NSSMIC.2018.8824571)
  - A 3DIC version of the SiPM can incorporate much more sophisticated processing including active quenching for each pixel, digital timing and windowing, inter micro pixel communication and digital pattern recognition and readout.



FBK high granularity AC-LGAD



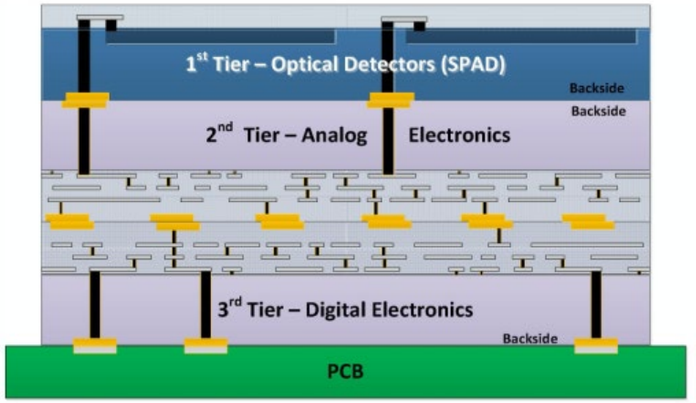
Possible applications in experimental physics - 2



- **Stacked 3D integrated chip**, (DOI https://doi.org/10.1016/j.phpro.2012.02.521)
  - Creating a 3D network of algorithm cells for advanced pattern recognition, adding a "third" dimension opens up the possibility for new architectures that could significantly enhance pattern recognition capability
  - The 3DIC based architectures allow massive three-dimensional networks for data communication with much shorter traces and very low parasitic capacitance, with flexible algorithm cells distributed throughout the network
  - Track finding or particle flow over multiple detector layers using both position information and time of arrival information
- **Edgeless tile arrays**
  - Electronic integrated circuits are generally limited by the size of the photo mask reticule, typically 2 × 3 cm or less while sensors can be produced on up to 8" wafers
  - 3D integration allows to build fully active tiles that can populate complex shapes with near-optimal tiling and low dead area.
- **Small pixels** (10 um or less) that reduces the input capacitance of thin sensors (e.g. thin LGADs) increasing both space and time precision (DOI https://doi.org/10.1016/j.nima.2019.162423)
  - 3D integration allows for small pixels with minimal capacitance associated with the inter-connect and electronic processing in complex, multi-tier readout integrated circuits.
  - The induced current pulse is prompt, with very fast rise time, and, combined with low capacitance, has the potential to provide excellent time resolution

Possible applications in experimental physics - 3

- **2D Interconnects and Interposers**
  - Replacing conventional hybrid circuits with silicon-based "2.5D"substrates can improve the bandwidth, density and power efficiency of these systems.
  - A silicon-based substrate or interposer (with TSVs), combined with micro bump technology connecting the substrate to component "chiplets" can improve performance by an order of magnitude or more.

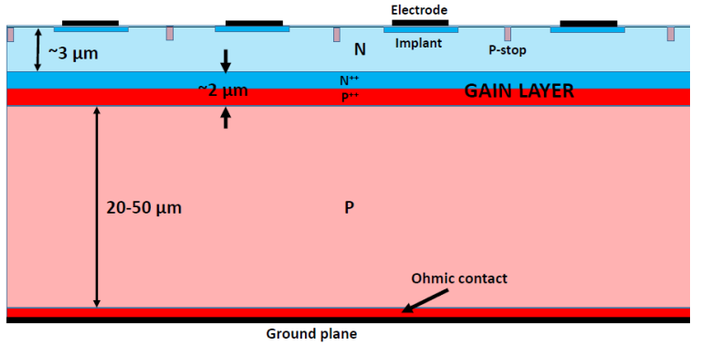


(J.F Pratte Sherbrooke)

- **Zero mass trackers with very thin and highly populated layers of 3D integrated sensor + chip for tracking close to interaction point**
  - A zero mass tracker would be extremely useful in many detectors where the preservation of the energy of the particles escaping from the interaction point is very important. The thin layers of detectors/readout, after thinning is foreseeable to have a 50 um sensor (or less) plus a 10 um of electronics per layer.

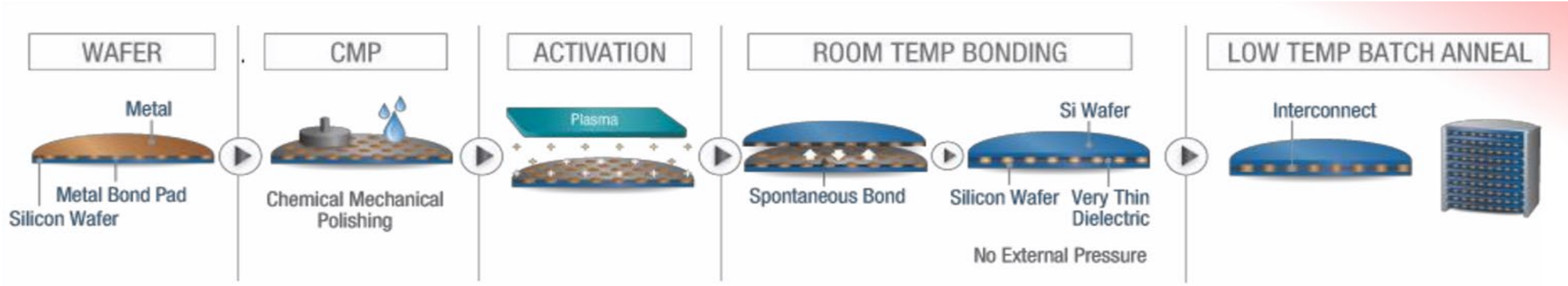
Possible applications in experimental physics - 4

- **Sensor stacks for high energy X-ray detection**
  - This technology would make possible to build stacks of 3D interconnected sensors/readout that can be used for X-ray detection applications with thin sensors.
  - For mid-high X-ray detection a fair amount of material is necessary to achieve a reasonable detection efficiency. 3D integrated layers of thin LGAD and readout would allow high repetition rate and large active thickness
- **Dense active targets**
  - The stacks of 3D interconnected sensors/readout could also be applied to the construction of high granularity active targets for particle decay reconstruction.
  - The fast charge collection time allows for great pulse pair resolution, paired with high granularity and low inactive area it would allow to fully reconstruct particle decay chains.
- **Development of substrate engineering**
  - Production of devices with buried doping profiles such as DJ-LGAD and buried LGAD



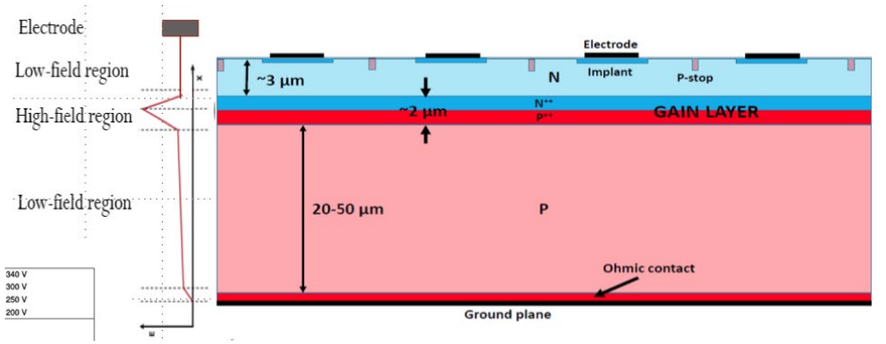
Industry partners

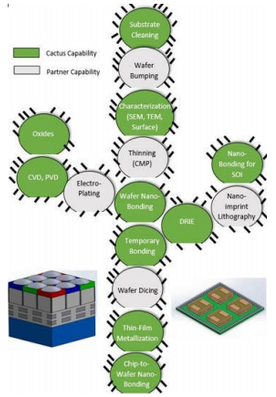
- NHanced (R. Patti) have been in the 3D integration business for over a decade
- Hybrid bonding, Oxide bonding, Si Interposers
- Lower temperature (down to 150 C) bonding
- Bonding yield around 70-80 % with very fine pitch

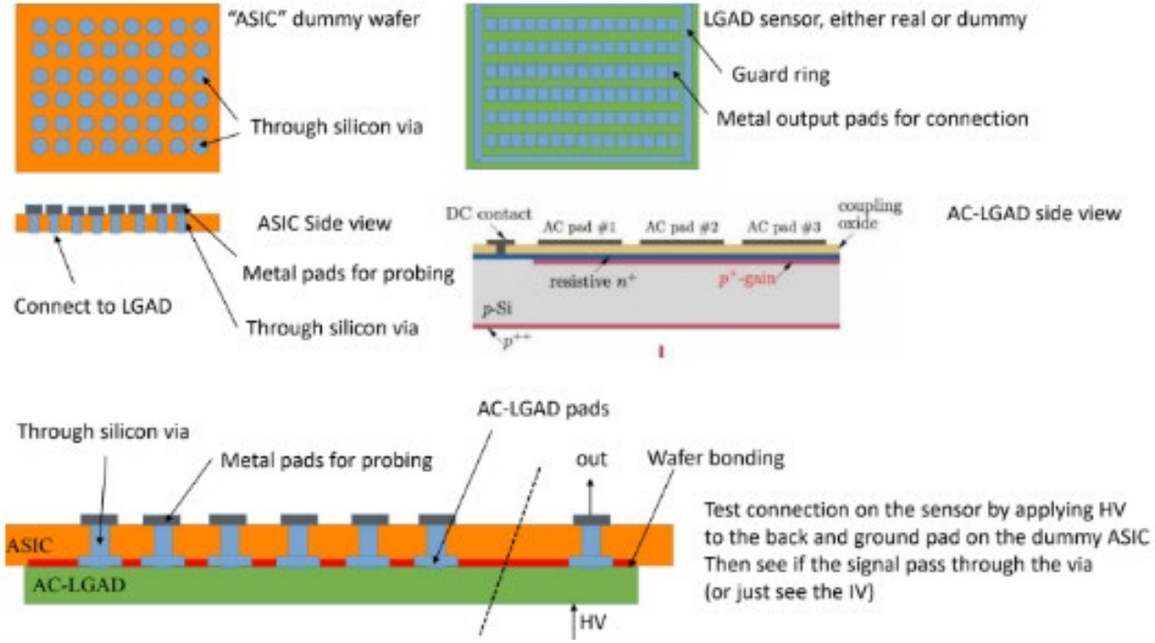


Industry partners

- CACTUS material capabilities (R. Islam)
- Low temperature wafer to wafer and chip to wafer bonding capabilities
- Currently working with UCSC to demonstrate successful 3D integration of high density LGADs to readout using TSVs
- Wafer2wafer bonding for deep substrate engineering (DJ-LGAD, Buried LGAD)
  - https://arxiv.org/abs/2101.00511
- Effort funded by awarded SBIRs

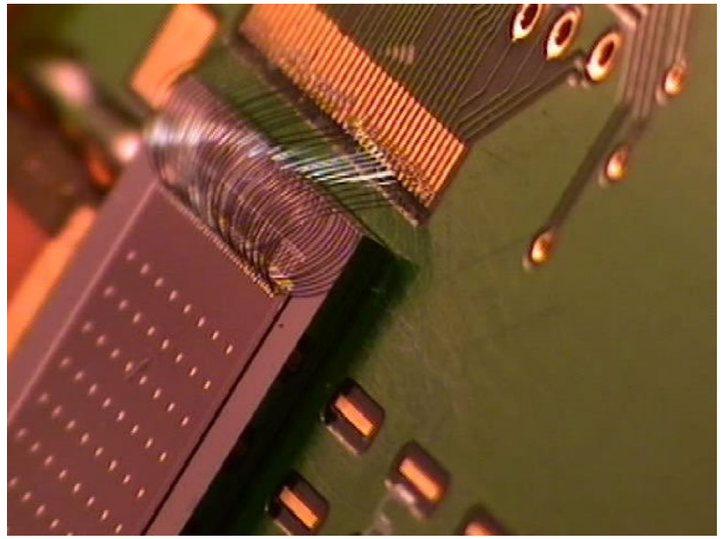






Current status

- 3D integration still lacks a large scale research application
  - But recent efforts produced or will produce working prototypes of 3D integrated modules
- Fermilab has had a long history of R&D into 3D integrated circuits
  - Pursued with many vendors during the years
  - E.g. "3D integration of sensors and electronics" (DOI https://doi.org/10.22323/1.309.0025)
  - Comparison of performance of 3D integrated sensor vs bump bonded
  - This project produced two-tier chips that were 3D(DBI) chip-to-wafer bonded to silicon sensors. Yielding a three-layer stack with readout layers35 microns thick.
  - This allowed a direct comparison of identical ROICs and detectors that were assembled with bump and DBI bonds.
  - The DBI bonded assemblies had roughly half (37.7 vs 70) the noise of the bump bonded set due to the lower interconnect capacitance.
- UCSC (new in the game) working with cactus material to test 3D integration and substrate engineering of LGADs



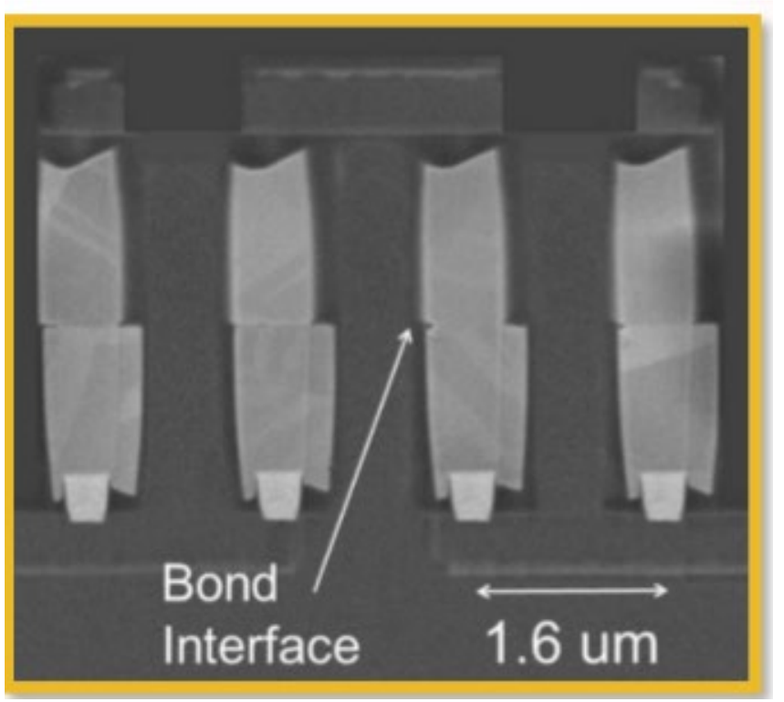
Path for future development

- The collaboration between national laboratories, universities and industry with established expertise in advanced packaging is crucial for the successful introduction of 3D integration in the high-energy physics research community
  - This comes naturally since this technology is much more advanced in industry than it is in research
  - (some future outlooks in https://semiengineering.com/next-gen-3d-chip-packaging-race-begins/)
  - Such partnership can provide cost-effective implementations of this technology to use in a research setting
- **Advanced packaging will enable the pursuit of 4D tracking to a level of precision beyond what is currently achievable**
  - Future high-energy physics, nuclear physics and photon physics efforts have to consider advanced packaging and industry partnerships as a possibility to reach their set goals
  - This will allow to advance the introduction of this technology in the global research community
- A few US based group are pursuing this goal in collaboration with small volume companies

Conclusions – 3D integration

- Time has come for detector packaging to ramp up for the next generation of experiments.
  - New challenges on many fronts: need for finer pitch, lower noise, higher density…
  - Many applications in several research field can benefit from advanced packaging
- There are many promising technologies for 3D integration becoming available that have the potential to revolutionize the next generations of experiments
- **Current "blue sky" development will pay off in the long run**

- We need to **think about what technologies will be available 10 years** from now and start developing the tools to use them



Thanks for the attention