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Technology developments for fast timing (Si trackers)

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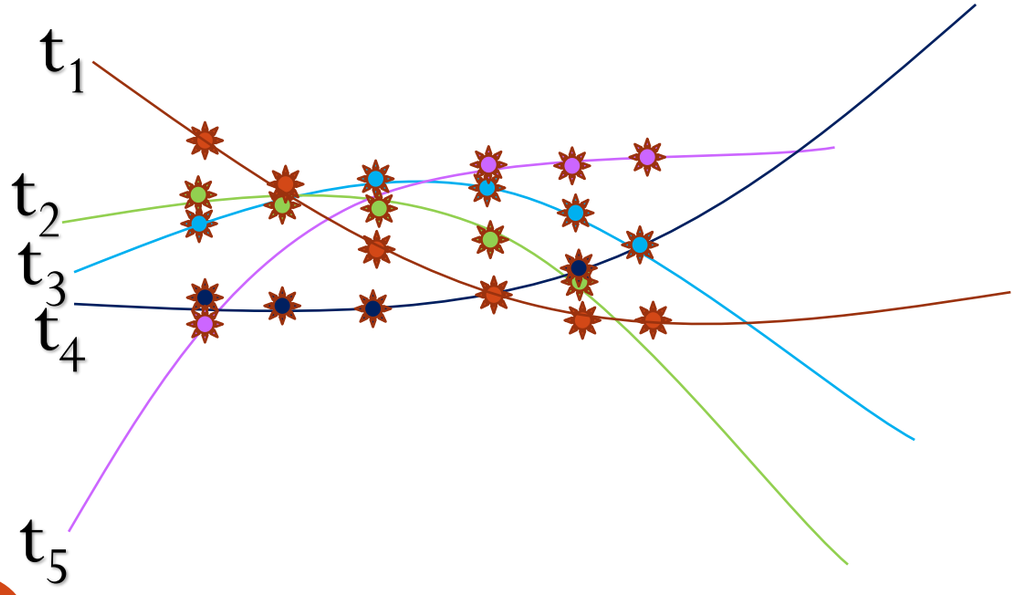
Cross Frontier session
Snowmass community summer study

Fast timing in tracking

- **Why fast timing? → 4D tracking**
  - Efficient tracking in dense environment
  - Pile-up suppression
  - Long Lived Particle detection
  - Appearing/Disappearing tracklets identification
  - ToF-based particle identification
  - Jet flavor tagging enhancement

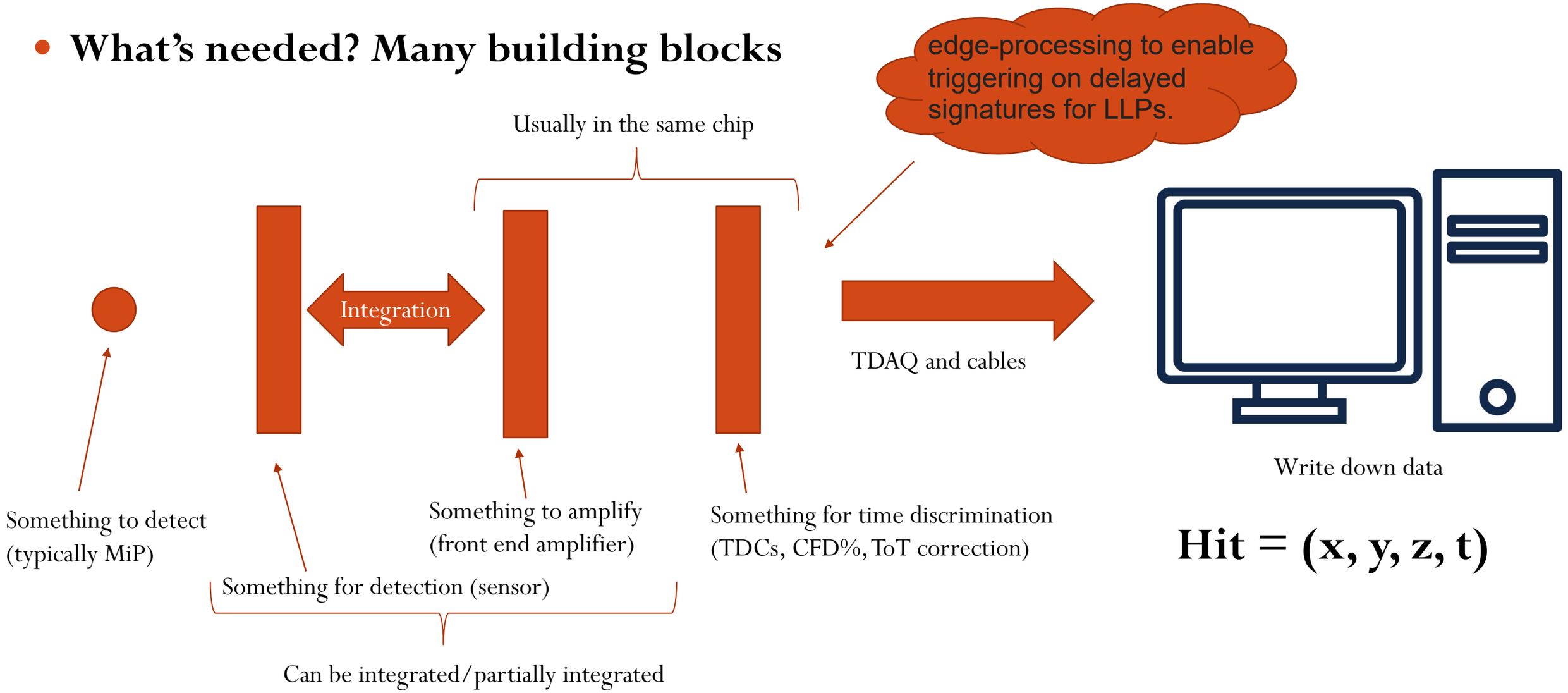


- **What is needed for future colliders?**
  - Depends on the application and environment
- High time and spatial precision
  - Time resolution **5-50 ps** per hit
  - Spatial resolution **5-25 um** per hit
- Very low material tracking
- For some applications radiation hardness is also important
- Coarse timing (ns) and high position precision (um)
- 5D tracking (incident angle measurement)

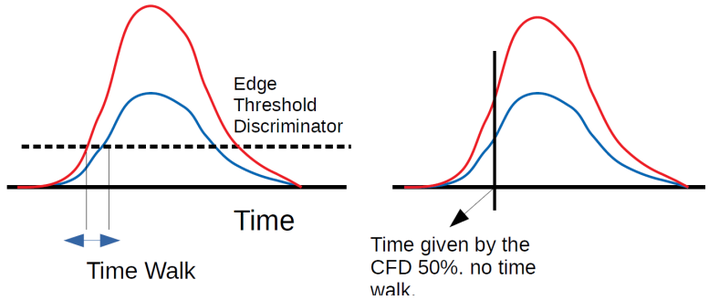
- Many more details in yesterday's session and many white papers
  - https://indico.fnal.gov/event/22303/sessions/20647/#20220719
  - 4D tracking paper, CMOS, Electronics, SiC, 3D integr.

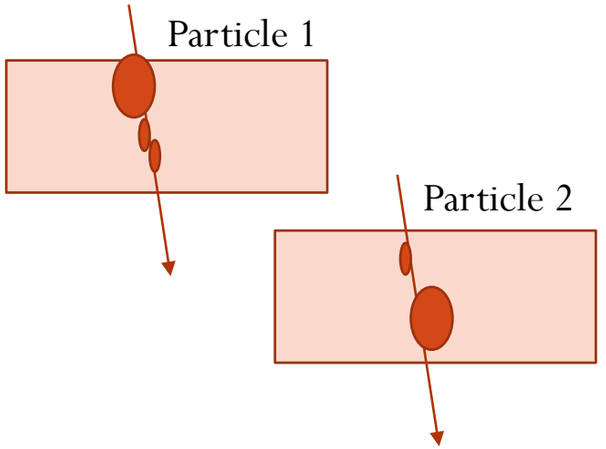
Fast timing in tracking

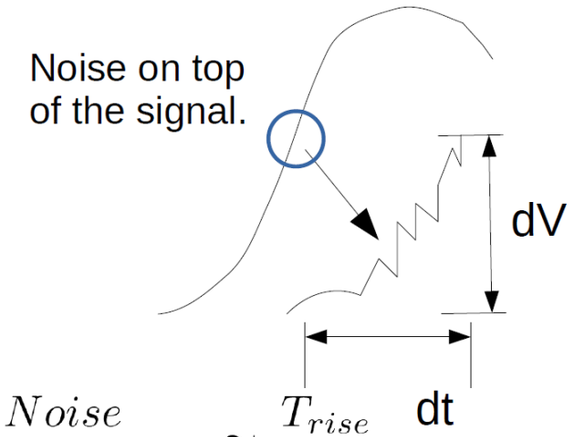
- **What's needed? Many building blocks**



Time resolution components







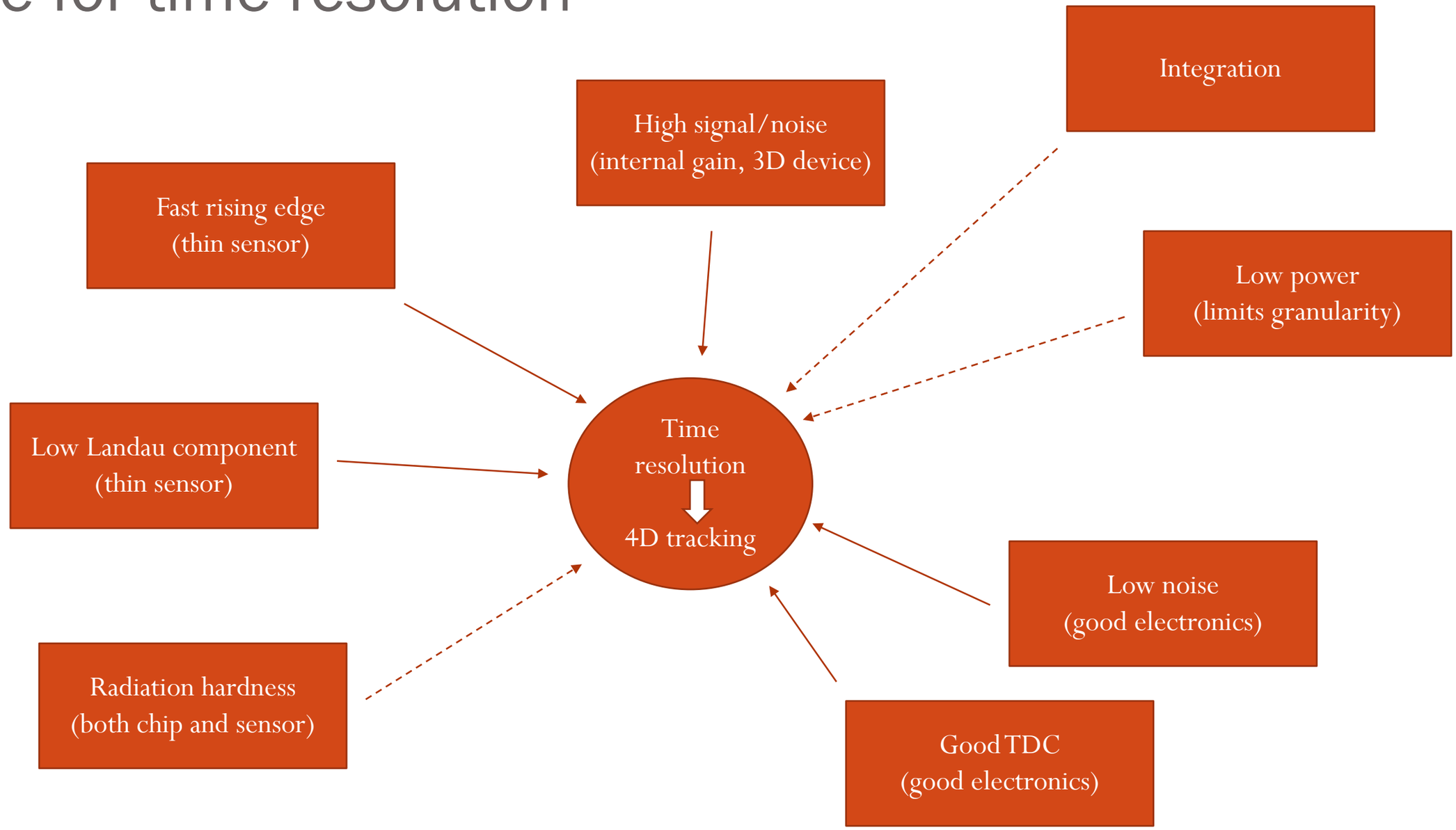
$$\sigma_{Jitter} = \frac{Noise}{dV/dt[CFD\%]} \approx \frac{T_{rise}}{SNR}$$

Time resolution main terms

$$\sigma^2_{timing} = \sigma^2_{time\,walk} + \sigma^2_{Landau\,noise} + \sigma^2_{Jitter} + \sigma^2_{TDC}$$

- Time walk: pulse-by-pulse variation
  - **Minimized with time of arrival correction**
  - (e.g. Constant fraction discriminator: use 50% of the pulse as time)
- Landau term: proportional to thickness
  - Charge deposition dis-homogeneity
  - **Reduced for thinner sensors**
- Jitter: from electronics
  - Proportional to $1/\frac{dV}{dt}$
  - **Reduced by increasing S/N ratio**
- TDC term: from digitization clock (typically small, ~7ps for ATLAS/CMS chips)

Recipe for time resolution

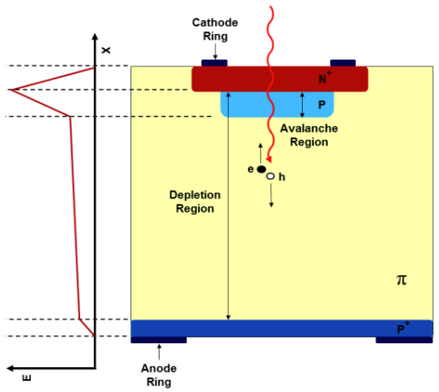


Sensors

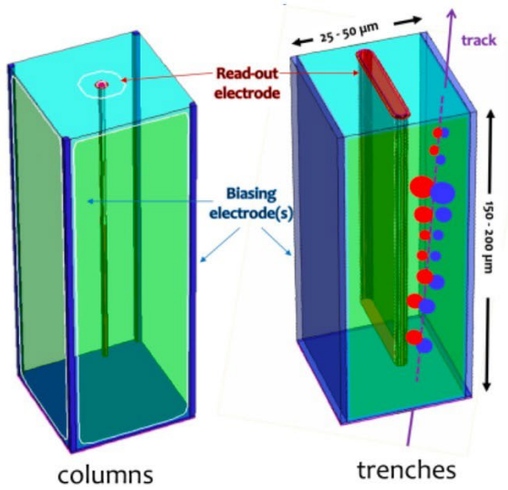
Time precision sensors

- **Which technology has sufficient time resolution for 4D tracking?**
  - Most technologies introduced here: https://arxiv.org/abs/2203.13900

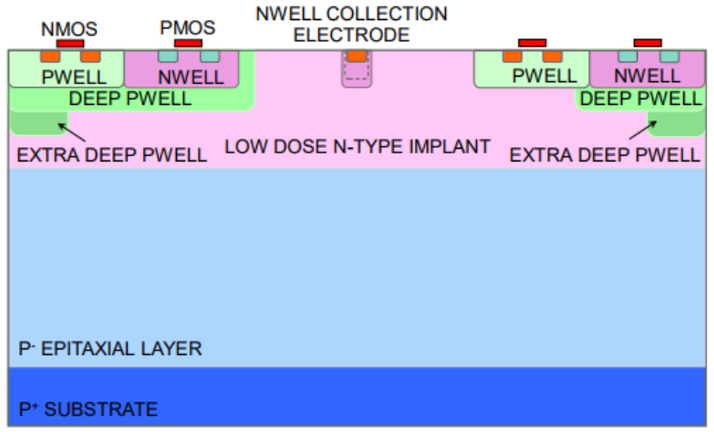
- **Low Gain Avalanche Detectors (LGADs)**
  - Intrinsic gain, thin bulk
  - High granularity LGADs
  - Innovative materials LGADs
  - Radiation hard LGADs



- **3D detectors**
  - Very fast charge collection perpendicular to charge deposition
  - Electrodes optimization

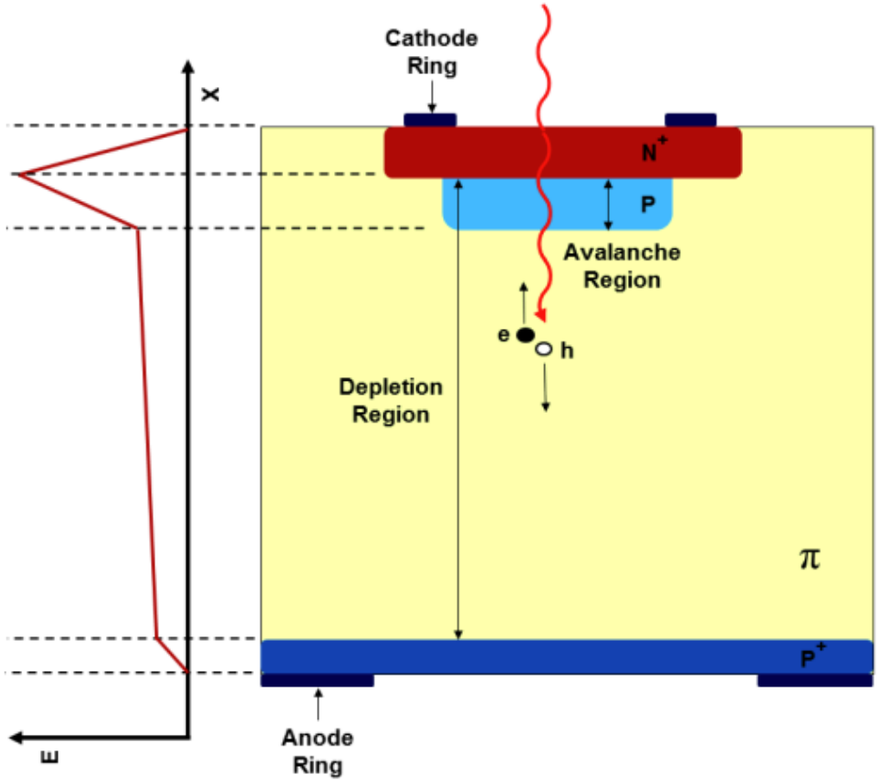


- **HV-CMOS**
  - Internal gain from integration
  - Improved time resolution
- **Small pixel detectors**



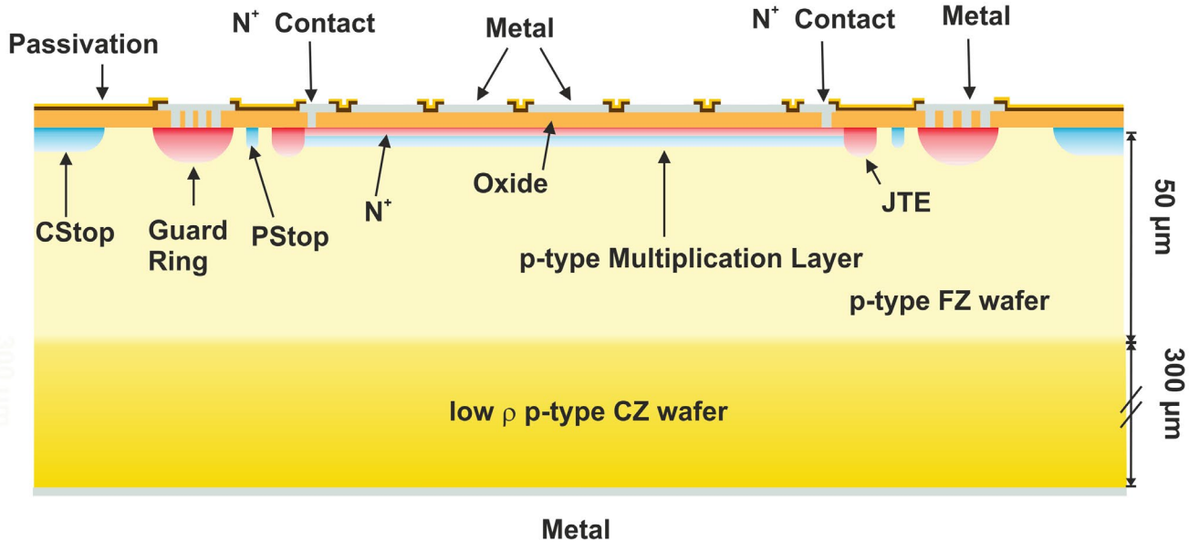
Low Gain Avalanche Detectors

- LGAD: silicon detector with a thin (<5µm) and highly doped (~10^{16} P++) multiplication layer
  - High electric field in the multiplication layer
  - Electron multiplication but not hole multiplication (not in avalanche mode, controlled gain)
- LGADs have intrinsic modest internal gain (10-50)
  - Gain = $\frac{Q_{LGAD}}{Q_{PiN}}$ (collected charge of LGAD vs same size PiN)
  - Better signal to noise ratio, sharp rise edge
- Better signal to noise ratio and thin detectors means improved timing resolution
  - **Time resolution down to 20 ps**
- Field protection structures currently limit granularity of LGADs
  - ~50-100 um inactive region between pixels
- But intensive R&D is ongoing to overcome this limitation

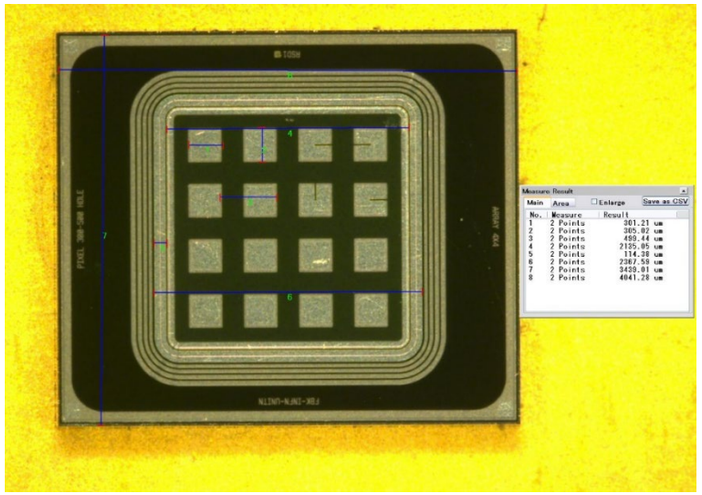


AC-LGADs

- Most advanced prototype of high granularity LGADs are **AC-LGADs**
  - (UCSC - US patent N. 9,613,993 B2, granted Apr. 4, 2017)
- Continuous sheets of multiplication layer and **N+ resistive layer**
  - N+ layer is grounded through side connections
- **Readout pads are AC-coupled** (Insulator layer between N+ and pads)
  - Allows for 100% fill factor and fine segmentation
- Intrinsic charge sharing between metal electrodes
  - Allows for precision hit precision better than $\sqrt{12}$
  - 5 um precision achievable for 500 um pitch



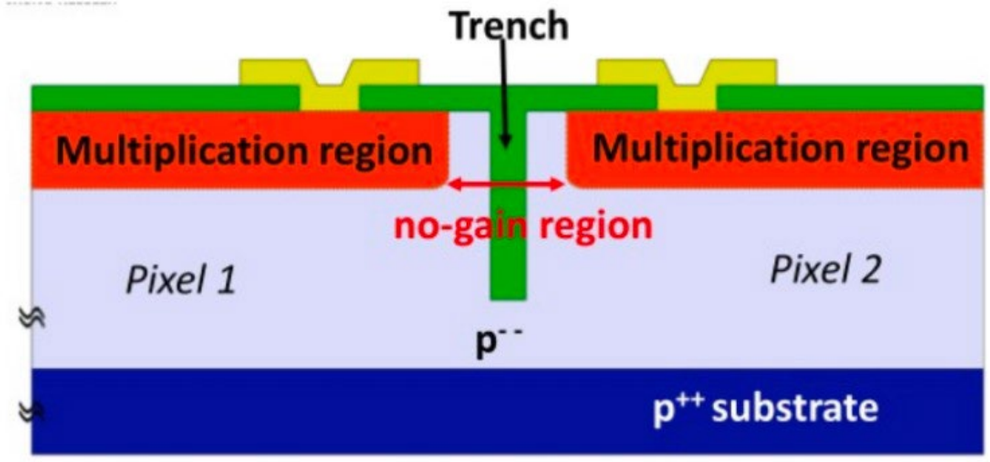
- **The response of the sensors can be tuned by modifying several parameters**
  - Pad distance
  - Resistivity of N+ layer
  - Oxide thickness
  - Pad geometry and dimension



Prototype AC-LGAD from FBK, 500 um pitch, 300 um metal

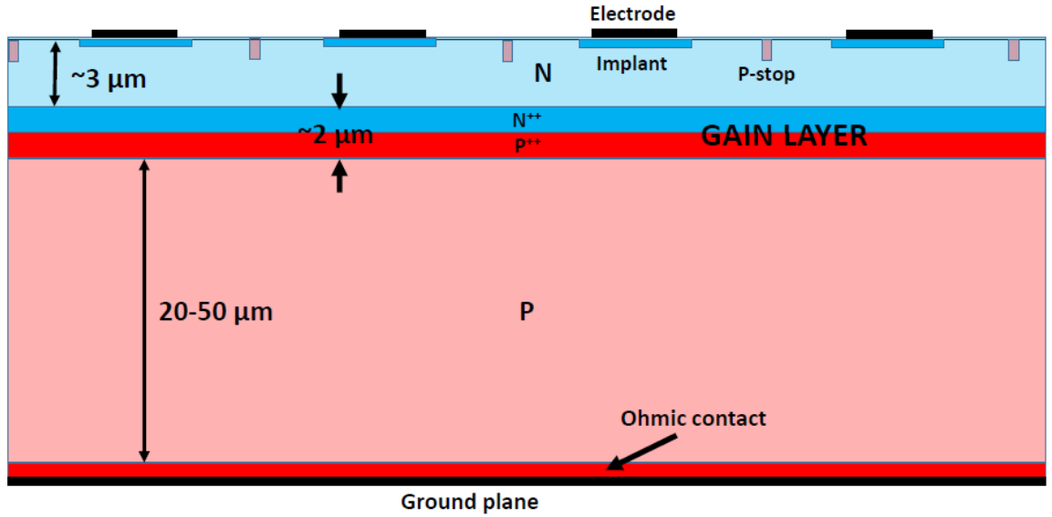
Trench insulated LGADs (TI-LGAD)

- Traditional DC-LGAD with trench insulation between pads
  - Prototypes produced by FBK: https://indico.cern.ch/event/861104/contributions/4514658/
- Proven to have very low IP gap: 5-10 um
- Time resolution and gain in line with standard LGADs



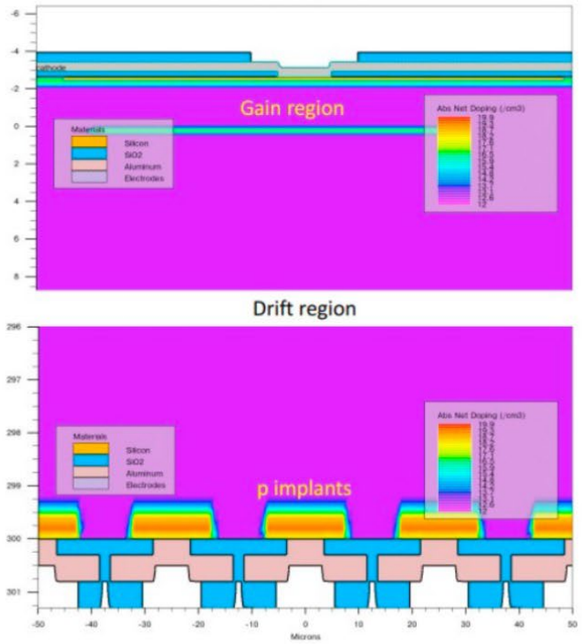
Deep-Junction LGADs (DJ-LGAD)

- P++ gain layer is paired with a N++ layer that lowers the field
  - Junction is buried ~5 um inside the detector
- Tuning of N+ and P+ parameters important
  - Low field outside of the electrodes while maintaining sufficient gain
  - No need for a JTE, standard silicon pixelization possible
- Effort ongoing to develop first DJ-LGAD demonstrator
  - **First prototype ready soon!**
- Additional efforts for HV-CMOS DJ-LGAD development
  - E.g. https://arxiv.org/abs/2206.07952



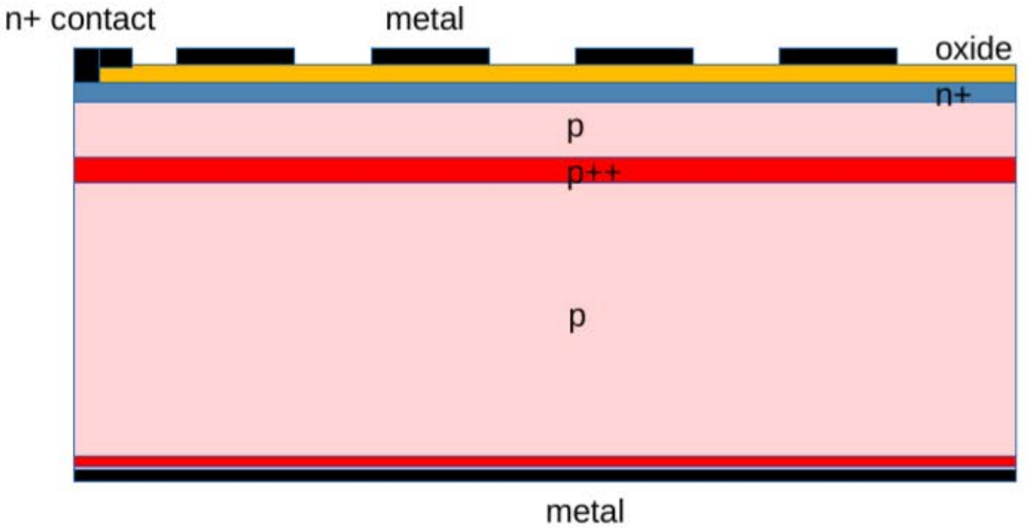
Double sided LGADs (DS-LGADs)

- Gain layer on the opposite side of the highly pixelated readout
  - On the gain layer side the readout is AC-coupled
- With thicker bulk 5D tracking is also possible



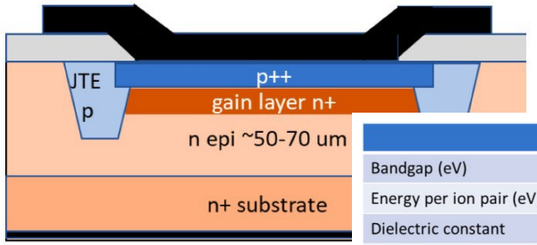
Buried LGADs

- P++ gain layer is buried ~5 um inside the detector bulk
- Increased radiation hardness with deep gain layer
  - Effect observed with not-so-deep gain layers already (~2.5 um) with many prototypes
- AC-coupled readout for high granularity



Silicon Carbide LGADs

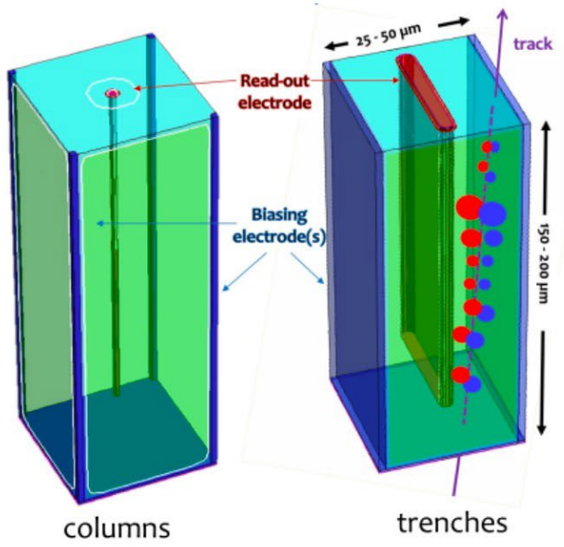
- Promising material that can increase even further LGADs performance
  - Thanks to the increased band gap and electron velocity
  - https://arxiv.org/abs/2203.08554



Property	Silicon	4H-SiC
Bandgap (eV)	1.12	3.27
Energy per ion pair (eV)	3.6	7.78
Dielectric constant	11.7	9.7
Breakdown field (MV cm^{-1})	0.3	3
Density (g cm^{-3})	2.3	3.2
dE/dx minimum (MeV cm^{-1})	2.7	4.4
Atomic number Z	14	~10
Electron mobility (cm^2 V^{-1} s^{-1}) at 300K	1300	800-1000
Hole mobility	460	115
Saturated electron velocity (10^7 cm s^{-1})	1	2
Threshold displacement energy (eV)	13-20	22-35
e-h pairs per micron	80	57
Thickness for equivalent signal (µm)	1	1.57
Thermal conductivity (W m^{-1} K^{-1})	130	370
Radiation length	9.4	8.7
Impact ionization coefficient	$\alpha_e > \alpha_h$	$\alpha_e < \alpha_h$

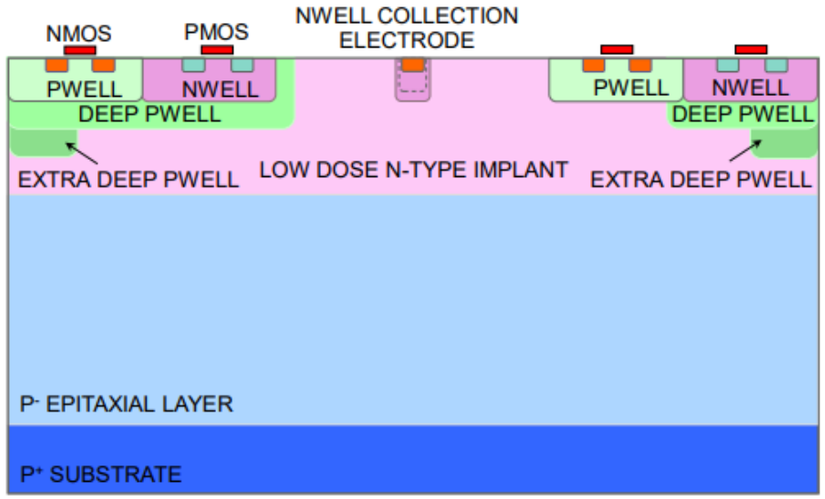
3D detectors

- MiP traveling parallel to electrodes allows for large charges deposition but with very fast charge collection
- Recent electrode optimization allows for homogeneous drift potential
- Time resolution down to 20ps



Monolithic

- State-of-the-art results from MALTA show < 2ns time resolution: suitable for ee colliders
  - https://arxiv.org/abs/2203.07626
- FASTPIX dedicated sensors optimizations achieve 120 ps resolution
- DMAPS CACTUS (150nm process, 1mm pixel pitch) <100ps resolution
  - https://authors.library.caltech.edu/103788/1/2003.04102.pdf
- SiGe BiCMOS SG13G2 (for ToF PET) <50ps resolution
  - https://arxiv.org/pdf/2005.14161.pdf



Small pixel detector

- Same sensor as a traditional silicon detector but utilizes small pixel pitch and 3D
  - integration (3DIC) techniques to create a low-capacitance pixel unit cell and readout chain
- Allows the detection of the induced current at the readout electrode
- Very fast rising edge (15ps) and angle of incidence information

Readout electronics

See next talk by D. Braga

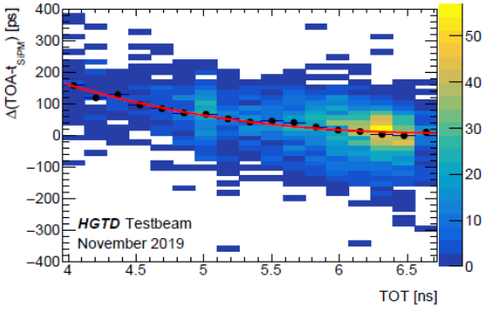
ROC (Read Out Chip) challenge

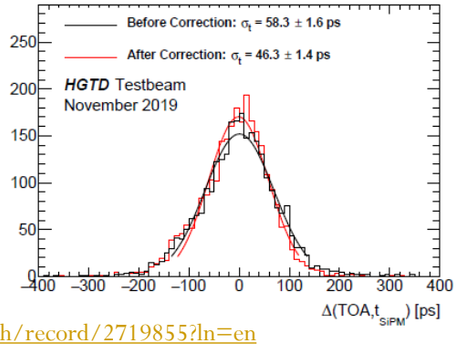
- Readout electronics has to maintain the time resolution of the sensor
- Simple ToA (Time of Arrival) method for timing not sufficient (time walk uncertainty)
- Time needs to be corrected in some way:
  - Using ToT correction (Time over Threshold) which measures the length of the pulse, current method used by ATLAS and CMS electronics
  - Using a variable threshold (eg: at 50% of the Pmax) → (CFD) Constant Fraction Discriminator
  - Etc…?

- HL-LHC timing ASICs are a revolutionary step forward to bring O(ps) timing to collider experiments, but use significant more space and power than what is required for 4D trackers
  - **Need R&D to minimize both power consumption and channel size**
- **Power consumption is and will be an issue for timing layers**
  - Especially when the granularity is lower than ~1mm

ASIC	Technology	Pitch	Total size	Power consumption	TID tolerance
ALTIROC	130 nm	1.3 mm	19.5×19.5 mm^2	5 mW/chan	2 MGy
ETROC	65 nm	1.3 mm	20.8×20.8 mm^2	3 mW/chan	1 MGy
RD53A/HL-LHC pixels	65 nm	50 µm	20×11.6 mm^2	< 10 µW/chan	5–15 MGy

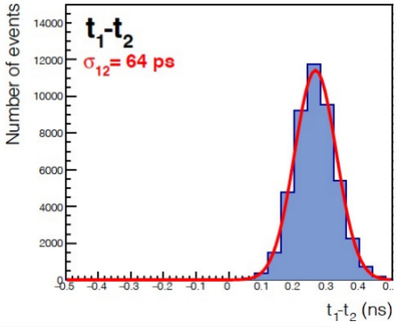
ATLAS readout chip (ALTIROC) ToT timing correction to ToA for time resolution evaluation





https://cds.cern.ch/record/2719855?ln=en

CMS ETROC, FNAL test beam



$$\sigma_i = \sqrt{0.5 \cdot (\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2)} \quad \sim 42 - 46 \text{ ps}$$

https://indico.cern.ch/event/1019078/contributions/4443946/attachments/2277823/3938539/ETROC1_TWEPP-v4.pdf

Electronics R&D efforts

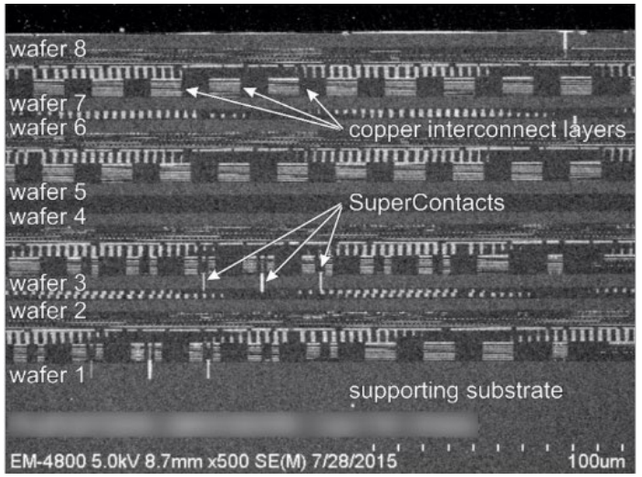
See next talk by D. Braga

- **Some current ongoing chip R&D projects:**
  - **CERN** EP R&D WP5 has promoted the selection of **28nm CMOS** node as the next step in microelectronics for HEP designs. Twice as fast and allows 4-5x circuits densities than 65nm.
  - **22nm CMOS** technology TDC design **Global Foundries** has been used by Fermilab extensively for cryoelectronics development for both Quantum control and readout electronics as well as cryogenic detectors (GF 22nm)
  - **Fermilab** is developing a chip based on the novel approach **to time-stamping LGAD signals based on Constant Fraction Discriminator (CFD)**, v0 version of the chip tested showing 20 ps Jitter
  - **SLAC has designed a TDC in 28nm** with bin size of 6.25ps to minimize the TDC component of time resolution to <2ps. Fabrication expected this year
  - **SiGe readout chip optimized for low power and 10ps resolution** are being produced by Anadyne Inc. and UC Santa Cruz (TowerJazz 130nm)
  - **Full waveform digitization chip** UC Santa Cruz is working with Nalu Scientific on a waveform digitization ASIC for AC-LGAD sensor arrays **(TSMC 65nm)**. First prototype being tested
- All efforts have the goal of producing a **reliable readout chip with high time resolution and low power**
  - Details: https://arxiv.org/abs/2204.00149

Integration

Advanced integration

- **3D integration** technology in industry currently allows tight packaging of sensor and chip
  - Improves sensor to chip connections in many ways
  - Additional aid to reach the goal of 4D tracking
  - https://arxiv.org/abs/2203.06093
- Not currently available in HEP, we need a community effort to make it available
  - Currently pursued by few groups together with small companies through DoE SBIRs



- **Very fine pitch** bonding (down to ~3 μm)
- **Better connection:**
  - Connections are shorter and faster than in circuit boards with long traces
  - Shorter connections also have reduced dissipated power
- **Better performance**: reduced input capacitance and lower noise
- **Integration of heterogeneous materials or different wafer technologies**
- **Reduction of single layer thickness**, after integration all supports can be removed
- See white paper https://arxiv.org/abs/2203.06093

Conclusions

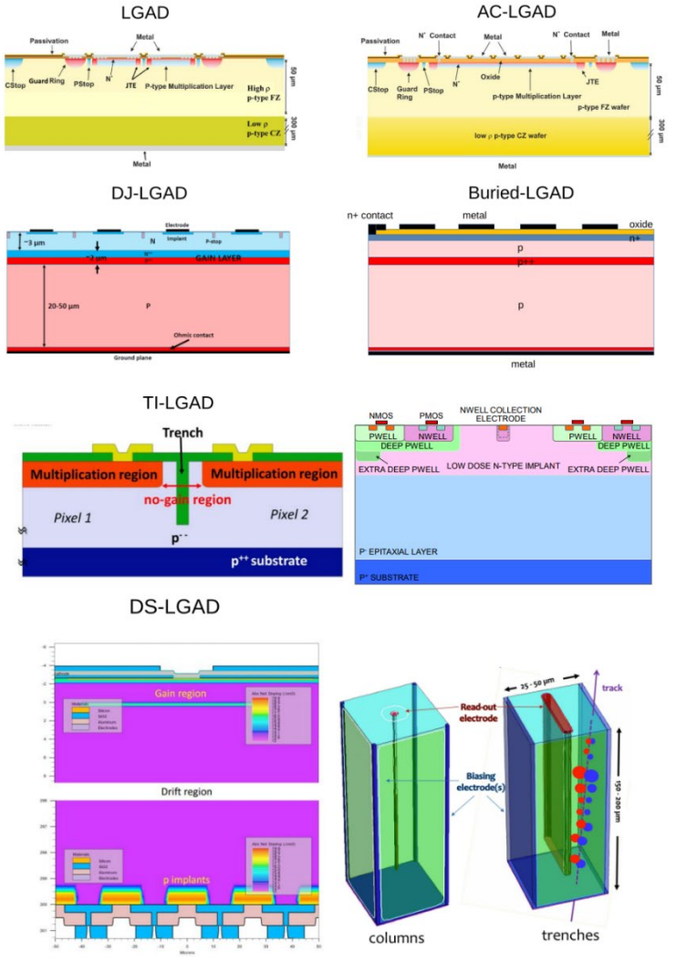
Applications and limits

- Different sensor designs feature unique advantages and weaknesses, **the choice of technology must be tuned to the specific application**
  - **AC-LGADs** have a **very high fill factor and rely on charge sharing** for hit reconstruction: **high position resolution for a sparse readout in low occupancy environments**. However, in a high occupancy environment this is an issue
  - **DC-LGADs** (TI-LGADs, DJ-LGADs …) can tolerate a **high occupancy environment**, but introduce non-zero dead regions between adjacent channels
  - **Double-sided LGADs** have a higher hit precision and **can detect the angle of the particle**, however they have a thicker bulk (resulting in reduced time resolution) and require additional readout channels
  - With **high radiation doses, Buried LGADs, thin LGADs or 3D sensors** are more robust
    - 3D sensors are less affected by radiation damage, however the lower material budged introduced by LGADs make them a more suitable choice for low mass trackers
- **High granularity readout chips** with high timing resolution are **limited by power consumption**
- Any sensor technology that is not monolithic requires integration with the electronics readout
  - **HV-CMOS** are an **integrated and cheaper** solution
  - Advanced packaging can help

Conclusions

- High precision timing will be very important in the next generation of particle/nuclear/astroparticle physics detectors
- Several technologies are being developed to achieve high time/spatial resolution or radiation hardness
  - Many based on LGADs, but also CMOS and 3D detectors
  - Each application has specific needs that can be fulfilled choosing the right technology
- Many efforts ongoing for developing a high precision and low power readout chip
  - Introduction of advanced integration would also bring improved performance

- **There's a very promising technology effort across several fields/groups to achieve 4D tracking**



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Thanks for the attention