



# SNSPD cold readout: activities and plans

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Snowmass Workshop 7/18/2022

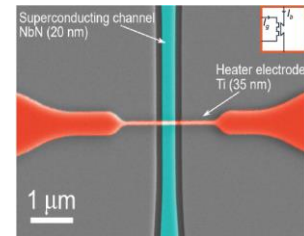
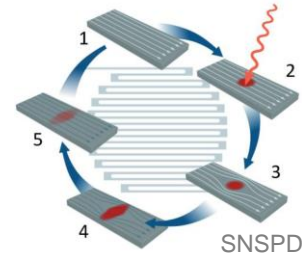
# DOE Microelectronics Co-Design Research: “Hybrid Cryogenic Detector Architectures for Sensing and Edge Computing enabled by new Fabrication Processes”

Advancement of two complementary classes of cryogenic state-of-the-art single-photon and particle detectors:

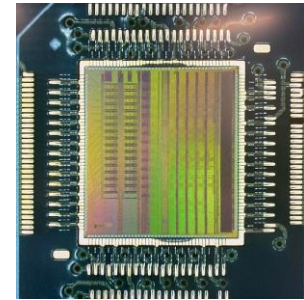
- the **Skipper CCD-in-CMOS** silicon detector
- a **hybrid detector platform based on superconducting nanowires**

Development and co-design of:

- advanced **fabrication and integration techniques**
- novel optimized **hybrid readout architectures**
- cryo-ASICs and cryotron-based superconducting electronics for **integrated sensing** and data reduction at source, through **feature extraction** and **edge computing**.

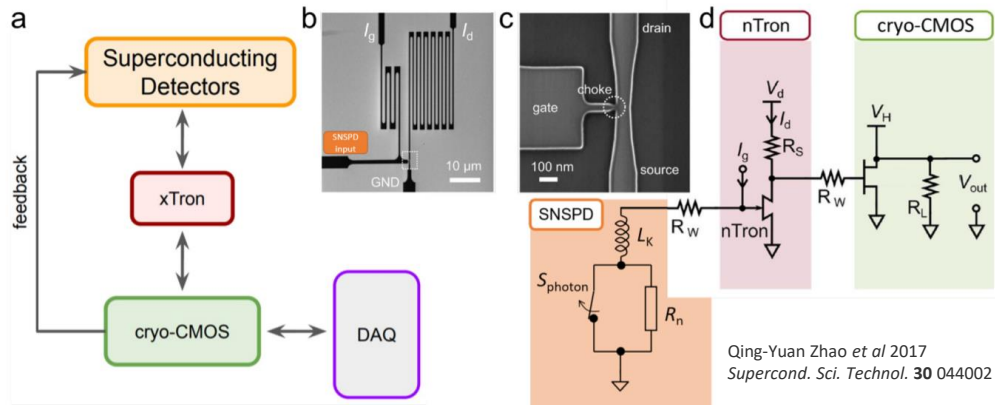


xTrons



cryoASIC

# Hybrid nanowire-based superconducting detector platform



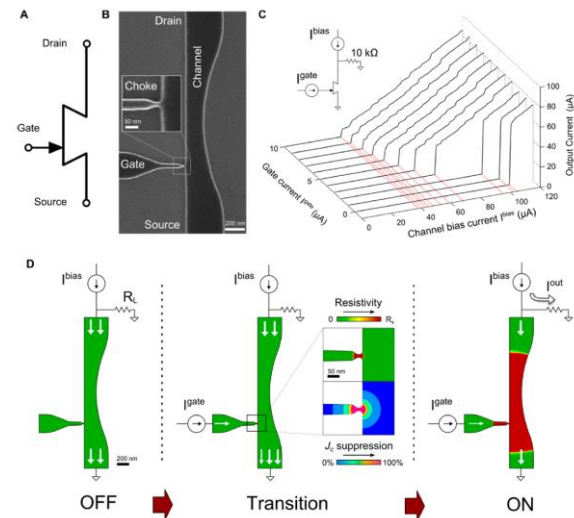
Hybrid architecture for cryogenic detectors, based on the co-design of:

- 1 – superconducting sensor (SNSPD),
- 2 – nanocryotron-based superconducting electronics (xTRON),
- 3 – cryoCMOS ASIC in nanometer scale (22nm FDX).

- develop the technology required for overall integration at cryogenic temperatures (Matt Shaw – JPL)
- SC and cryo-CMOS modeling and extraction (Synopsys, EPFL)

Goal: scalable, large count detector with edge computing and integrated sensing → on-chip DNN and physics-driven hardware codesign (e.g FNAL's Autoencoder)

Device-circuits-system codesign will concurrently enable large channel count, power optimization, impedance matching, edge compute and feature extraction, and data processing



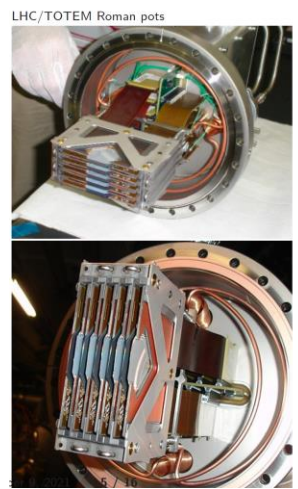
# Superconducting Nanowires Detectors

## As PHOTON DETECTORS:

- Highest performing detectors available for time-correlated single photon counting from the deep UV to the mid-infrared
- Demonstrated detection efficiencies as high as 98% at 1550 nm
- Timing jitter below 3 ps
- Effectively zero dark count rates
- Intrinsic photon number resolution
- Maximum count rates exceeding 1 Gcps in arrays

## As PARTICLE DETECTORS:

- Can have high segmentation ( $\sim 10\mu\text{m}$  “pixels”)
- Can be truly edgeless detector (important for beam monitoring)
- Operation in high magnetic field (5T)
- Radiation hardness to be investigated at Fermilab test beam facility



Exploited for photon detection (classical and quantum optics and communication)

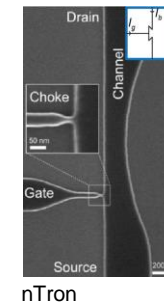
Unique capabilities for far-forward detectors that operate close to the beam (high T, high radiation, high segmentation)

# Superconducting Integration (Matt Shaw, JPL)

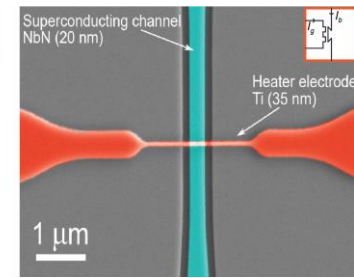
- Caltech/JPL to develop a nanofabrication process which will enable indium bump bonding of SNSPD focal planes to interposer structures,
- Evaluate the limits of ultra-high-density cryogenic microwave interconnects,
- and perform interface tests between SNSPD devices and digital readout electronics developed at FNAL and MIT.

# Nanocryotrons (MIT, K.Berggren)

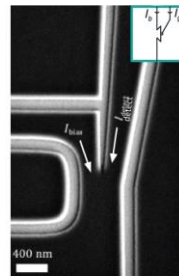
- Family of devices based on superconducting nanowires
  - Can thus be monolithically integrated with the nanowire sensor
  - Can be configured to operate as comparators, logic gates, signal level shifters, memories, shift registers...
  - Impedance matching drive high-impedance loads and drive following cryoCMOS stage
- Ideally suited for feature extraction and data reduction at the edge
- Evaluating radiation hardness (fabrication and architecture) and optimal energy budgeting
  - Developing increasingly complex circuits as well as work on yield



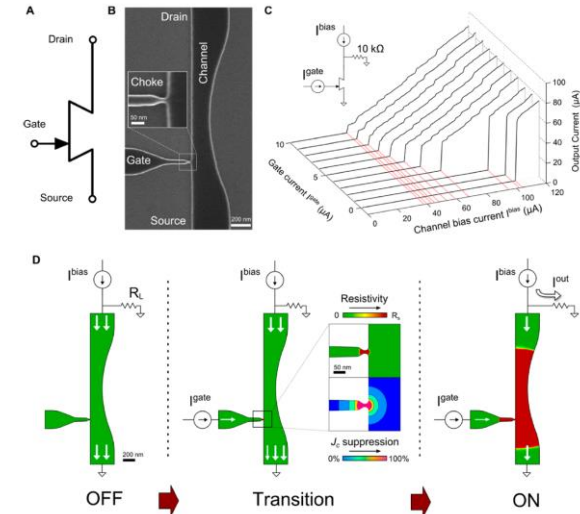
nTron



hTron



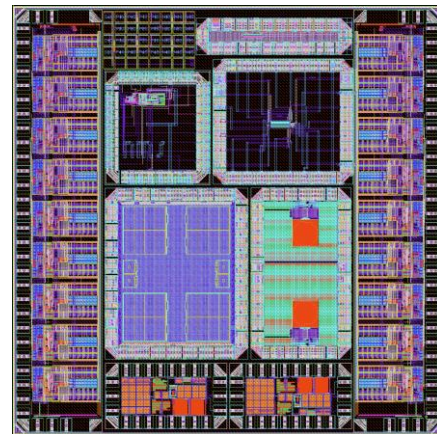
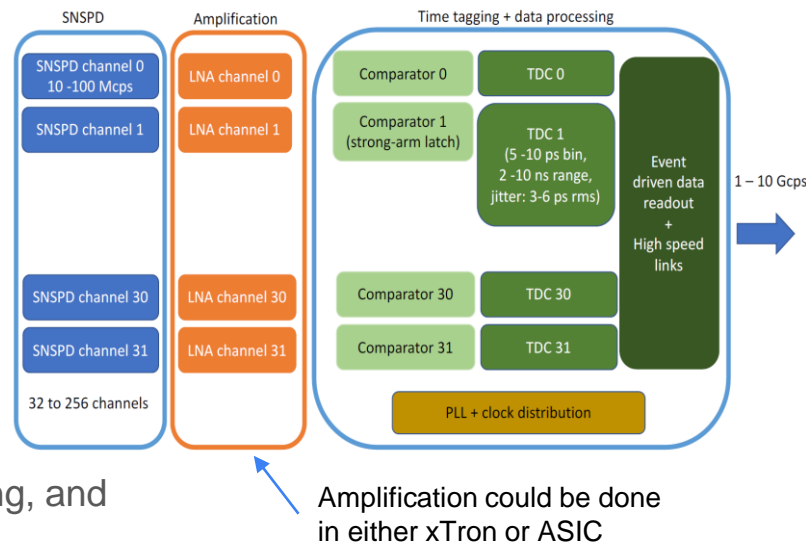
yTron





# CryoCMOS

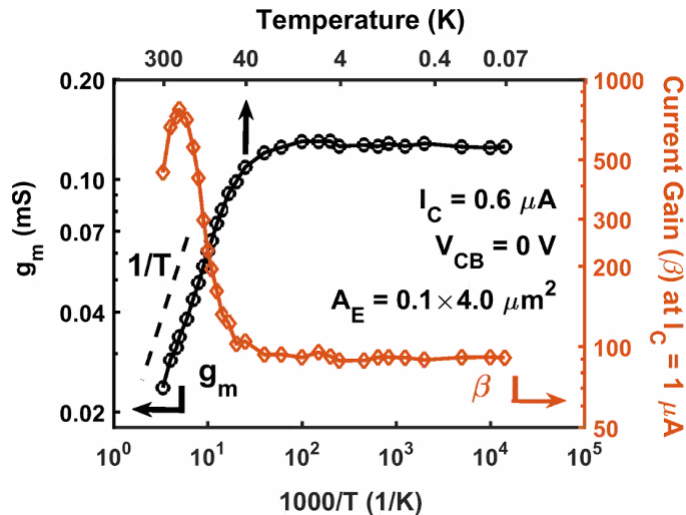
- Operation at <4K demonstrated in modern, state-of-the-art commercial processes (no special processing)
- Leverage low power, high performance ASICs for signal conditioning, time-tagging, data concentrator/edge computing, and serialization/readout
- Highlights:
  - SiGe HBT (high performance LNA)
  - FDSOI with backgate control to compensate for threshold increase at cryo
- Fermilab and EPFL currently collaborating on EAD-compatible cryomodels for Global Foundries' 22nm FDSOI



Fermilab's 22nm prototype

# SiGe Heterojunction Bipolar Transistors (HBTs) at cryogenic temperatures

- Unlike conventional bipolar transistors, when cooled SiGe HBTs exhibit **improved frequency response, current gain, noise, bandwidth, output conductance and other performance metrics**.
- **BiCMOS** (SiGe HBT + Si CMOS) platform **ideal mixed-signal technology** that marries high-performance SiGe HBTs for analog, RF, and microwave circuits, with Si CMOS to support highly-integrated system functionality.
- Fabricated on large wafers (300 mm) at **high yield** and **low cost** using conventional silicon processing techniques and silicon economy-of-scale.
- SiGe HBTs cooled to temperatures as low as 70 mK demonstrated operability for a variety of interesting circuit designs (gain of 2000 at 100 mK at only a few  $\mu\text{W}$  dissipation).
- At sub-K, the amplification principle becomes fundamentally quantum mechanical in nature, as tunneling becomes the dominant transport mechanism. **Constant operation across temperature below  $\sim 7\text{K}$ .**





## SC and cryo-CMOS modeling and extraction

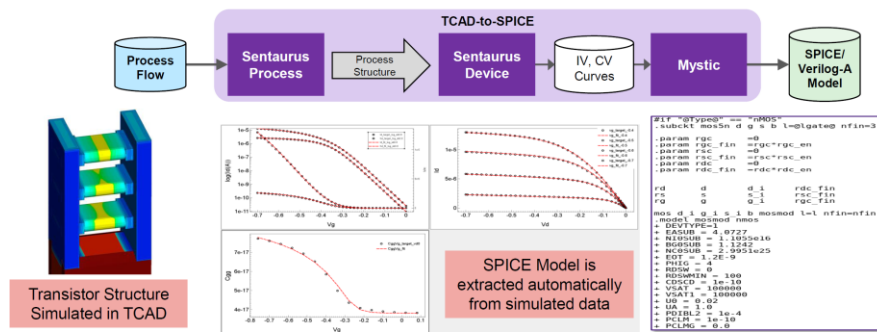
In collaboration with Synopsys

- SC electronics models (MIT, FNAL)
- cryoCMOS models (FNAL, EPFL)
- Prototyped a test structure for  $1/f$  noise measurement

Now simulating CMOS + xTron + SNSPD

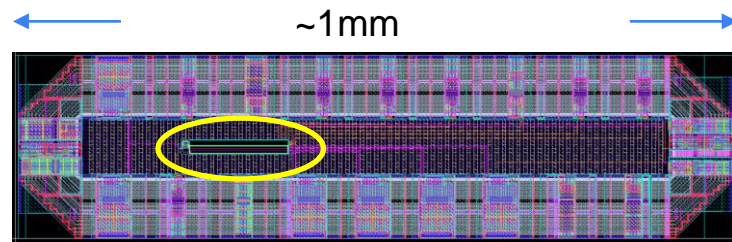
## TCAD-To-SPICE Sub-Flow Extracts SPICE Model From TCAD Before Wafers Are Available

Mystic extracts SPICE or Verilog-A compact model from Sentaurus Device Output



# cryoASIC readout and control

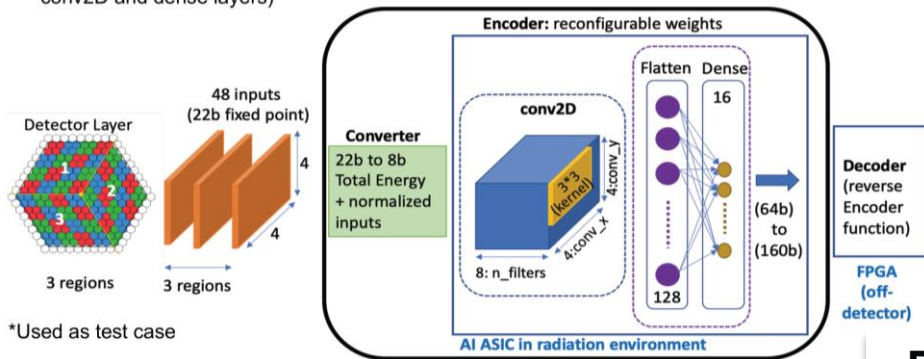
- xTron driving directly comparator for binary readout
  - Active quenching biasing from ASIC can reduce the deadtime of the nanowires
- Prasana Ravindran, Risheng Cheng, Hong Tang, and Joseph C. Bardin, "Active quenching of superconducting nanowire single photon detectors," Opt. Express 28, 4099-4114 (2020)
- CryoCMOS allows for fine resolution TDCs for time tagging
  - Fermilab prototyped a 22nm cryo TDC for 5ps resolution and >10ns range (7b fine, 10b coarse), <0.5mW
  - Digital readout:
    - Event driven, serializer, line drivers, etc.
  - Feature extraction:
    - Correlation between detector layers
    - Event selection/reconstruction
    - DNN



# HL LHC High Granularity Calorimeter\*: Data flow

## CNN: Encodes information by correlating spatial features

- conv2D layer** – extract spatially correlated geometric features
- Flatten layer** – Vectorizes the 2D image from the conv2D layer [ $8 \times 4 \times 4 = 128 \times 1$ ]
- Dense layer** – aggregates the various features to provide higher order information
- ReLU** – an activation function which introduces non-linearity by applying thresholds (part of both the conv2D and dense layers)



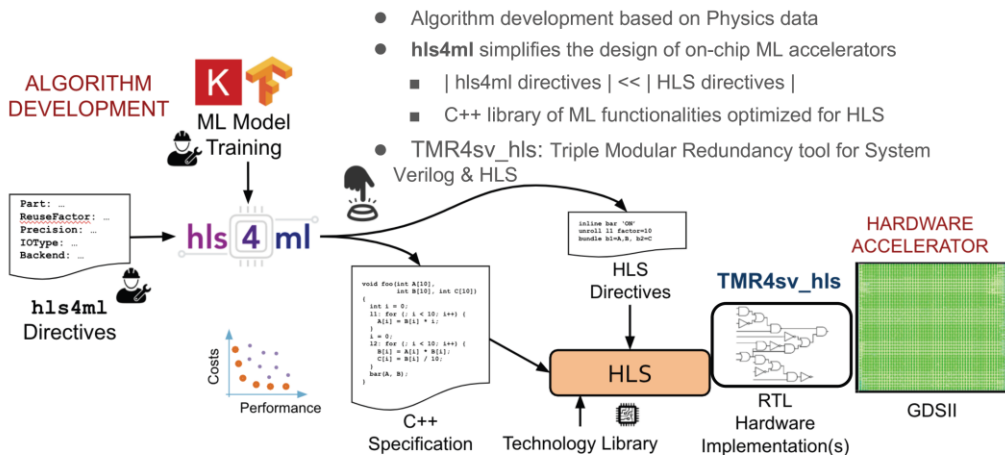
\*Used as test case

## Example of recent on-chip DNN and physics-driven hardware codesign at Fermilab

(Farah Fahim, Nhan Tran)

- Physics inspired autoencoder
- Ultrafast inference every 25 ns
- Operation in extreme radiation environment (use of triple modular redundancy for SEE mitigation)
- Successful chip test results
- hls4ml- AI ecosystem for fastML application, widespread community adoption
- Part of MLCommons™ with Open Datasets and Tools to Drive Democratization of Machine Learning

## Physics Driven Hardware Co-design



# Collaborators

## 6 Thrust:

### **cryoASIC**

(Lead: Davide Braga, Fermilab)

### **Skipper-in-CMOS**

(Lead: Juan Estrada, Fermilab)

### **Superconducting Electronics**

(Lead: Karl Berggren, MIT)

### **Superconducting Detectors**

(Lead: Whitney Armstrong, Argonne)

### **Cryogenic Integration**

(Lead: Matthew Shaw, JPL)

### **Codesign Tools**

(Lead: Ricardo Borges, Synopsys)

