DUNE Single Phase Cold Motherboard and ASICs

Report of the Preliminary Design Review

05–07 February 2020

Contents

1. Executive Summary

This document is the report of the Preliminary Design Review (60% design maturity) of the cold ASICs and Front-End Mother Board (FEMB) for the DUNE single phase TPC. The review was held at CERN on February 5–7, 2020 to evaluate the preliminary design of the 3-chip (LARASIC, COLDADC and COLDATA ASICs) and single chip (CRYOASIC) solutions and their associated FEMBs.

The committee would like to commend the team for putting together an as comprehensive as possible overview of the ASIC designs and FEMBs, and for responding to all the review committee questions promptly. The committee found the documentation and presentations useful in evaluating the maturity of the design, although the impossibility to have full access to some of the ASIC schematics has been limiting the work of the reviewers.

The committee believes the current design does meet the standard for a 60% maturity. The committee has identified a number of recommendations which should be addressed. Many of these recommendations relate specifically to completing the specifications and to the design as well as design and verification methodologies of the ASICs.

The report addresses the specific charge questions with **findings and comments** (statements of facts that summarize noteworthy information presented in the review, and judgement statements about the facts which should be evaluated by the project team and action taken where appropriate), and **recommendations** (actions that should be addressed by the project team). The answers the committee reached for each of the charge questions can be found at the end of this document.

2. Review Committee

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3. Agenda and Documentation

Agenda and documentation are available on the indico site: https://indico.fnal.gov/event/22423/other-view?view=standard

4. Findings and Comments

The status of the design of the ASICs which could possibly be used for the readout of the DUNE single phase TPC was presented. Two alternatives are considered:

- One based on a single readout ASIC (CRYO) of 64 channels and including the front-end pre-amplification and shaping, a 2 Msps ADC and an interface to the Warm Interface Board (WIB).
- The other one based on 3 ASICs, a 16-channel pre-amplification and shaping ASIC (LARASIC), a 16-channel ADC ASIC (COLDADC) and a 64-channel ASIC interfacing to the WIB (COLDATA).

The design status of two types of front-end mother boards (FEMB) were also presented. Both FEMB read out 128 channels. One is housing 2 CRYO ASICs (and possibly external LDOs if the CRYO internal LDOs are not used) while the other houses 8 LARASICs, 8 COLDADCs and 2 COLDATAs and a few other chips (e.g. LDOs).

Although the design teams made open and complete presentations, the design reviewers have been disappointed of not having been able to see all the schematics. This limits the efficiency of the review, can cause misunderstandings and such a restriction should not happen at the time of the final design review or of the production readiness review.

In the following paragraphs, findings and comments will be given for each of the 4 ASICs, the FEMBs and system issues.

4.1. Specifications

Additional specifications are to be defined and some existing specifications are to be modified. For instance, the 220pF detector capacitance is to be updated to 150pF, and additional specification concerning double pulse resolution, specifications of the clock received by the FEMB (e.g. maximum jitter), specifications concerning the admissible ripple on the power lines are to be added. The minimum required ENOB should be specified at a particular frequency (general comment not related to CRYO specifically).

4.2. CRYO ASIC

The CRYO ASIC uses the 130-nm CMOS technology from TSMC. The chip was initially designed for the nEXO experiment but could be adapted to the DUNE TPC. A first version is already available and has been bench tested. A second version, optimized for the nEXO detector was submitted last Fall and is expected in the course of February. A third version adapted to DUNE is currently being designed for a submission in July 2020.

The technology characterization at cryogenic temperatures was performed at SLAC in 2017. From this, characterization cold models have been extracted for both the DC and noise characteristics of the transistors. The test structures include 8 different type of transistors (nominal and low-Vt) at 2.5V and 1.2V and 256 devices have been characterized across cold temperatures (-113^{o} C and -186^{o} C). These cold models were used to fully design CRYO at the target temperatures although the digital part of the design has been using standard TSMC libraries.

The low temperature models are extracted for nominal parameters and no simulations were shown for the corners and mismatch. The cold models consider corners by adapting the same process variations of the model card from foundry. The cold models do not support Monte Carlo analysis. Monte Carlo simulations were done using the models of the foundry at room temperature and -40°C. This should be carefully studied to make sure that there is margin for the performance of the final system built from production lots.

In order to improve the reliability and the lifetime of the device, the Vdda and Vddd of the analog and digital parts is reduced to 1V and 2V respectively. This should drastically reduce the hot carrier and such measures have been used and validated in other designs. There have not yet been lifetime tests but they will be done in the near future. It is noted that the reduction of Vdd is deemed sufficient by the design team and that no minimum channel length rule has been introduced.

An important warning is given by one of the reviewers: there is a bug in the TSMC130 Bsim3 noise models leading to an underestimation of the thermal noise towards weak inversion up to 50% (weak) while it is correct for strong inversion. A solution to this problem is to use Spice2 level for the thermal noise. As a result, one will get slight overestimation of gamma factor (gamma always 0.66 independent of the inversion factor) and consequently the simulated noise. To do that one should modify the parameter noimod=2 to noimod=3 in scs file. The thermal model will be described by SPICE2 and the flicker model is still described by BSIM3V3.

As already said, no detailed schematics were available to the review committee and there are no specifications nor simulation results for important elements, such as the power supply rejection ratio (PSRR). This is particularly important as the input stage of the pre-amplifier is a single ended amplifier with a PMOS input transistor which is referred to the positive supply and not optimal for PSRR at high frequency. The design includes internal LDOs to power the different power domains. It would be good to see the PSRR figures with and without the internal LDOs activated. The design team will provide the following information in the coming days: simulation results of the PSRR of the full frontend chain up to the sample and hold with and without the LDOs.

The phase margin of the preamplifier is larger than 80^{o} in all conditions of gain and shaping time.

The phase margin of the low noise LDO is higher than 90°. This is obtained with nominal decoupling capacitors (2 external 100µF silicon capacitors) and including the bonding connections and the parasitics of the capacitors.

The transient behavior of the LDOs should be looked at. For example, its behavior should be looked at when the clock disappears and then comes back.

It is noted that, when used, the internal LDO error amplifiers see the full 2.5V. As all devices used in the LDOs are 2.5V devices and as there are no minimum L devices in the LDOs there should not be any problem. It is also foreseen to conduct lifetime studies of the LDOs at 2.5V.

The tests of the first CRYO version has been done with the inputs loaded with discrete capacitors to emulate the wires. The review team believes it is important to have measurements made with the chip connected to the APA wires (which cannot be properly modelled with a single capacitor). This is important to have final noise estimation and to verify there are no stability issues in the final system. The design team foresees such a test to be done beginning of July with the nEXO version of CRYO. It is recommended that the submission of the DUNE CRYO be done after this test is performed.

There is some discrepancy between the simulation and the measurement of the noise for bare chips. Although some improvements might be expected from a better design of the test board, part of the problem may come from the internal design of power/ground grid (resistance of the connection for the input transistor etc.) and/or a poor PSRR. This should be studied.

Since the architecture of input stage feedback of CRYO is similar to those of LARASIC, one could expect a similar "ledge effect" when there is an input overdrive. CRYO does not exhibit a similar "ledge effect" with an input charge of up to 250fC. Simulation with an overdrive of x5 to x10 the maximum expected dynamic range of 80fC should be performed.

No measurements and simulations on cross talk were presented. This is being addressed with the help of other institutes (MSU and Hawaii) and testing should be done early April.

The eye diagram presented is not a real eye-diagram (clock signal instead). To assess the quality of the signal a PRBS eye-diagram is needed. This should be measured at the end of the long cables (25m). So far, no pre-emphasis is included in the LVDS driver of the 896 Mbps output serial link. Tests with long cables will be done soon and if needed an existing pre-emphasis will be included for the next submission.

It is noted that the clock jitter is high (~60 ps). Although it's neither an issue for the 12-bit ADC (given the signal bandwidth) nor the data transmission (at 896 Mbps), this seems to be relatively high and it might be useful to understand the cause of the jitter.

An external clock has been used for the measurements of the ADC linearity. The performance when using the internal clock should be measured.

A measurement of the "full chain" has been presented. Such a measurement should be done when all the ADCs are working and when only one ADC is active.

It is noted, that although it is well within specifications, the power dissipation of the ADC is quite large compared to state-of-the-art similar designs. The ENOB estimation is optimistic if one considers the full range but realistic in the expected use range.

Performance measurements should be made at 2 MSPS with a 300 kHz (or whatever is most relevant) signal. It should also be made at Nyquist frequency.

Cross talk studies with saturated signals should be done.

Measurements of noise and linearity with the nominal speed ADC and a fully functional multiplexer are needed to validate the design.

Concerning the design and verification methodology, the review committee has some concerns. During the meeting, the review committee did not understand why the loading problem of the latch into the multiplexer was not seen during the verification phase. This is due to the fact that this effect shows up only in an extracted view simulation which was not performed on this section. The verification methodology will be reviewed. As analogue on top is used, a detailed description (register level) of all the interfaces and clocks (ADC <-> ENCODER <-> SERIALIZER) is needed.

The two output serializers work at 896Mbps which is enough to transmit the ADC data of the 64 channels but which does not leave any space for transmitting special characters (e.g. comma characters) or extra information such as the time stamp of the events. While the 12 to 14-bit encoding of the ADC data is used to detect data transmission errors, the synchronization must be maintained/monitored at the system level without this time stamp information. During the questions/answers session, the design team clarified how the synchronization is initialized and maintained at the system level.

The presented list of modifications/improvements for the next submission is justified and the schedule for implementing them and be ready for a new submission (in July 2020) is realistic. However, it assumes that the tests to be done with the version expected in February are done rapidly and successfully. This part might need to be revisited.

It is suggested that the CRYO team considers an additional ADC that may be powered down when not in use or powered up to monitor analog bias, power and other important parametric information including the input voltage to the ASIC.

It may be useful to consider splitting CRYO into two 32 channel ASICs to spread out the power density from 1.6W to 0.8W and reduce the input trace crowding.

4.3. COLDADC

The design of the COLDADC is very conservative (in particular its power consumption is high with respect to state-of-the-art ADCs) and as a consequence no major issues have been discovered. However, the first version had some problems, mostly due to miscommunication between designers and this indicates that the design methodology and the verification methodology need to be improved.

The power consumption is much larger than state-of-the-art designs but is within the specifications.

The ENOB is taken optimistically, but in the worst case will be 10bits and there is plan for improvement. The minimum required ENOB should be specified at frequencies of interest for data taking.

Performance measurements should be made at 2 MSPS with a 300 kHz (or whatever is most relevant) signal. It should also be made at Nyquist frequency.

Cross talk studies with saturated signals should be done.

The large spread in the measured power consumption must be understood.

Lifetime tests are still to be done.

The presented modifications to fix the few issues observed during testing are properly justified. However, the review committee has two remarks:

> The IR drop is a possible cause for the non-linearity observed on the first version and this is indirectly confirmed by running the chip at higher voltages. However, a complete IR drop analysis should be done to confirm this suspicion.
>
> It is not sure that a larger size of the analog multiplexer would solve the problem observed during measurement if it is really due to higher threshold at low temperatures. Hence, the use low Vt transistors for the switches might be considered.

A submission of a new COLDADC in April is deemed realistic.

4.4. COLDATA

The design is sound and the design and verification methodologies (digital on top and UVM) are properly defined and implemented.

The output serial links have enough bandwidth for transmitting both the ADC data and additional comma characters and timing tag.

It should be verified that the time constant of the Power-On Reset is compatible with the ramp up of the system supply. It is noted that simulations have already been done using a pSpice model of the LDO (TI TPS74201) that is used on the FEMBs.

When at room temperature, the PLL requires a voltage larger than the design target (1.1 V) to oscillate. This problem does not appear at cold. The Vdd range for which the PLL starts has been evaluated by simulation. After having seen the schematics, it is agreed that the small gm is probably the cause for the VCO failing to oscillate. Increasing the transistor sizes will solve the problem as shown by simulation. This gives about 100 mV margin. This margin is to be evaluated for all corners.

The direct connection of the gm cell to Vdd is relatively sensitive to supply noise. This can be improved by employing a “filtered” current source architecture. However, this will limit furthermore the minimum operating voltage of the VCO. It is suggested to study this option.

Lifetime tests are still to be done.

It is understood that the way the clocks are handled in the system is due to historical reasons. The DUNE timing is based on a 62.5 MHz clock transmitted to the FEMB and used to define the time tag. It’s from this clock that the sampling clock of the ADC is derived. The data transmission runs at 1.28 Gbps and derives its clock from a local 40 MHz oscillator located on the FEMB. Although this works, it could be simpler to use the 62.5 MHz as a master clock for everything and it would avoid the need for this extra

40 MHz oscillator (for which no reliability data has been presented). The fact the PLL is to be modified might be a good opportunity to consider this option.

4.5. LARASIC

The LARASIC design has a long history and is now very mature and understood.

As expected, the presented PSRR is bad at high frequency but thanks to the use of LDOs and to the limited bandwidth of the signal, the performance remains reasonable.

The option of having a weak ESD protection to try and limit the capacitive load on the inputs is questionable. Although diodes are used on the FEMB's the chip is going to be packaged and there must be ESD protection strong enough to avoid possible large yield losses due to handling prior to assembly and act as backup for external protections on the FEMB. The design team mentions they did not get any problems while packaging the 5,000 chips that were fabricated for ProtoDUNE. However, the presented protection is using two standard NMOS of dimension 4.8µm/0.96µm. The area of the diodes is small when compared to standard ESD diodes. For comparison the ESD protection in ABC130 chip (using IBM 130nm and unpackaged) the ESD protection has been scaled down to 80µm/0.12µm and the level of the protection was only 1.5kV HBM i.e. below required standards for packaged chips (usually 4kV HBM). The design team should consider improving the ESD protection on the input pads.

The configuration of the LARASIC is done through the COLDATA and uses an SPI interface. The double transmission of data to make sure there is no error is surprising to the reviewers.

4.6. Front-End Mother Boards (FEMB)

The designs are not mature for all options. In particular, the single board option for the 3-chip solution is still in a very preliminary phase. It is recommended to pursue this solution as it has a lot of advantages. The FEMB for the CRYO is currently assuming a chip on board is used. In case a packaged version of CRYO is needed, the design will have to be changed but that's not a problem. The effect of the package on the CRYO performance (e.g. possible stress) would require analysis.

The shields of the cold data cable are connected on both ends (i.e. on the FEMB and on the signal feed-through flange board), following the DUNE grounding and isolation rules, which have proven to be working well.

The review committee appreciates the effort to improve reliability and lifetime of PCB by modifying via aspect ratio and selected solder process. There should be a QC plan for FEMB production and consideration should be given to adding test points that would simplify testing to be done after assembly. For example, it might be a good idea to add test points that can be easily used to accurately measure the voltage output of each of the LDOs. Careful consideration should be given to making sure that the FEMB is supported in such a way as to prevent possible flexing. This is especially important if the decision is made to change from the mezzanine solution to the single board solution.

4.7. System and general issues

Communication to the COLDATA chips from the WIB should be reassessed for what happens if one of the chips loses power. Input protection linked to the on chip positive supply could prevent logic levels for LVDS or CMOS data lines from reaching their proper logic levels. Referencing protection on these lines to GND can serve to eliminate this issue.

It would be useful to have analog monitoring of bias voltages and important references internal and external to the ASICs in ProtoDUNE II and in Dune if feasible. If possible, an external voltage could be generated in the warm and sent over a multi-use copper line to keep track of the ADC accuracy through a programmable mux.

It is suggested that ProtoDUNE II have a moderate number of 23m (bottom side) cables (~10) to ensure that there are no lurking problems over extended periods of operation in the cold.

The timing synchronization method based on time stamp is deemed efficient. For the 3-chip solution a time stamp is sent from the FEMB to the WIB. For the CRYO solution, the time stamp can be implemented at the WIB level because of the synchronous data transmission and control lines that will deliver all samples in a known sequence.

The phase adjustment for handling cable length differences is available for both options.

The way possible LAr boiling is managed still requires some work, especially for the CRYO option for which the power density is higher.

The quality of the clock received by the FEMB is important for the precision of the sampling time of the ADC (although the signal bandwidth does not set demanding performance requirements) and also for the 1.28Gbps readout serial links quality. It is hence important to evaluate the maximum allowed jitter and put this as a specification.

There should be a QC plan for the cables, both power and signal, between the WIB and FEMB (although we understand that the vendor will test 100% of the cables for connectivity).

5. Recommendations

1. A complete and coherent list of specifications from both developments should be agreed and established. This includes:
    - Input capacitance to be updated (150pF instead of 220pF)
    - Maximum allowed clock jitter on the received clock
    - Maximum noise on power supplies (ripple vs frequency) and expected range of allowed PS
    - Minimum acceptable ENOB. Is 10 bits enough?
    - Double pulse resolution and settling time
    - Overload recovery (maximum recovery time vs overload)
    - Maximum acceptable crosstalk
    - Specifications for the FEMB (there are currently none)
    - For the 3-chip solution, all the interfaces (clocks, communication, data path) between COLDATA, COLDADC and LArASIC are to be fully specified and documented. It is recommended to review these specifications with all development teams prior to submission of these chips.
2. The ASIC specifications, for parameters such as “ENOB”, “SNR”, noise and others, must explicitly list the testing conditions, such as the loading capacitance and shaping time for the noise tests, the sampling frequency for the ENOB tests, and so on.
3. The design methodologies and verification methodologies need to be clarified and improved for all the ASICs.
4. Concerning the cold temperature models, a drop-in test structure with standard transistors could be designed and used to follow lot to lot process variations in the cold. This methodology

is used for checking the radiation hardness of some technologies: test structures are added to each submission and measured. Transistor matching data as a function of temperature should be derived from measurements and used in simulations.

5. A program and protocol for accelerated aging tests should be agreed and established for both solutions.
6. Using a single clock source as master clock for all functions should be considered for the 3-chip solution (already done for the CRYO solution). In particular, as part of the design changes to be done for the COLDATA PLL, it should be considered to use the master 62.5MHz clock as input.
7. For the 3-chip solution, the design of a single FEMB housing all the chips (i.e. no mezzanine) is to be pursued.
8. The DUNE CRYO ASIC should be submitted only when all missing tests with nEXO version are finished. In particular, the test with the APA is to be done prior the submission. The schedule of this test is to be revisited if the DUNE CRYO is to be submitted in July.

6. Answers to the Review Charge

1. Are the requirements for the ASICs and FEMBs sufficiently well documented?

There are specifications to be updated and some missing specifications. This includes:

- Input capacitance to be updated (150pF instead of 220pF)
- Maximum allowed clock jitter on the received clock
- Maximum noise on power supplies (ripple vs frequency) and expected range of allowed PS
- Minimum acceptable ENOB. Is 10 bits enough?
- Double pulse resolution and settling time
- Overload recovery (maximum recovery time vs overload)
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- Specifications for the FEMB (there are currently none)
- For the 3-chip solution, all the interfaces (clocks, communication, data path) between COLDATA, COLDADC and LArASIC are to be fully specified and documented. It is recommended to review these specifications with all development teams prior to submission of these chips.

The ASIC specifications, for parameters such as “ENOB”, “SNR”, noise and others, must explicitly list the testing conditions, such as the loading capacitance and shaping time for the noise tests, the sampling frequency for the ENOB tests, and so on.

2. Do the chips and boards satisfy the requirements?

The available chips have still problems and there are missing test results to be sure the new generation of ASICs are fulfilling requirements.

Concerning the 3-chip solution, issues seem to be understood and simulation of the next version of designs are promising:

- LARASIC has identified solutions. Consider improving the ESD protection on the input pads.
- COLDADC issues also understood (with the exception of the large spread of power dissipation). The IR drop explanation for non-linearity requires a detailed analysis.

- COLDATA has very small bugs. PLL issue seems understood

CRYO is a less mature design (i.e. the design started only a year ago) and the first version of the CRYO ASIC has few issues (ADC speed, noise level to be understood, …) but fixes have been implemented in the second version (nEXO chip). Measurements of the nEXO chip should be used before going to next submission.

3. Have interfaces with other Cold Electronics detector components (e.g. WIB communications and data protocols, clock and power distribution, cabling and connectors) been addressed and documented? Are the electrical and mechanical interfaces with the APA fully defined and documented? Have lessons learned from ProtoDUNE been implemented?

Interface with APA was addressed in a previous review. WIB interface will be addressed in the next review in March.

4. Are the full specifications of the ASIC designs and complete documentations for ASIC users available in EDMS or DocDB? Is the standalone testing of the ASICs complete and are the results of these tests available in public documents in DocDB or EDMS? Are there test results that are not yet fully understood and require further work before the ASIC design team(s) can proceed to a further iteration of the design? Should the COLDATA and CRYO ASICs develop in-situ time delay measurements to the WIB?

The presented tests are satisfactory. However, there are still missing tests:

- ADC with higher frequency signal
- Overload for CRYO
- Test with APA for CRYO
- CRYO next submission after test with APA

We suggest that the testing results reported explicitly list the testing conditions which should be as closed as data taking conditions, such as the loading capacitance, the gain, the shaping time and the sampling frequency.

Missing documentation: schematics should be made available to the reviewers.

5. Do the standalone tests of the new generation of ASICs indicate that the design goals have been achieved? Do these design goals meet the detector requirements? Have all issues observed in previous versions of the ASICs been addressed? Do the performance measurements obtained from test stands meet the expected performance? Does the response of the ASICs match the expectations obtained from simulation? Specifically:

a. *For LArASIC: have the issues with the baseline shifts been addressed by the latest iteration of this chip? Initial operation of ProtoDUNE has indicated some problems with baseline restoration that in principle had been addressed in the version of the ASIC being used. Is the source of these problems understood?*
b. *For the new Cold ADC: are the issues with the autocalibration and with the kickback from the pipeline to the SHA understood and fixed? Are all the other problems with the first prototype understood and fixed? What yield has been observed in testing all the prototype ASICs? Is there any understanding of the different types of failures?*
c. *For COLDATA: are there any issues with the design of the first prototype of COLDATA? Are measurements of the bit error rate for cable lengths of 9 m and 23 m available, both at room*

temperature and in LN2? Is a data equalizer chip required on the receiving end (WIB)? Are all the synchronization issues between the timing system and COLDATA understood? What is the level of synchronization that can be achieved in a system using COLDATA?

d. *For CRYO: have all the issues identified in the first iteration of the design been fixed? Is there an understanding of the differences in noise level between simulation and test stand results? Are measurements of the bit error rate for cable lengths of 9 m and 23 m available, both at room temperature and in LN2? Is a data equalizer chip required on the receiving end (WIB)? Are all the synchronization issues between the timing system and CRYO understood? What is the level of synchronization that can be achieved in a system using CRYO?*

Concerning the 3-chip solution, issues seem to be understood and simulation of the next version of designs are promising:

- LARASIC has identified solutions. Consider improving the ESD protection on the input pads.
- COLDADC issues also understood (with the exception of the large spread of power dissipation. The IR drop explanation for non-linearity requires a detailed analysis)
- COLDATA has very small bugs. PLL issue seems understood

CRYO is a less mature design (i.e. the design started only a year ago) and the first version of the CRYO ASIC has few issues (ADC speed, noise level to be understood, …) but fixes have been implemented in the second version (nEXO chip). Measurements of the nEXO chip reading out an APA should be used before going to next submission.

6. Is there an understanding of the reasons why issues with the ASIC design uncovered during testing (if any) were not observed during the simulation of the ASIC prior to the submission? Are the design methodology and the simulations of the ASIC response appropriate or are there improvements that could be made to avoid such problems future revisions? Is the internal review mechanism prior to the submission of an ASIC sufficient to identify possible failure mechanisms and to fully verify that the ASIC design is meeting the specifications? Should there be an external review of the ASIC design prior to the submission of the next iteration?

There are plausible answers. The design methodologies and verification methodologies need to be clarified and improved as there were problems uncovered during the verification of almost all ASICs.

7. Is the appropriate documentation of the FEMB design(s), the corresponding Gerber files and bill of material available in EDMS?

There is documentation available.

The single board solution for the 3-chip option is not yet mature but worth to be looked at.

For CRYO the decision of going or not for a package chip has some implication which will have to be addressed before a decision in favor of CRYO can be made. It is noted there is a potential improvement in going from 64 to 32 channels: power spreading especially for packaged versions, reduction in "fan in" trace density (in addition to yield or parametric acceptance).

8. What is the status of fabrication for the various FEMB prototypes and what is the timeline for standalone tests of the FEMBs and later for system tests?

A reasonable plan has been presented. It is recommended to order the LDOs as soon as possible.

9. What are the plans and the timeline for the next iteration of the design of the ASICs and FEMBs? Have sufficient resources been put in place to meet the submissions deadlines? Are there lessons learned from the previous design iteration of the ASICs on the management of distributed design teams? Are processes in place to ensure that the next ASIC submissions will not encounter the delays observed for the first submissions? Are plans for required technical resources consistent with scope of remaining work?

We do not see major problems with the next submissions schedules but we do insist on the need for revisiting the verification methodologies. Concerning the resources, we do not see major issues but very little information was presented making it difficult to judge.

10. What are the timeline and plans for obtaining results from system tests and from components lifetime tests on the current generation of ASICs and FEMBs? How will the results from these tests influence the decision on the submission of the next set of prototypes? What are the plans for testing to verify that the new ASICs/FEMBs will not cause additional system noise beyond that seen in ProtoDUNE?

It was announced prior to the review that the lifetime tests are not yet finished. We encourage the teams for pursuing the tests as quickly as possible. The measures taken at the design level (lower Vdd, long channels) are sensible and have shown to be effective on previous versions. However, we believe the lot to lot variations should be evaluated.

The measures taken for the FEMB designs are also deemed good.

The presented plans for next system tests with new boards and new ASICs are aggressive but clearly well understood by the team. We do not see major problems if there is a delay of a couple of months to allow the groups to measure and implement changes suggested by observation of the new ASICs and FEMB's prior to near final submissions.

11. What is the progress with the development of criteria for the selection of an ASIC solution for DUNE? What is the progress with the reliability committee and how will the results from this committee influence the ASIC selection process? Have the design rules for long lifetime in the cold been satisfied?

Question removed.

12. Are there any issues with the design that will complicate the procurement strategy and manufacturing plans for the ASICs and the FEMBs? Does the design lead to complications in the development of the quality assurance program and what kind of tests / vendor qualifications are required before finalizing the design of these components?

For the CRYO, the question of packaging has important implications for QC, possible stress, board design and boiling. We do not see that as a show stopper.

For the 3-chip solution, the necessity of testing the chips warm and cold prior to put them on board has clear work load implications but it is accounted for in the plan.