DUNE Preliminary Design Review of ASICs and Front-End Motherboards FEMB Plans (and other topics)

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Outline

- Lifetime and system tests
- Timeline and issues for DUNE production
- Address QC concerns
- Interface questions

System tests (i)

Q: What are the timeline and plans for obtaining results from system tests and from components lifetime tests on the current generation of ASICs and FEMBs? How will the results from these tests influence the decision on the submission of the next set of prototypes? What are the plans for testing to verify that the new ASICs/FEMBs will not cause additional system noise beyond that seen in ProtoDUNE?

A: Original plan foresaw that we would

Complete all system tests prior to submission of 2nd round of prototypes, perform lifetime measurements on all prototypes prior to 2nd round submission

Lifetime measurements (i)

We have a reliability committee (G. Varner, G. Broojimans, H. Chen, T. Shaw) that agrees with our basic approach, but has not delivered its final report

- Design ASICs to operate at lower voltage compared to standard of technology used for the design
- Use larger channel sizes
- Both contribute to reducing hot-carrier effect
- Still important to demonstrate with accelerated lifetime tests that ASICs will have very long lifetime in LAr
  - Done for previous version of LArASIC
  - Done for Analog Devices AD7274 (COTS single channel ADC used for SBND)

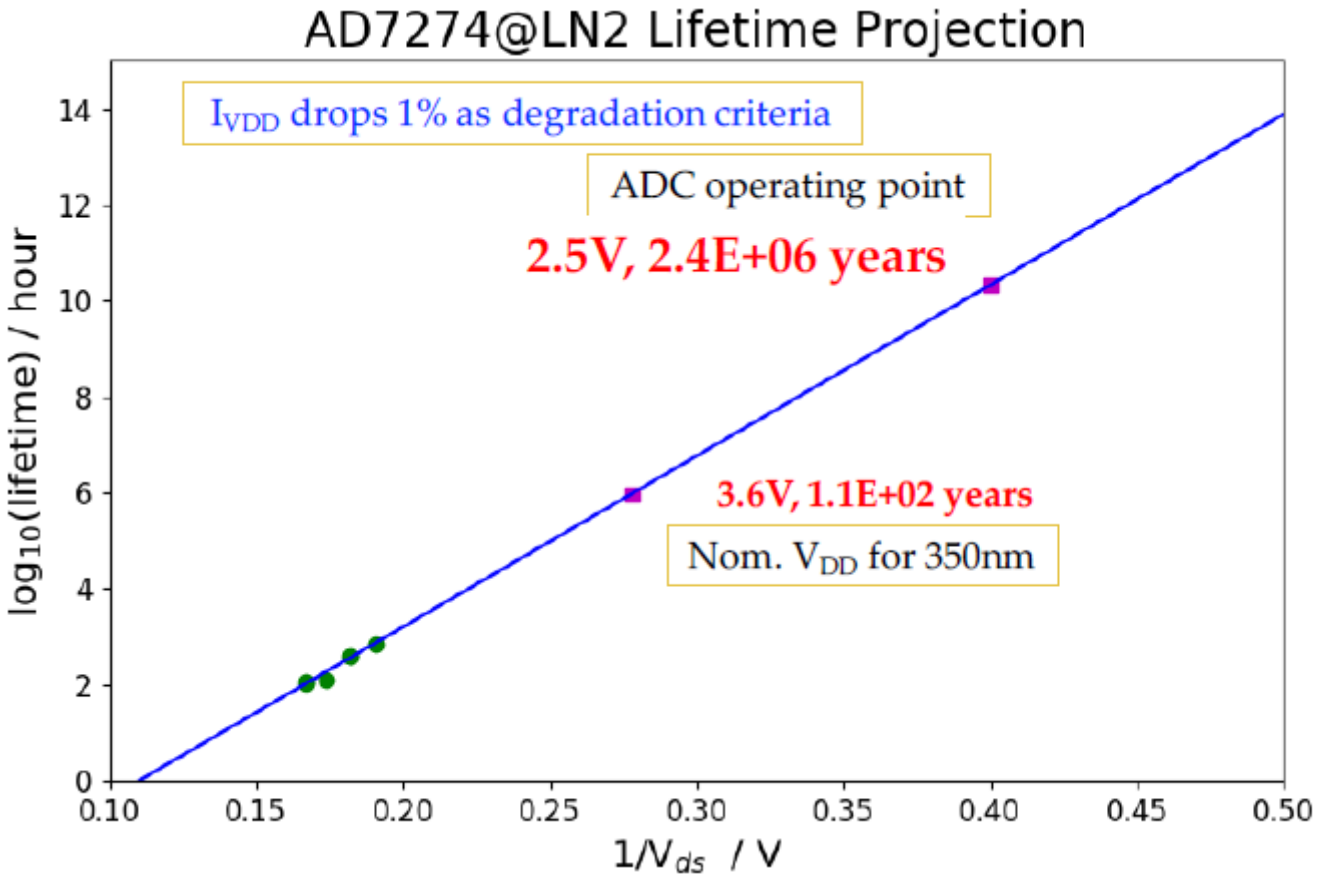
Lifetime measurements (ii)

How to perform lifetime measurements

Example (AD 7274, 350 nm)

- target operating voltage 2.5 V (technology designed for 3.6 V)
- Measure ASIC properties at the target operating voltage
- Operate for N hours at V_{ds}>2.5 V
- Go back for a few minutes to check again ASIC properties
- If no change, go back to V_{ds}> 2.5, operate for N hours
- Repeat until significant change of properties observed
- Record total time at given V_{ds} > 2.5 V prior to change
- Repeat with new ASICs for other reference voltages V_{ds}

Lifetime measurements (iii)



Lifetime measurements (iv)

ColdADC: already operated at voltage > design target, could not really use it to measure lifetime

CRYO: first prototype did not meet all specifications

Will start prepare test stands for performing these measurements when 2nd round of prototypes become available

Tricky part is identifying the property of the ASIC to be monitored to decide that the performance has degraded considerably

- In the case of AD 7274 this decision was based on a change of the current drawn by V_{ds}

CRYO is a special case, need to bypass LDOs, test them separately

Results from these tests will not be available prior to next submission, will be considered at the time of FDR

Interference in larger systems

Kurtis, Jack, Shanshan have discussed standalone tests of FEMBs

The next step is to mount FEMBs on APAs and check for noise induced by other systems

We have three such setups

- 40% LBNE APA prototype at BNL (can house 8 FEMBs)
- ProtoDUNE APA (and later DUNE prototype APAs) in the cold box at CERN (20 FEMBs)
- Small TPC in the ICEBERG cryostat at Fermilab (10 FEMBs, but APA size is 1/10th of DUNE)

Will have 2nd run of ProtoDUNE with final prototypes of all detector components (installation in 2nd half of 2021)

Pros/Cons of various systems

- 40% LBNE APA prototype at BNL
  - Filled with LN2, not a TPC, no drift, only TPC electronics
- ProtoDUNE APA (and later DUNE prototype APAs) in the cold box at CERN (20 FEMBs)
  - Full size APA, tests in cold gaseous N2, not a TPC, no drift, can have photon detector (not with ProtoDUNE APA), can have other electronics in the cold box (some cryo instrumentation)
- Small TPC in the ICEBERG cryostat at Fermilab (10 FEMBs, but APA size is 1/10th of DUNE)
  - Small size APA, real TPC (drift distance 30 cm on both sides of APA), has photon detector, room for additional electronics in the cold box (cryo instrumentation)
- ProtoDUNE Run 2
  - Unless major problems are observed, tried to avoid any design changes

Status of system test stands (i)

- 40% LBNE APA prototype at BNL
  - Operational (tests of first prototype FEMB with ColdADC and 2 FPGAs ongoing)
- Prototype APAs in cold box at CERN
  - Commissioned with 7th ProtoDUNE APA (no photon detector) in October using ProtoDUNE FEMBs
  - Will test SBND FEMBs in March
  - Move on with FEMBs with ColdADC+FPGA, CRYO, ColdADC+COLDATA as these (and the new WIB) become available
  - Will perform tests for interference with new RTDs that will be mounted on DUNE APAs
  - Replace with first prototype DUNE APA in the Fall

Status of system test stands (ii)

- Small TPC in ICEBERG at Fermilab
  - System was built to allow for fast turnaround and actual testing with cosmic rays
  - Commissioning has been plagued by multiple issues with both the cryostat and the TPC (discharges, damaging electronics)
  - Turning on this week using ProtoDUNE FEMBs
  - If no problem will move on to test next set of FEMBs
  - Turnaround for testing new set of FEMBs can be as low as 2-3 weeks
- With all the systems operational we can test two sets of FEMBs within 6 weeks even if they become available at the same time

Bottlenecks in FEMB testing

- Number of FEMBs available
  - This is an issue for LArASIC/ColdADC/COLDATA solution
    - For 20 FEMBs need 160 good LArASIC/ColdADC, get 240/200 respectively in MPW runs
  - Not an issue for CRYO (need 40 ASICs for 20 FEMB, typical MPW run is 100 ASICs)
    - Also not an issue for COLDATA
- New Warm Interface Board required for system tests
  - Two hardware prototype exist (all functionality verified), need to port firmware from ProtoDUNE WIB (Altera) to new WIB (Xilinx)
  - Hope to get this done in the Spring

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Production plans and design

Question 12: Are there any issues with the design that will complicate the procurement strategy and manufacturing plans for the ASICs and the FEMBs? Does the design lead to complications in the development of the quality assurance program and what kind of tests / vendor qualifications are required before finalizing the design of these components?

ASIC production (i)

Three ASIC solution

- LArASIC (180 nm technology), 24k ASICs required per detector, assume + 2 spare APAs, 300 spare FEMBs, assume 86% yield for ASICs (90% from dicing & packaging, 95% from LN_2 testing)
  - Require 26.7k chips per detector, i.e. 46 wafers (assume 700 chips per wafer)
  - Order 2 batches of 25 wafers, allow for minimum yield (no reordering of wafers) of 76%
- ColdADC and COLDATA (65 nm technology), require 4:1 ratio
  - Require 26.7k ColdADC and 6.7k COLDATA
  - Ideally place 4 ColdADC and 1 COLDATA in the 65 nm reticle

ColdADC / COLDATA reticle

Original ColdADC size: 6.86 mm x 7.61 mm,

COLDATA: 7.73 mm x 7.73 mm

We have decided to align the scribe lines and increase the size of ColdADC vertically to 7.73 mm to simplify dicing

Horizontally we can fit ratio 3:1 of ColdADC to COLDATA in a 65 nm reticle

Going to the desired ratio 4:1 would require that we reduce the horizontal size of ColdADC to ~5.8-5.9 mm

While there are several redundant parts in ColdADC, we have decided against trying to remove some of them and reduce the size of the chip

ASIC production (ii)

With 3:1 ColdADC/COLDATA ratio we can accommodate ~745 ColdADC and ~245 COLDATA per 12” wafer

We would need 42 wafers per detector, assume order 2 batches of 25 wafers

The minimum yield we can live with (no reordering of wafers) is 72% for ColdADC, 55% for COLDATA

For CRYO we expect to have 220 chips per wafer

We would need 36 wafers per detector, assume order 2 batches of 25 wafers

The minimum yield for CRYO is 61%

In general if yields are high we could save on the last batch of wafers for the second detector

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Production and quality control (i)

- The QC process is driven by how many chips we have on a FEMB
  - 3 ASIC solution: 18 custom ASICs (plus LDOs, oscillator)
  - CRYO solution: 2 custom ASICs
- All FEMBs are going to be tested in LN_2 prior to shipment to SURF (South Dakota) and tested again (warm) just prior to installation on the APAs
  - With 18 custom ASIC a failure rate of 1% means that 1 FEMB out of 6 requires rework
  - Need to test every ASIC in LN_2 (see also Shanshan's presentation)
  - Even if we have probably identified and fixed the main cause of poor LArASIC yield in LN_2, we are not going to be able to test now a sufficient number of ASICs to decide to skip cold testing (if we do both warm and cold testing, we could decide to skip cold testing after accumulating sufficient statistics)

Production and quality control (ii)

- For CRYO we could decide to skip LN_2 testing on the chip (or do it only warm, and at the wafer level at warm)
  - Warm testing at the wafer level will also be only possibility for individual chip QC if we are installing bare chips on the FEMB

- Final QC plan (wafer probing ? Test packaged chips at warm or in LN_2) will depend on ASIC choice, and may be changed after sufficient statistics is accumulated
  - For the moment the following assumptions are made
    - Package all ASICs
    - Qualify all ASICs in LN_2 prior to installation on the FEMBs
    - Test all FEMBs in LN_2

Production and quality control (iii)

- We have not observed any other specific problems that are observed only at LN_2 temperature that would require design fixes apart from the LArASIC issue with the BGR startup
- We think that there isn't anything specific to the design (after changing the dimension of ColdADC) that could result in any problem with the QC process (or with populating the FEMBs)

Quality control plans (i)

- The details of the QC testing are relatively well known for LArASIC
  - BNL group has tested several thousand chips for ProtoDUNE and SBND
  - Final testing process and final selection criteria will be refined after we get the next round of prototypes
- Cheng Ju has discussed the tests done on tens of ColdADC ASICs
  - This will form the basis for the QC procedures that will be fully developed after testing the second prototype
- Testing of COLDATA and CRYO so far has been limited to a few prototype chips
  - Need to develop protocol for bulk testing of chips

Quality control plans (ii)

- Parts database: unique ID that can be printed as bar or QR code on stickers, but cannot add stickers to ASICs/FEMBs
- Packaged chips will have serial number on the packaging, will have unique match in parts database
  - COLDATA chips will also have internal hardware identifier (E-fuses) that will be defined in one of the first steps of the QC process
  - Will consider having E-fuses also on CRYO (again with unique match in the parts database)
- Will put serial number of the printed circuit board for the FEMBs, and again have unique match between serial number and unique ID in parts database

Quality control plans (iii)

- All testing results (ASICs/FEMBs) will be stored in the hardware database with a key provided by the unique ID in the parts database
- For ProtoDUNE we used a custom database that was transferred into the Fermilab DB only after the beginning of data taking
- For DUNE we are actively participating in the design of the hardware DB and plan to use that exclusively to store the results of testing
  - Selection of ASICs to be used for populating FEMBs will be done based on the data stored in the hardware DB

Test stands for QC

- LArASIC chips being tested with single/quad board (see Shanshan's presentation)
- ColdADC: 3 different setups for testing (see ChengJu's presentation)
- COLDATA: tested with National Instruments setup connected to test board with 4 ColdADC
- CRYO: test stand compatible with previous setups at SLAC

Test stands for QC - future

- Assume that ASICs are packaged
- Need to test multiple ASICs in LN_2 within 1.5 hours cycle
- Multiple test stands in different institutions, using same setup and procedures, plan for cross-calibration using same set of chips
- Robotic system for placing ASICs in sockets on test boards (recognized to be one of the largest source of errors in testing)
- Using cryogenic test system (CTS) developed at Michigan State University to minimize condensation / freezing on chips / sockets / boards when immersing (extracting) boards in (from) LN_2 (another big source of issues, including damage to chips / sockets)

Test stands for QC – future (i)

- Test boards will be very similar to FEMBs, readout via warm interface board and FELIX card (required for parallel testing of multiple boards)
- Test board for LArASIC
  - Need extra input for signal from external high precision DAC
  - Use either ColdADC + COLDATA for digitization / serialization
  - Sockets for 4 or 8 LArASIC chips (socket will be on daughtercard to allow for socket's replacement if needed)
- Test board for ColdADC
  - Need extra input for signal from external high precision DAC
  - Signal goes to LArASIC and then is digitized from ColdADC
  - Serialization with COLDATA chips
  - Sockets for 4 or 8 ColdADC chips (sockets on daughtercards)

Test stands for QC – future (ii)

- Test board for COLDATA:
  - In both case 2 COLDATA chips will be on sockets mounted on daughtercards
  - FEMB-like board with additional FPGA to allow configuring each COLDATA alternatively as master and slave for clock, fast commands, I2C
  - Extra links to configure the additional FPGA
  - Can use either WIB backend, or use simple boards with FPGA+chip on a socket
  - WIB backend will need some additional firmware

Test stands for QC – future (iii)

- Test board for CRYO
  - Wafer probing if chips are mounted directly on FEMB ?
    - Most probably system will be evolution of current SLAC setup
  - FEMB style test board if chips are packaged, with additional input(s) for external high precision DAC
    - Backend via warm interface board

- Timeline for test boards
  - Current systems are OK (with minor modifications) for testing chips from MPW runs (limited number of chips)
  - Need to have more complex systems if we need to test more than few hundred chips for ProtoDUNE run 2 – Spring 2021

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Interfaces (i)

- Have interfaces with other Cold Electronics detector components (e.g. WIB communications and data protocols, clock and power distribution, cabling and connectors) been addressed and documented?
  - Interfaces with the APA (mechanical / electrical) have already been addressed in the PDR of February 2019, no changes in that part
  - Interfaces between the FEMBs and the WIBs are still being worked on
    - Exact power distribution scheme depends on the ASIC choice (and we should do more testing to decide which is the optimal scheme from the point of view of electronics noise and ohmic losses in the cables)
    - Data protocols for COLDATA and CRYO are defined
    - Cables and connectors are defined, we may just change number of connections to ensure overall reduction of 10% needed to fit cables in the conduit in the side tube of the APA frame
- Would like to defer detailed discussion of WIB/FEMB interface to the next review (10/11 March)

Backup Material

- None for the moment