Simulated FE output noise when injecting wide-band noise at power supply:
-900mV BL, DC coupling (blue)
-200mV BL, DC coupling (purple)
-200mV BL, AC coupling (yellow)
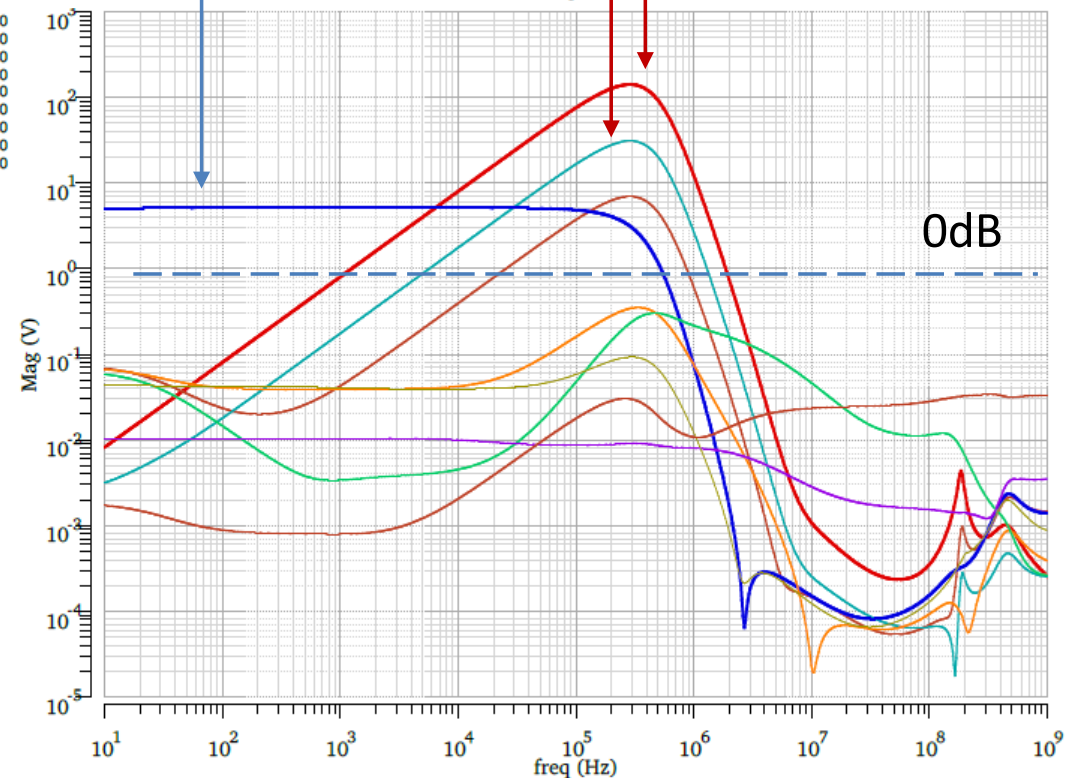
Simulated FE output noise when injecting wide-band noise at power supply of _each FE block_:
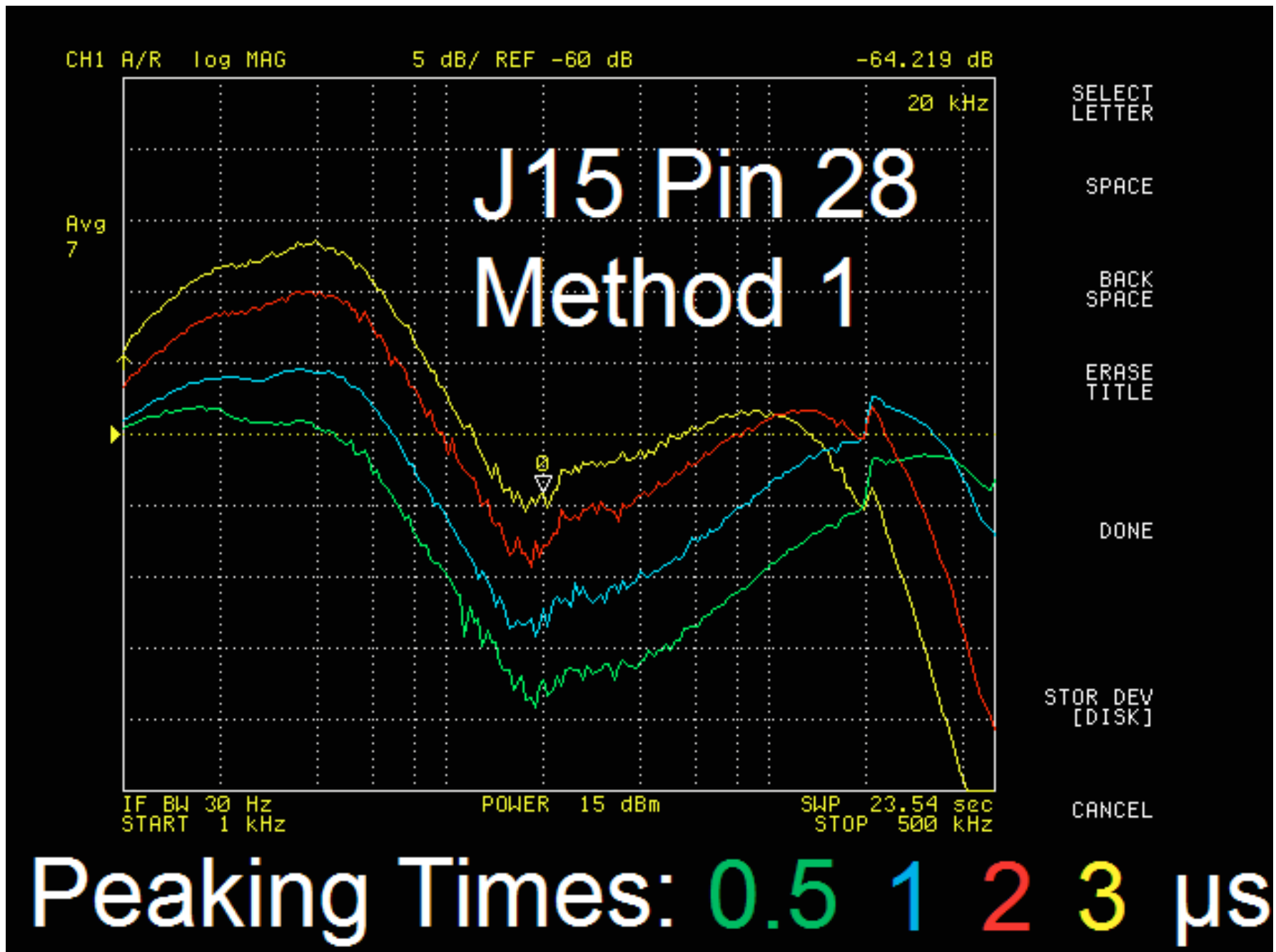-VDDP (CA1 input PMOS only, red)
-VDDA of CA1 (w/o CA1 input PMOS, brown)
-VDDA of CA2 (w/ CA2 input PMOS, turquoise)
-VDDA of SH1 at 200 mV BL (blue)
-VDDA of SH1 at 900 mV BL (yellow)
-VDDA of SH2 (orange)
-VDDA of SH3 (green)
-VDDA of dc/ac coupling (purple)
--VDDA of buffer (brown #2)
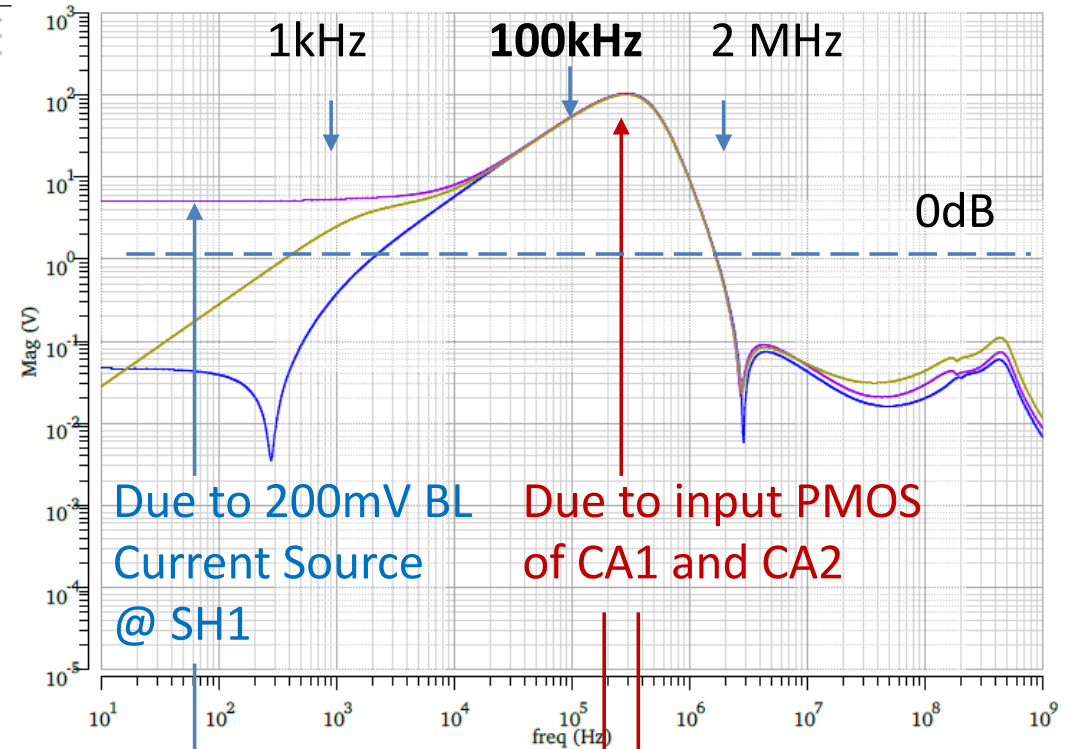
PSRR Measurement of MicroBooNE Cold Mother Board with Voltage Regulator, better than -45dB

FE ASIC Configuration

- FE ASIC configuration is coming through COLDATA with SPI interface
- As presented in Dave's COLDATA talk yesterday
  - Every SPI sequence for a LArASIC is issued twice & the pattern read back (the second time) is compared to the pattern sent
  - An error bit is set in one of the status registers if the two differ
- The configuration of FE ASIC doesn't go through ColdADC, which uses I2C interface