

DUNE Preliminary Design Review of ASICs and Front-End Motherboards ASIC schedule and ProtoDUNE Run 2

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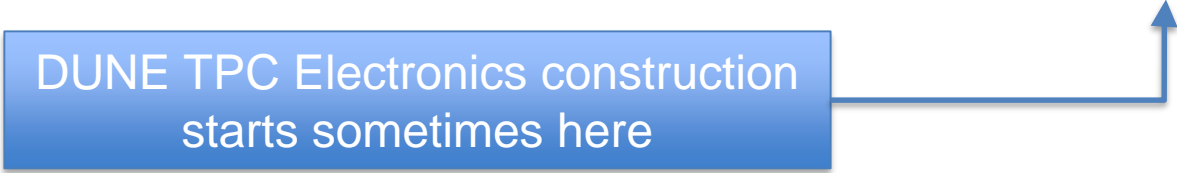
Fermilab

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The question

- Is the ASIC development schedule compatible with the desire of using final FEMB prototypes in the 2nd run of ProtoDUNE ?
- CERN SPSC has recently approved a 2nd run of ProtoDUNE
- We will start emptying the ProtoDUNE SP this year, then reopen the technical cryostat aperture (TCO), and remove the current set of APAs (six)
- In the 2nd half of 2021 we will have four DUNE APAs at CERN
- Install FEMBs on the APAs, perform final check in the cold box, and then move them into the cryostat
- Close the TCO, refill the cryostat, take cosmics and beam data

DUNE TPC Electronics construction starts sometimes here



Is this feasible ?

(i)

For ProtoDUNE run 2 we are planning for 80 FEMBs

- For 3 ASIC solution need 800-1000 LArASIC and ColdADC, 250 COLDATA (640 needed for the FEMBs plus yields)
- For CRYO solution need 250 CRYO chips (160 yields)

These numbers depend on yields in ASIC fabrication & QC testing, populating FEMBs, QC on FEMBs

For the CRYO solution we most probably can get all the ASICs in a MPW run

For the 3 ASIC solution we most probably need to make an engineering run to be 100% sure that all the required ASICs are available for the 2nd run of ProtoDUNE

The timeline

Assume that by June 2020 we complete the submission of the 2nd prototype of all ASICs

Receive chips from MPW run at the end of September

Start testing and packaging at the same time

Have FEMBs populated and tested by the end of the year

Measurements and selection of ASICs for DUNE complete by February

Fabrication and packaging of ASICs completed by July

Chip testing in August, FEMB population and testing in September / October

APA integration in November 2021

Is this feasible ?

(ii)

This timeline allows for no delay between now and December 2021

Any delay will impact readiness of ProtoDUNE for data taking at the end of the accelerator shutdown between 2021 and 2022

Ways to increase float

- Try to anticipate submissions (discussed by Dave Christian)
- Order all ASICs at the time of the submission of the prototype for the MPW run (unclear that we can really get that many ASICs)
- Go straight to engineering run (expensive, risky)
- Share engineering run with other ASIC submissions using similar design (could even accept 1-2 months delay)

Conclusions

Getting ready in time for ProtoDUNE run 2 without causing delays (TPC electronics is on the critical path) is not easy

Will investigate all the possibilities to get this result (very large number of ASICs in MPW run or early engineering run)

Most important is getting the design for the next submission right

- Any design mistake that requires additional investigation / fixes will likely result in a delay of > 6 months
- If we do not go for an early engineering run we could correct minor mistakes when making the masks for an engineering run