ProtoDUNE-SP FEMB

Research, Development, Production, Installation and Commissioning

Shanshan Gao on behalf of the CE group

Brookhaven National Laboratory

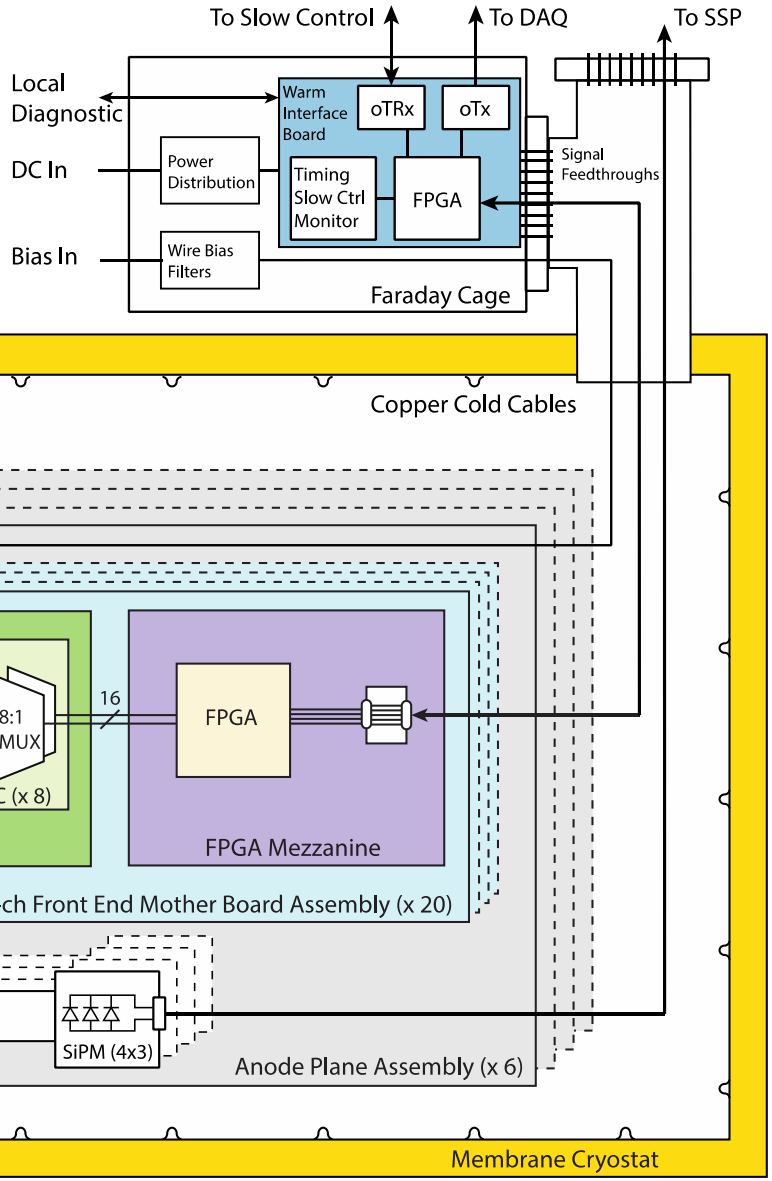
02/06/2020

Outline

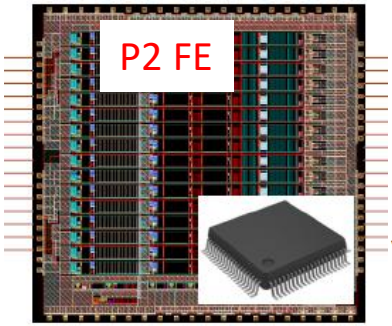
- ProtoDUNE-SP TPC Readout Electronics
- Integral System Design Concept
- QC Procedure for FEMB Production
  - QC Plan and Procedure
  - QC Test Stands
  - QC Tests for Components
  - QC Tests for FEMB Assembly
  - FEMB Installation Failure at CERN
- ProtoDUNE-SP CE Status in Detector Operation
- Summary

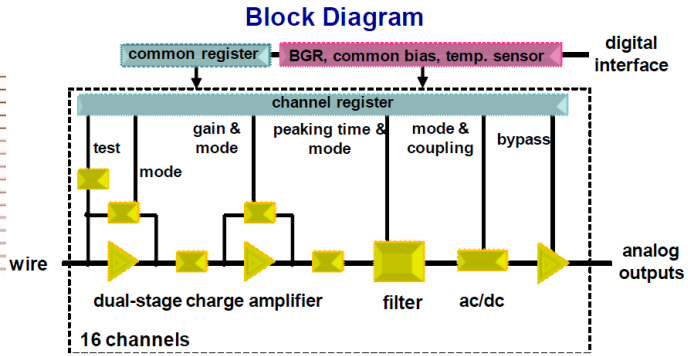
ProtoDUNE-SP TPC Readout Electronics

- Front End Electronics System
  - 960 FE ASICs/960 ADC ASICs/120 Cold FPGAs
  - 120 Front End Mother Board assemblies
  - 6 sets of cold cable bundles, 6 sets of signal feed-throughs
  - ~36 boards in warm interface electronics crates

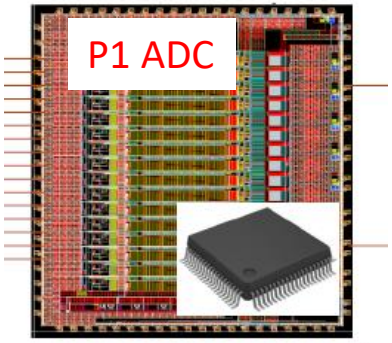


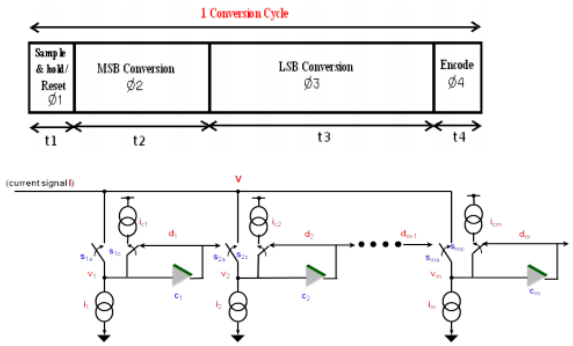
Key CMOS Devices of CE





16 channels, programmable
Charge amplifier
Adjustable gain: 4.7, 7.8, 14, 25mV/fC
Adjustable filter time constant
Designed for 77K-300K operation
Designed for long lifetime
Tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES





16 channels, programmable
12-bit ADC at 2MS/s sampling rate
Current-mode domino architecture
Designed for 77-300K operation
Tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES
Low resolution due to stuck codes
Development discontinued after ProtoDUNE-SP

FPGA (COTS)

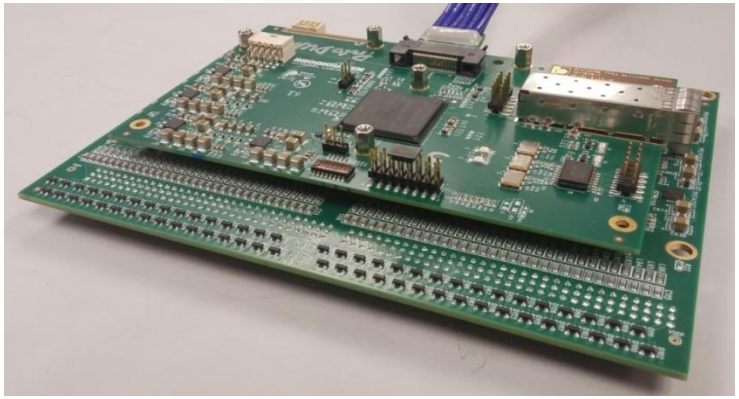
Voltage Regulator (COTS)
(< 100mV dropout)

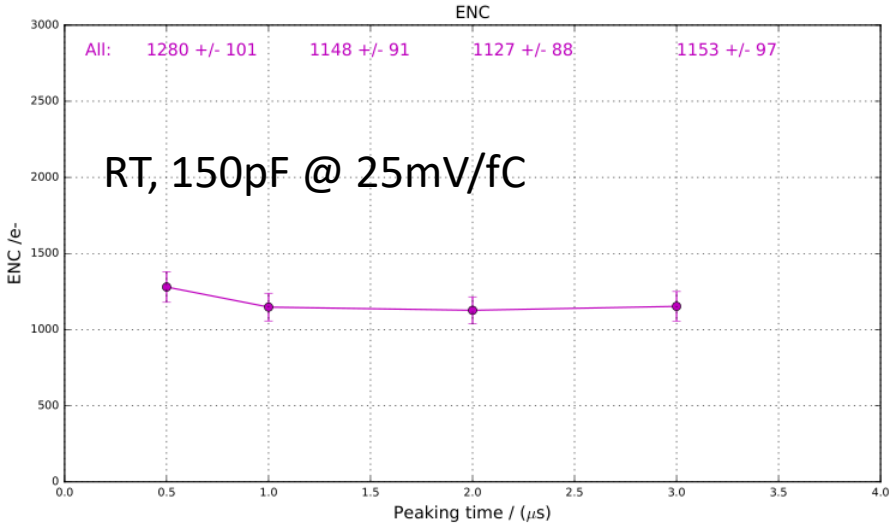
Commercial FPGA and regulator study

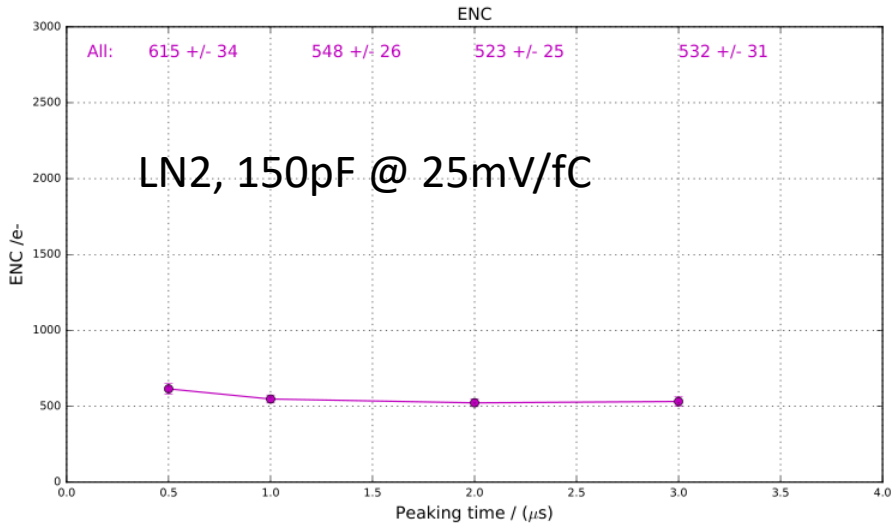
1. Screening various commercial devices to find survivors at LN2 temperature (77K)
2. Lifetime study
   - → Hot Carrier Effect is the dominant degradation at cryogenic temperature
   - → Extreme environment to accelerate the degradation process

Front End Mother Board (FEMB) Assembly

- 128 channels of digitized TPC wire readout
  - Analog Mother Board
    - 8 FE ASICs and 8 ADC ASICs
  - FPGA Mezzanine
    - Multiplexing and readout of digitized detector signals
    - 4x1Gb/s serial links to transmit 128 FE channels of data



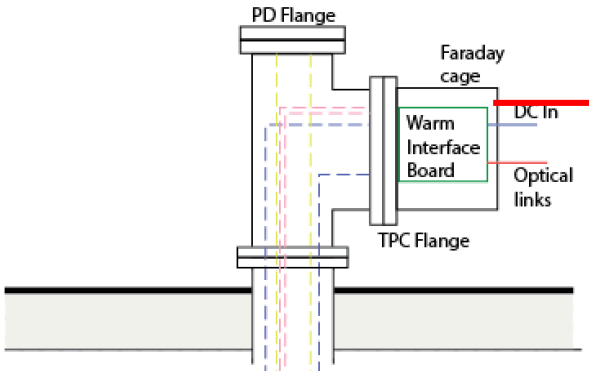


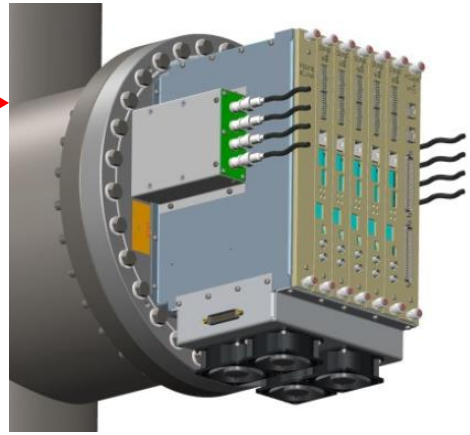


~1150e$^-$ at RT and ~550e$^-$ at LN2 @ 1us peaking time, 25mV/fC gain and 150pF C_d

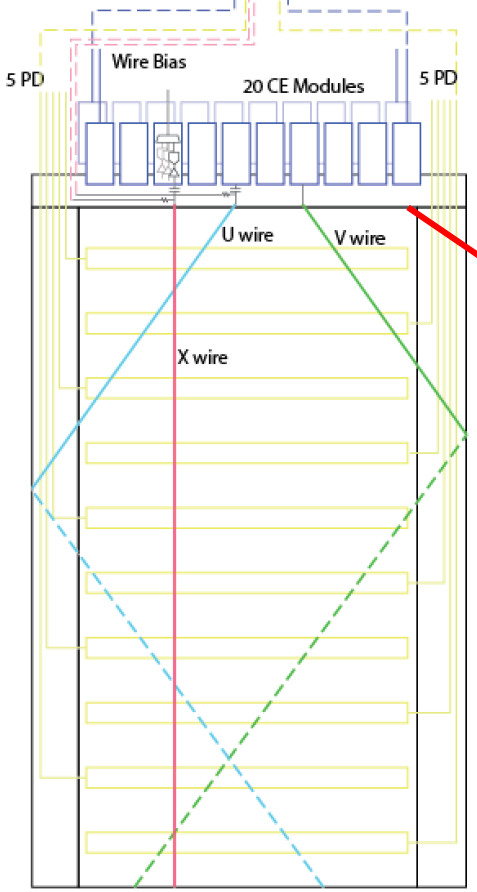
Noise decreases significantly at cryogenic temperature

Integral System Design Concept

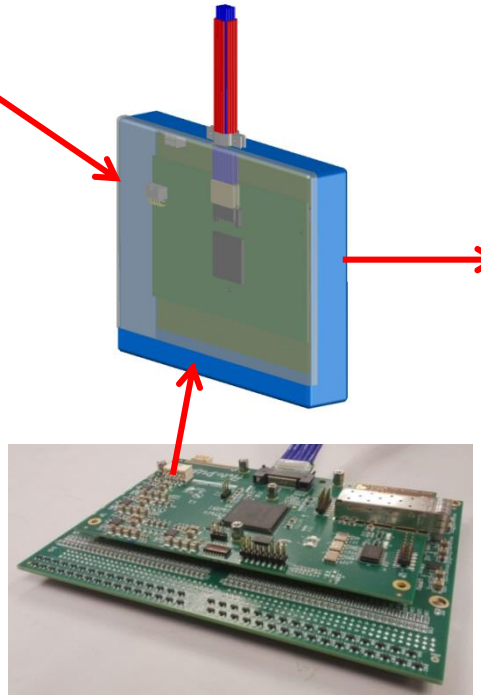


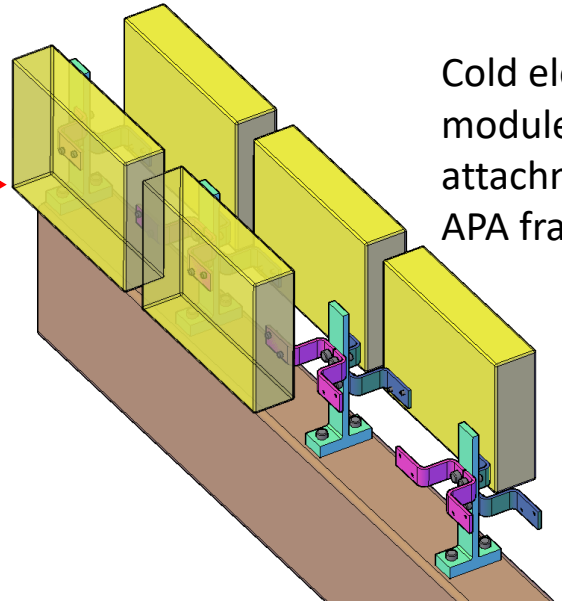


A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed



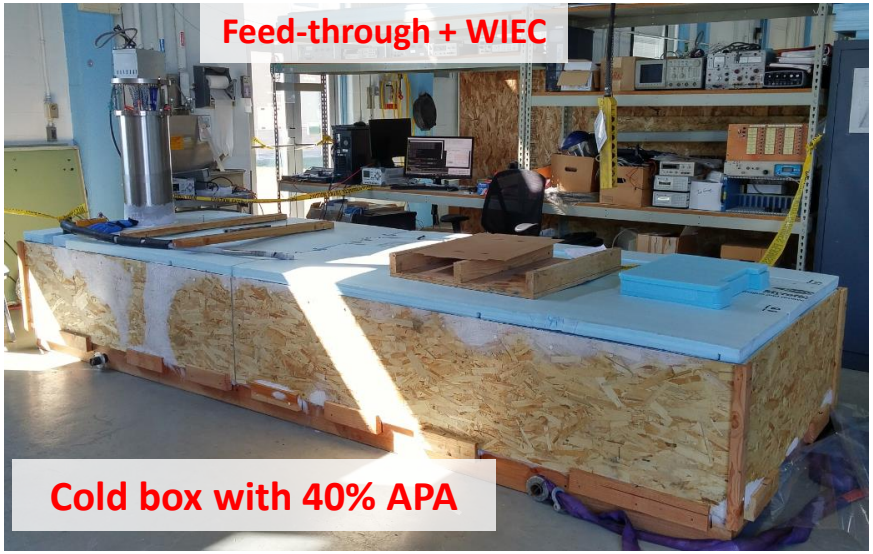
ProtoDUNE-SP



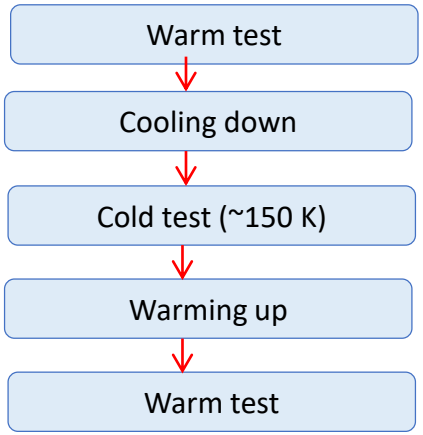


Cold electronics module and its attachment to the APA frame

Integration Test Stands at BNL and CERN

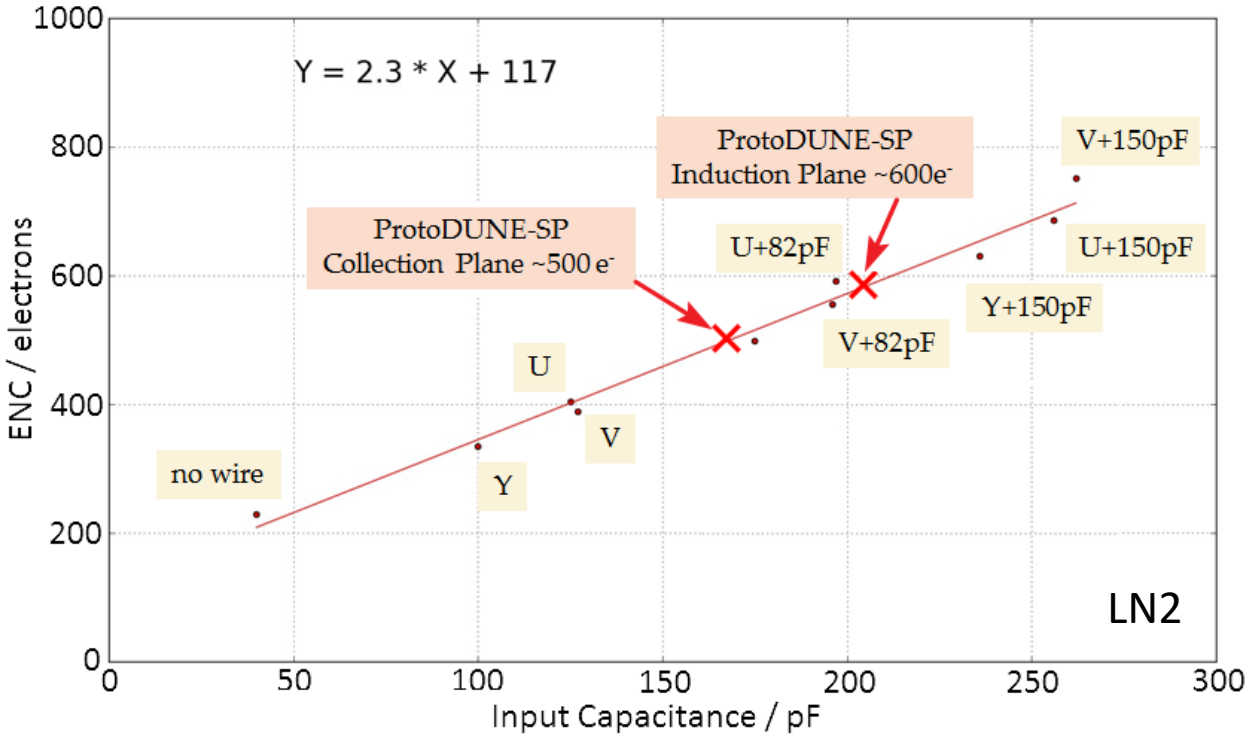


40% APA: 2.8m x 1.0m, 1024 wires



DUNE APA: 6m x 2.3m, 2560 wires

ENC Projection Based on 40% APA



- 40% APA
  - U/V wire: 4.0 m
  - Y wire: 2.8m

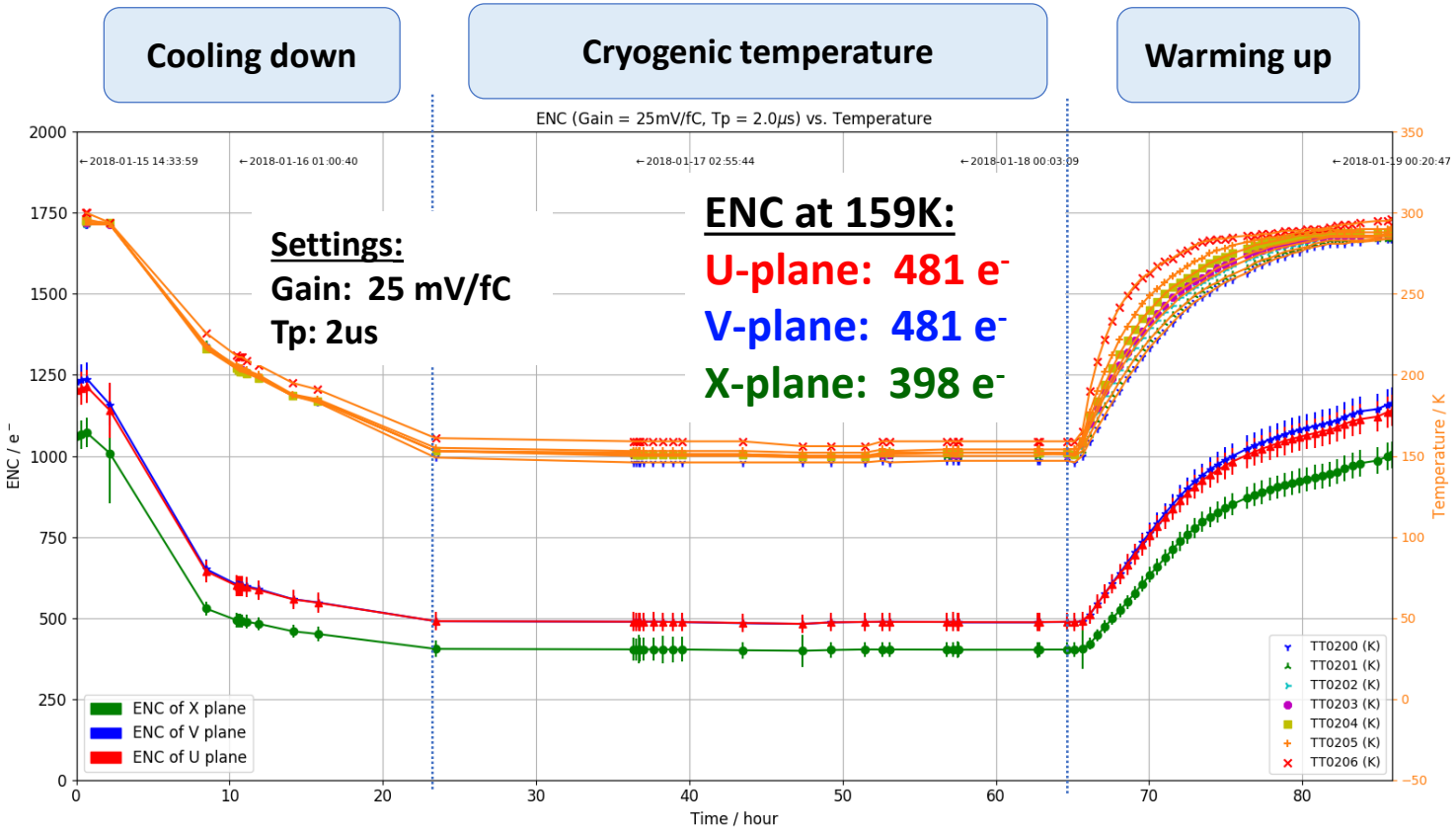
Note: 82pF and 150pF mica capacitors are added on some wires

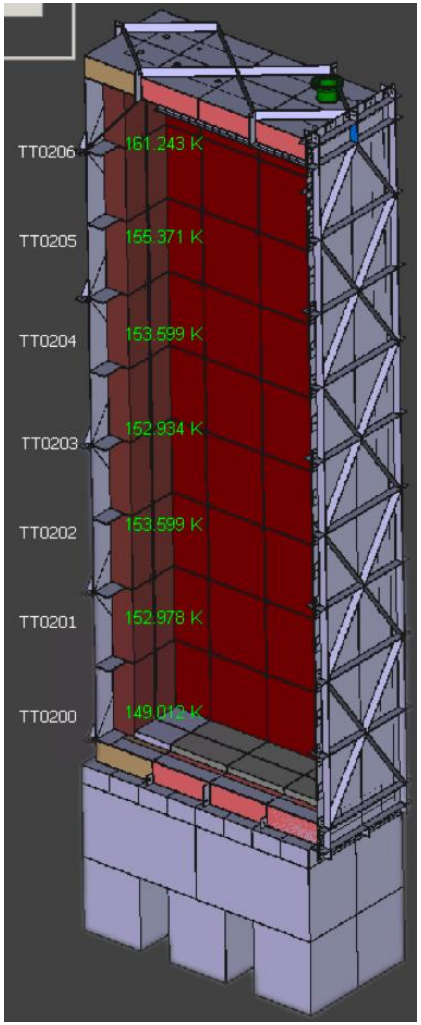
- ProtoDUNE APA
  - U/V wire: 7.39m
  - Y wire: 6.0m

- DUNE Far Detector
  - Same APA as ProtoDUNE-SP
  - Threshold: 1,000 e^-
  - Goal: as low as possible

CERN Cold Box Integration Test

APA2 (2018-01) Cold nitrogen gas with lowest temperature reached ~ 159K



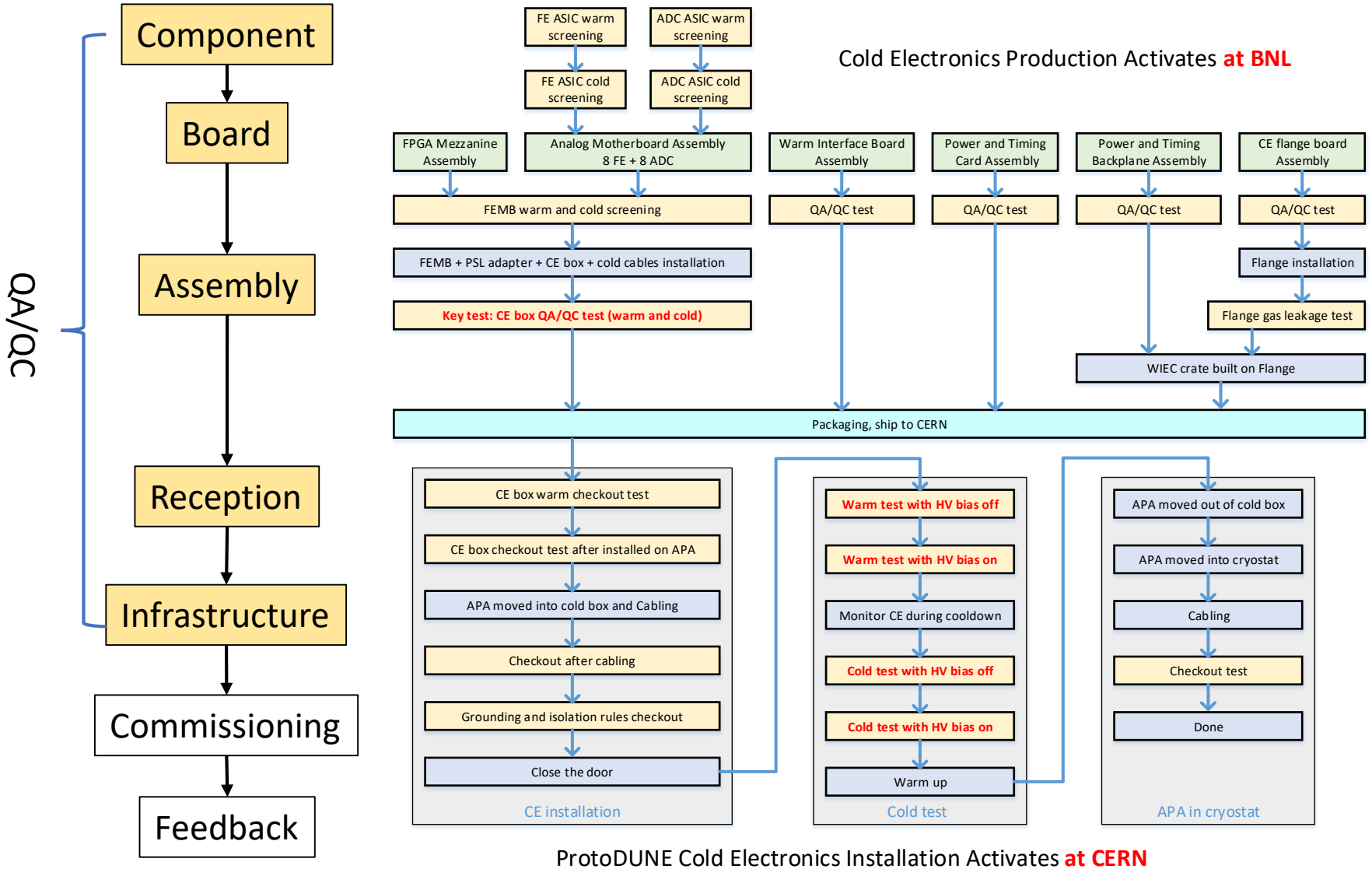


1. Uniform gain (77 e-/bin) is applied for calculating noise of all channels
2. HV Bias voltages were off
3. Data are read out chip by chip over local diagnostic GbE port.

QC Procedure for FEMB Production

- A comprehensive set of QA/QC tests carried out for all components to ensure reliable operation of FEMB in the ProtoDUNE-SP detector
  - FE & ADC ASIC screening test
    - Characterization both at room temperature and liquid nitrogen temperature
      - FE: baseline, noise, gain, linearity, peaking time, power consumption
      - ADC: DNL, INL, range, power consumption
  - Oscillator cold screening test
  - EPCS serial configuration memory cold screening test
    - Chip to configurate Altera FPGA, not needed for DUNE
  - FEMB QA/QC procedures
    - Post-assembly screening test before installation in CE box
      - Get rid of defective FEMB assemblies
    - Characterization both at RT and LN2 after assembly
      - A whole assembly includes FEMB, CE box, cold power cable and data cable

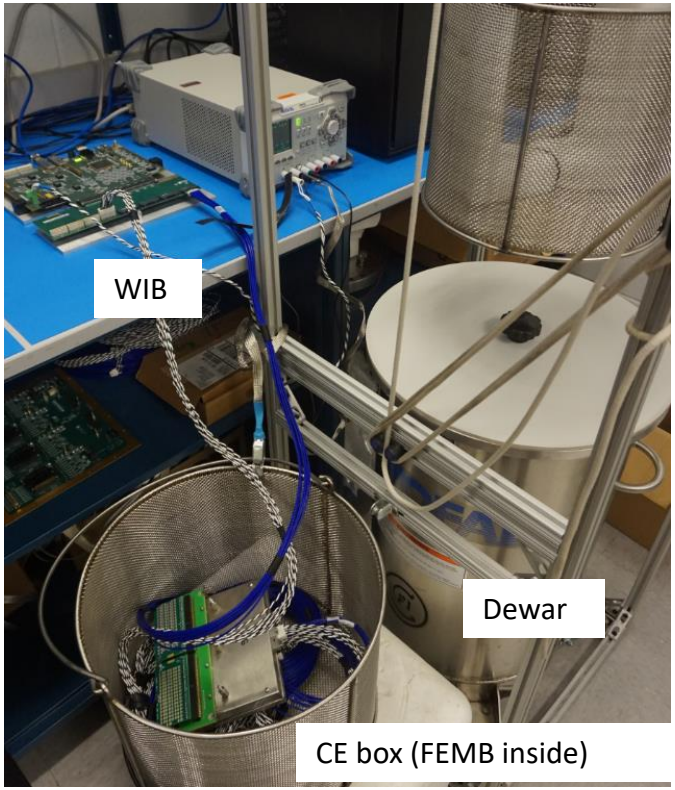
Procedure for CE Production and Installation



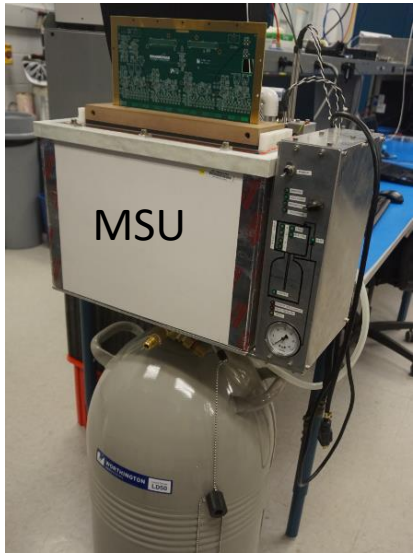
Test Stands for QC

Quad Socket FE Test Setup (RT)

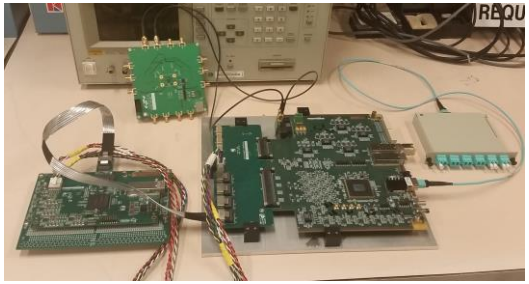
Quad Socket ADC Test Setup (RT)



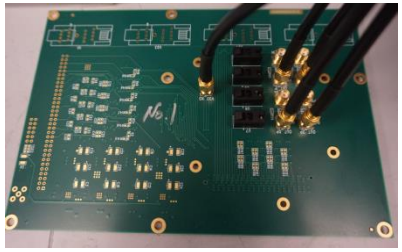
FEMB Test Setup (RT & LN2)



Cryogenic Test System



WIB Functionality Check



XO Cold Test Board

EPCS Cold Screening Test Board

P2 FE ASIC QC for ProtoDUNE-SP

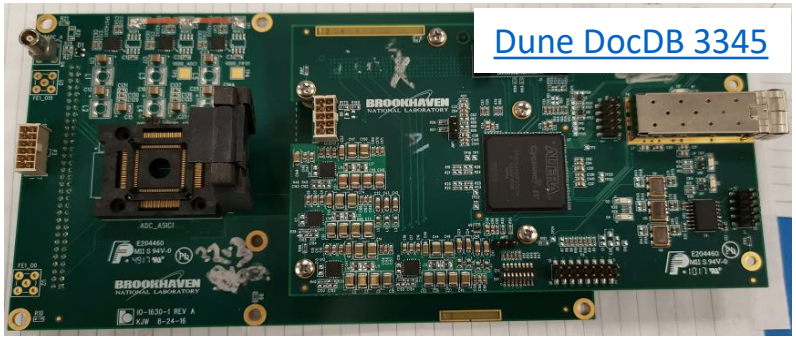
- FE ASIC chips for APA1 to APA5 passed QC test at RT
  - Criteria for passing: selection cuts for uniform FE response
    - Combine results over many ASIC test cycles for each channel to get expected pedestal, gain and ENC distributions
    - Reject ASICs with any of those values >5 sigma from channel expected response
  - 1,850 chips tested at warm
    - Rejected ~113 (5.6%) with warm selection cuts
  - Thermal cycle test on FEMB rejected and replaced FE failed at LN2
    - On average, 1 chip on two FEMBs (8x2) failed at LN2 (~6%)
- FE ASIC chips for APA6 passed QC test at both RT and LN2
  - Rejected ~4% of the FE ASICs in the cold screening test
    - Collection baseline < 100 mV
    - Failed to observe calibration pulse
    - Power cycle failure (start-up issue)
    - Input pin dead to external pulse
  - Only 1 FE ASIC replaced on all 21 FEMBs for APA6 (~0.6%)
- FE ASICs were tested under the thermal cycle (RT --> LN2) on FEMB

P1 ADC (Development discontinued after ProtoDUNE-SP) QC Results

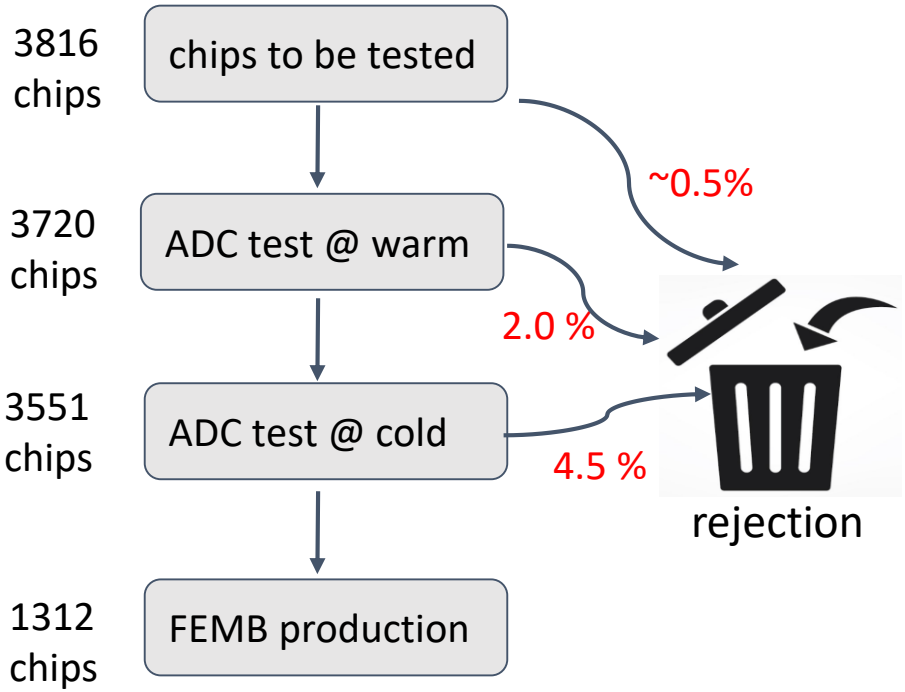
Just a reference for DUNE new ADC QC

Criteria for passing:

- ADC functionality with 1 & 2MHz internal/external clocks for all channels
- Slow external ramp input for detailed ADC linearity and stuck code calibration



August 2017-April 2018



Single-socket ADC test board

ADC Failure Mode

Temperature	Failure	# of chips
Total Handing failures	mostly drops	~20 (of 3816) 0.5%
RT	Only ½ of dynamic range worked	11
RT	SPI readback didn't match	28
RT	Sync failure	14
RT	Bad channel (no WF)	23
Total RT failures		76 (of 3816) 2.0%
CT	Bad input pin (high ADC count)	72
CT	SPI readback didn't match	39
CT	Sync failure	24
CT	Bad channel (no WF)	29
CT	Large rollback	5
Total CT failures		169 (of 3720) 4.5%

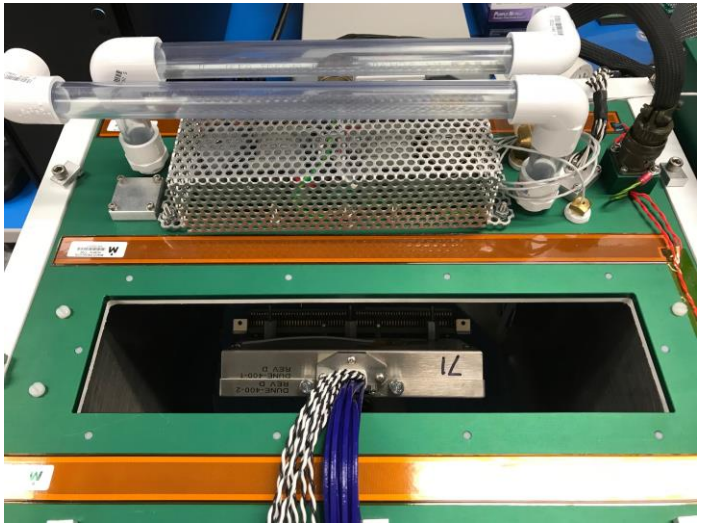
Ranked by Q metric, 37% selected for production

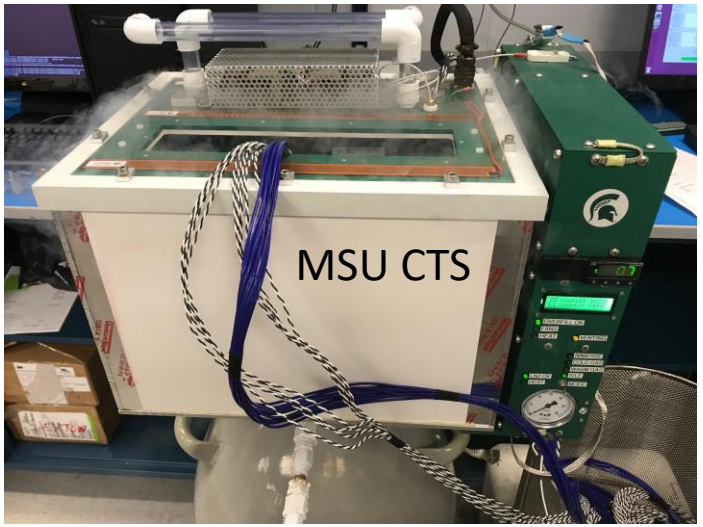
Oscillator and Flash Cold Screening Test

- Oscillator cold screening
  - 700 XO were tested over 175 test runs on a quad socket XO test board
  - ~450 were accepted for FEMBs (64%)
- Flash memory cold screening (Not needed for DUNE FEMB)
  - The FPGA mezzanine has one Altera EPCS64 flash memory to load firmware on power up
  - 860 chips were tested over 216 test runs on a quad socket flash test board
  - ~190 were accepted for FEMBs (22%)

FEMB QC Tests

- Power cycle test
  - Power to FEMB cycled and simple baseline measurement performed
  - 5 iterations
- Gain/ENC measurements
  - 17 separate gain/ENC measurements performed with different combinations of configurations
    - Gain: 14mV/fC, 25mV/fC
    - Shaping time: 0.5us, 1.0us, 2.0us, 3.0us
    - Both FPGA-DAC and ASIC-DAC calibration
    - One check of internal ADC clocks using nominal FE settings
- Power / current monitoring
  - Reads back FEMB voltages/currents measured on WIB
- Summary PDF of test results created as part of the test automatically





Sample FEMB Test Summary

protoDUNE FEMB QC Summary: CE Box 3

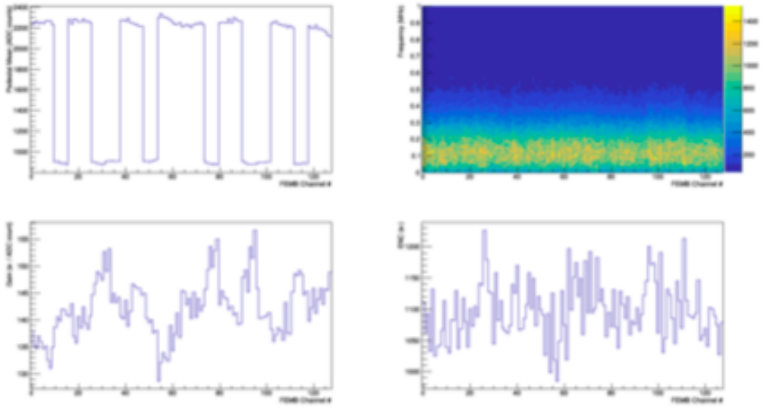
Timestamp: 20170810T161005 Tested by: Matt Bass Temperature: RT
Analog MB ID: 9 FPGA Mezz ID: 22

FE ASICS:	195	197	199	200	201	202	203	160
ADC ASICS:	70	41	67	13	380	55	110	379

Average ENC measured with internal pulser (electrons)

	0.5 us	1 us	2 us	3 us
14 mV/fC	1794	1270	1098	1115
25 mV/fC	1928	1223	1089	1111

Gain/ENC Measurement: Gain = 14 mV/fC, Shaping Time = 1 us, Internal Pulser



FEMB power cycled 5 times at beginning of data collection with no failure.

Current Monitoring:

Nominal Voltage	4.2 V	3 V	2.5 V	1.5 V	5 V
Voltage (V):	4.22	3.01	2.49	1.50	4.99
Current (A):	0.06	0.37	1.34	0.53	0.03

Data stored on hothdaq1:
/dsk/1/data/oper/femb/wib_sbnd_v109_femb_protodune_v308/20170810T161005
Position on WIB for test: 1

protoDUNE FEMB QC Summary: CE Box 3

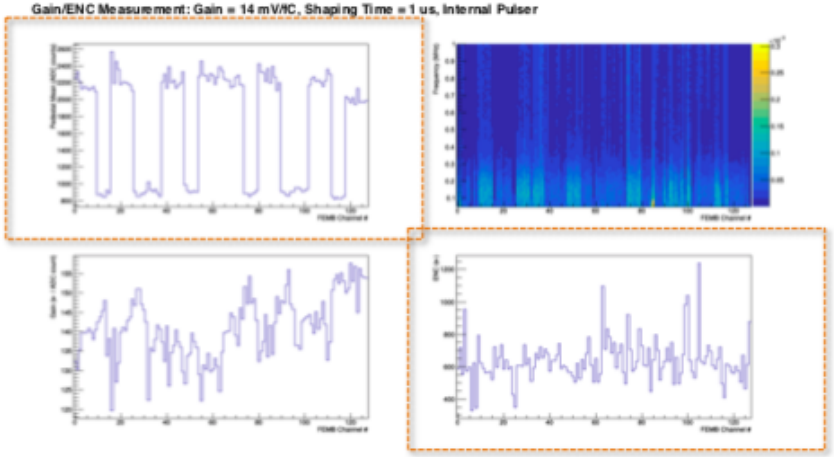
Timestamp: 20170810T173247 Tested by: Matt Bass Temperature: CT
Analog MB ID: 9 FPGA Mezz ID: 22

FE ASICS:	195	197	199	200	201	202	203	160
ADC ASICS:	70	41	67	13	380	55	110	379

Average ENC measured with internal pulser (electrons)

	0.5 us	1 us	2 us	3 us
14 mV/fC	969	719	637	653
25 mV/fC	926	650	589	601

Gain/ENC Measurement: Gain = 14 mV/fC, Shaping Time = 1 us, Internal Pulser



FEMB power cycled 5 times at beginning of data collection with no failure.

Current Monitoring:

Nominal Voltage	4.2 V	3 V	2.5 V	1.5 V	5 V
Voltage (V):	4.06	2.89	2.40	1.44	4.80
Current (A):	0.06	0.40	1.11	0.48	0.01

Data stored on hothdaq1:
reprocess/dsk/1/data/oper/femb/wib_sbnd_v109_femb_protodune_v308/20170810T173247
Position on WIB for test: 1

From Elizabeth Worcester

FEMB QC Test Results

- 25 FEMBs for APA1 tested warm in August 2017 (2.5 weeks)
  - 23 shipped to CERN
  - Rejected 2 because of ADC sync issues later resolved
- 124 production FEMBs tested warm and cold from 11/2017-4/2018
  - Rate dictated by APA delivery schedule which dictated ADC selections
  - Took about 2 hours to take/analyze data including the cryo cycle

Stage	# pass	# fail	Example failures
RT pre-screen	141	8	Bad connector to FM, short on AM, excess low frequency noise, FE SPI fails on ½ AM
CT pre-screen	139	2	Bad connector to FM, sync failure on ½ AM
Dressed QC	135	4	Excess low frequency noise, ADC sync failures, single bad channels
At CERN	120+1	13+1	See next slide

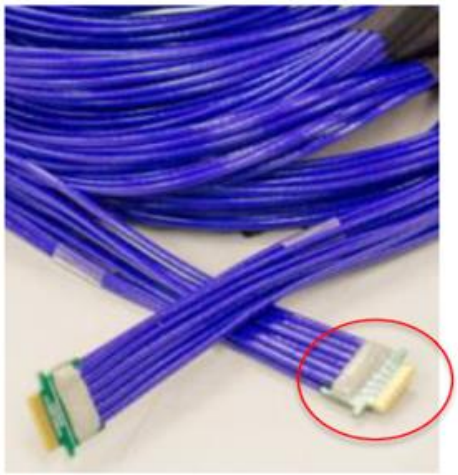
Summary of Failed FEMBs at CERN

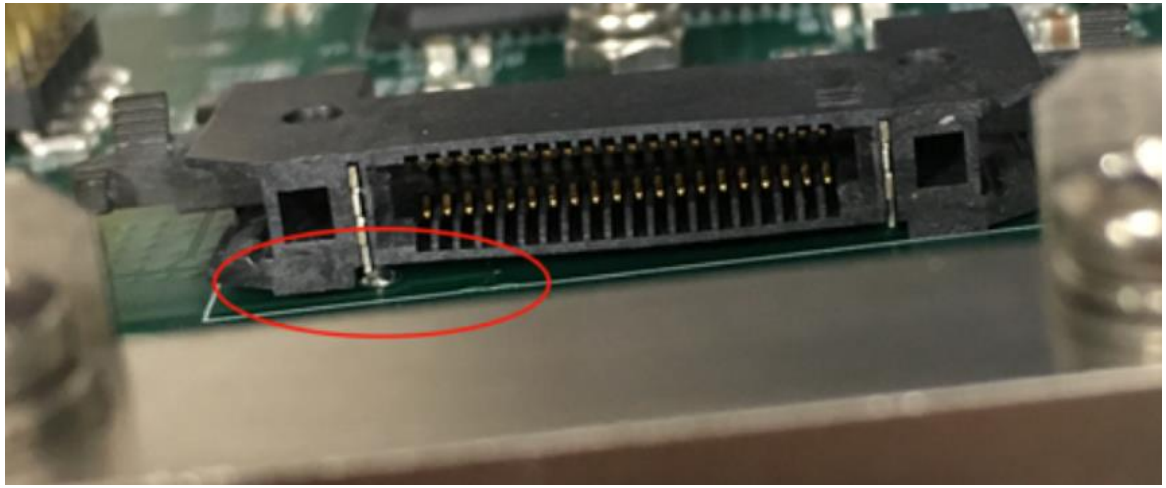
- Each CE box contains a FEMB assembly
  - 9 of 14 failed FEMBs at CERN due to broken data connectors

APA	Failure Mode	CE Box IDs Replaced	Testing Stage Identified
1	*1 dead FE channel at RT*	*009*	*QC at BNL*
	1 LV return wire cut during cabling on APA	020	Installation
	3 dead FE channels at RT	024	Installation
2	Data cable connector failed during GN2 cooldown	039	Cold Box
3	1 dead channel at RT	069	Installation
	Data cable connector failed at RT in cold box	018, 049, 075	Cold Box
	1 FE ASIC (16 channels) failed during GN2 cooldown	022	Cold Box
4	1 dead channel at RT	091	Reception
	Data cable connector failed at RT in cold box	085	Cold Box
5	Data cable connector failed at RT in cold box	106, 122	Cold Box
6	Data cable connector failed at RT in cryostat	112	Cryostat
	Data cable connector failed	146	Reception

Data Cable Connector Failure

- Issue: Data cable connector on FM detached from PCB board
  - Resulted inoperative FEMB
  - 9 CE boxes were replaced due to connector failure
    - 1 rejected at reception
    - 7 replaced after cold box test
    - 1 replaced after APA installed in cryostat
  - 1 possible failure after cryostat filled
    - FEMB in cryostat was recovered with new firmware using on board oscillator as clock (bypassing the system clock)
- Solution for DUNE
  - Redesign both FM PCB and male connector attached to the cable
  - More information in Jack's talk





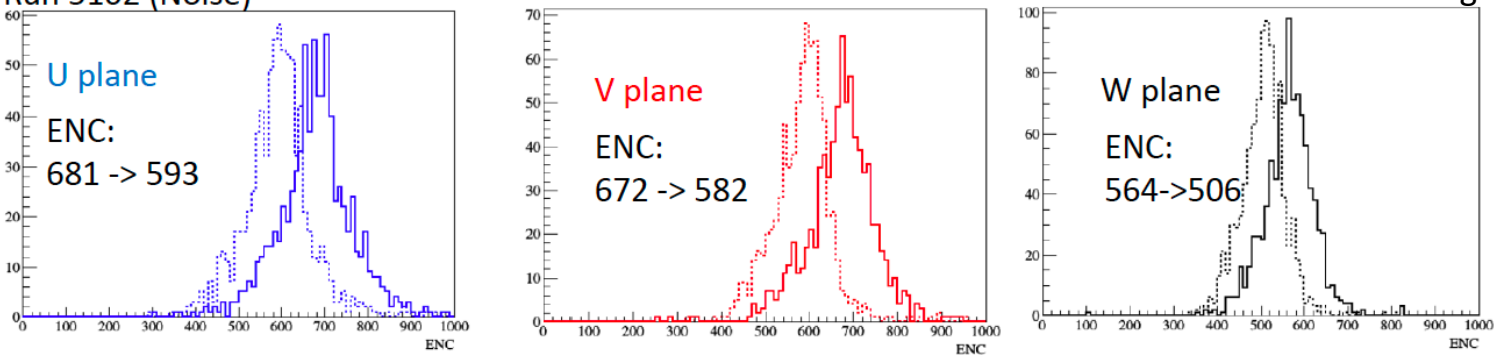
ProtoDUNE-SP CE Status in Detector Operation

- No FE channel got damaged by bias during CERN cold box integration test
  - No cathode but nominal wire bias voltages under strong LN2 air flow
- With 180kV cathode and nominal bias voltages
  - 99.74% (15320 of 15360) of TPC channels are active
    - **Only 4 inactive cold electronics channels**
  - **92.83% TPC channels have excellent noise performance**
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
  - **2 more inactive channels** on APA6 were observed Nov.27, 2019

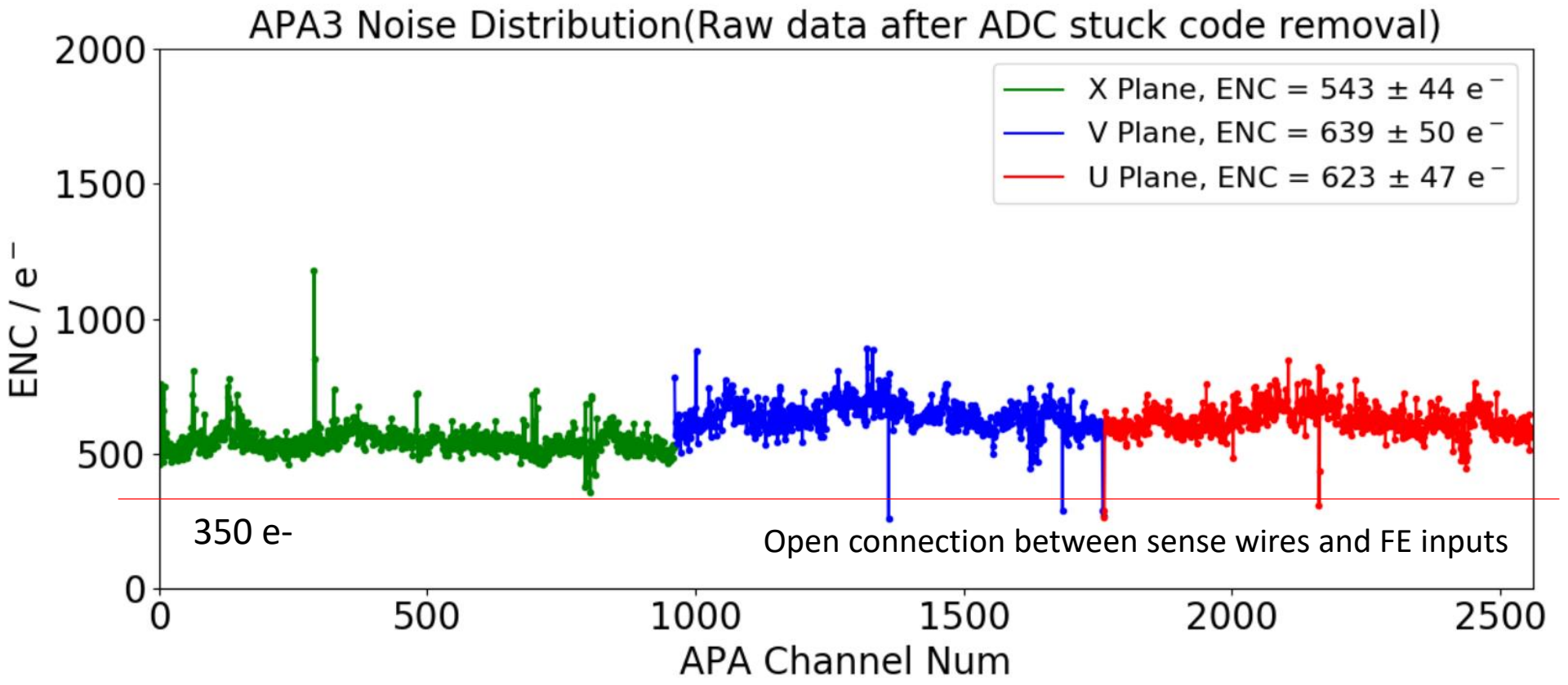
	09/13/2018		09/23/2018		11/27/2019
Item	**test#1**	**test#5**	**test #18**	**test #35**	**DAQ**
Drift	**off**	**120kV%**	**160kV**	**180kV**	**180kV**
Bias	**off**	**on**	**on**	**on**	**on**
FE Inactive	**0**	**2**	**4**	**4**	**6**
Channels (good & <800e-)	**14397**	14297	14179	**14259**	**/**

Run 5102 (Noise)

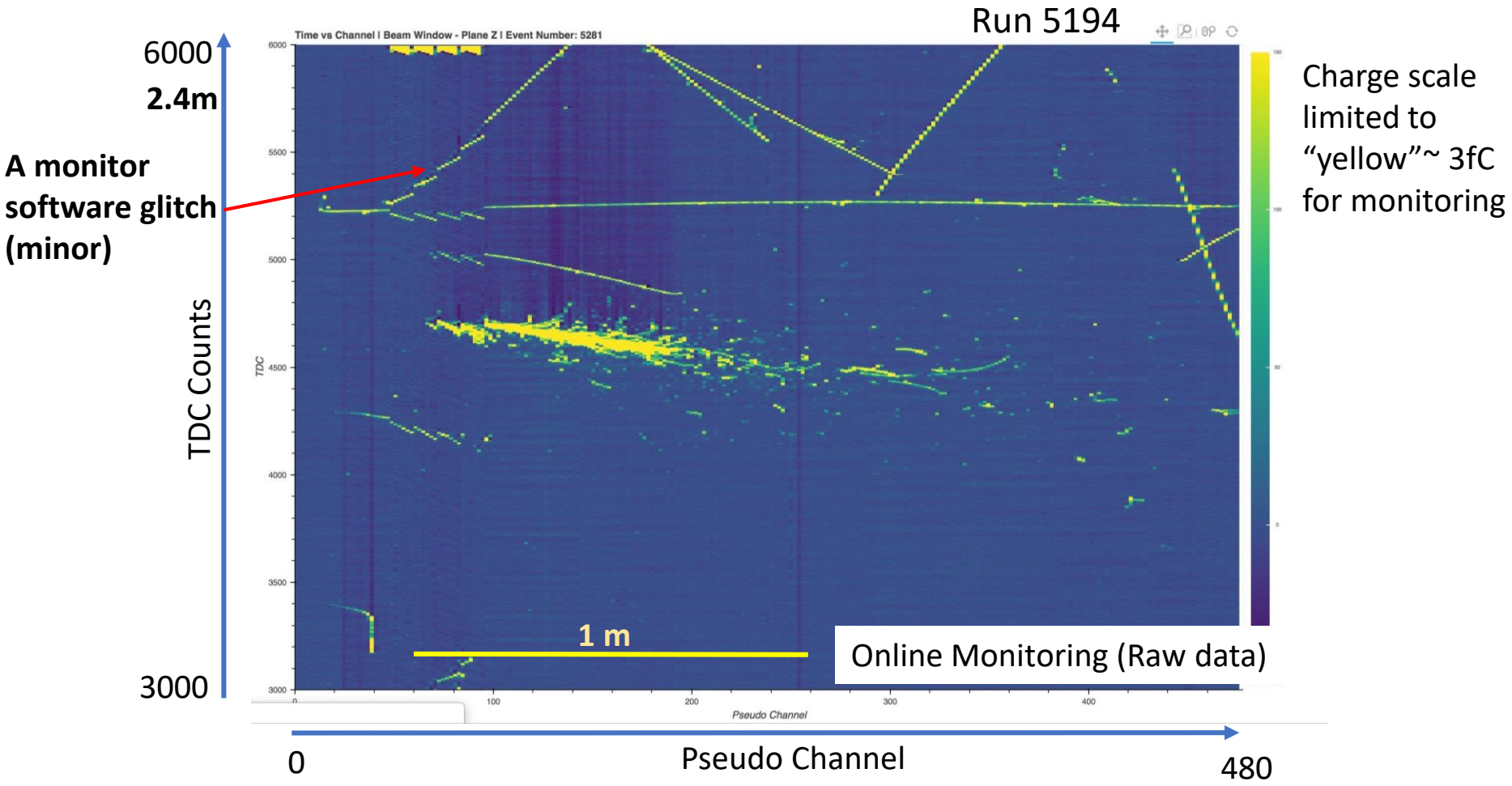
Solid line: raw data. Dotted line: offline filtering



APA3 Noise Distribution in ProtoDUNE-SP Commissioning



Shower Event under 7Gev Beam

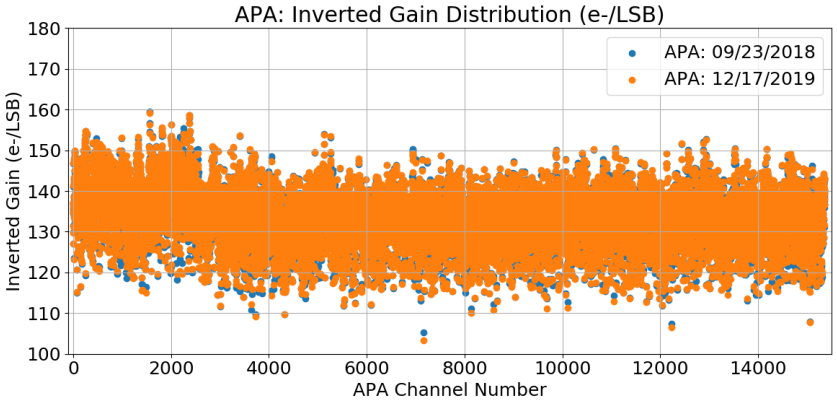


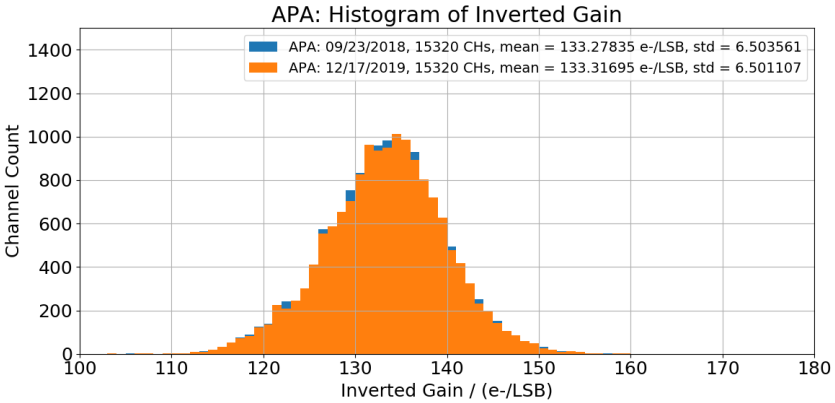
T. Yang's talk in the LBNC Review

- High signal-to-noise ratio (Collection Y: 48, induction U: 18, induction V: 21)
- Very few dead/noisy channels (< 0.1% dead)
- Most of the identified issues in raw data are minor and can be mitigated in the offline analysis

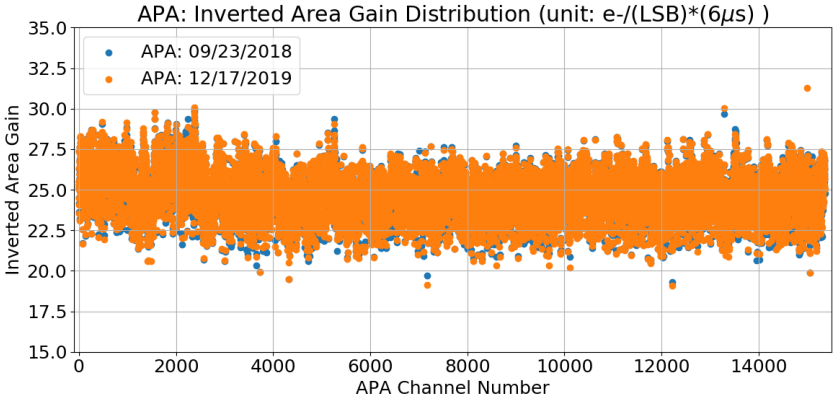
Stability of CE in ProtoDUNE-SP

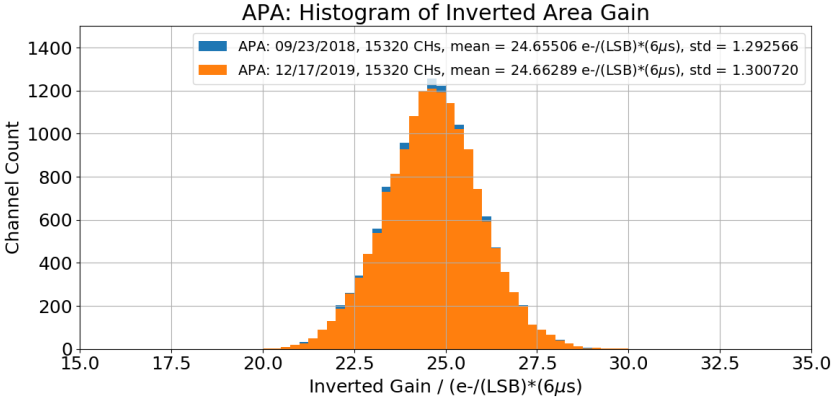
- No measurable degradation is observed over 15 months operation





Gain calculated from peaks indicates no degradation (0.03%) in the pulse amplitude





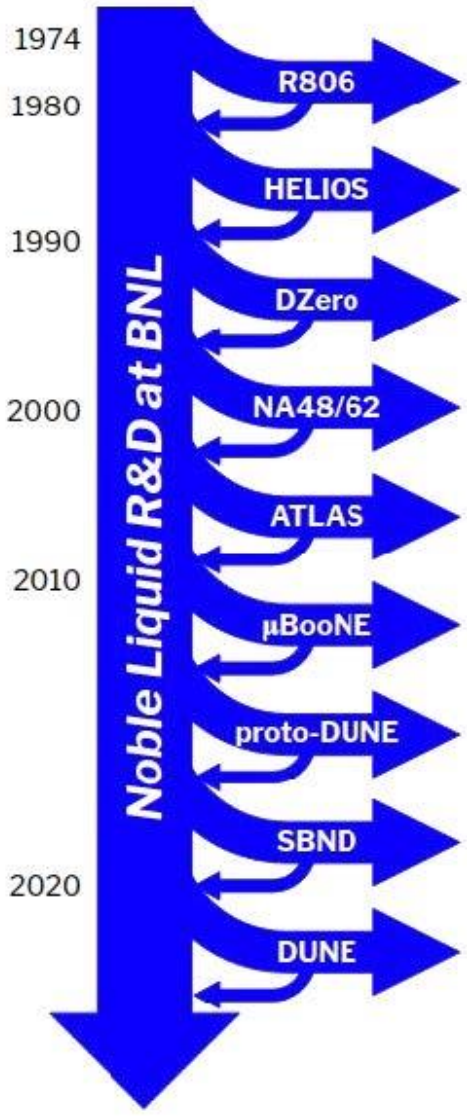
Gain calculated from areas indicates no degradation (0.03%) in the shape of pulse waveform

Summary

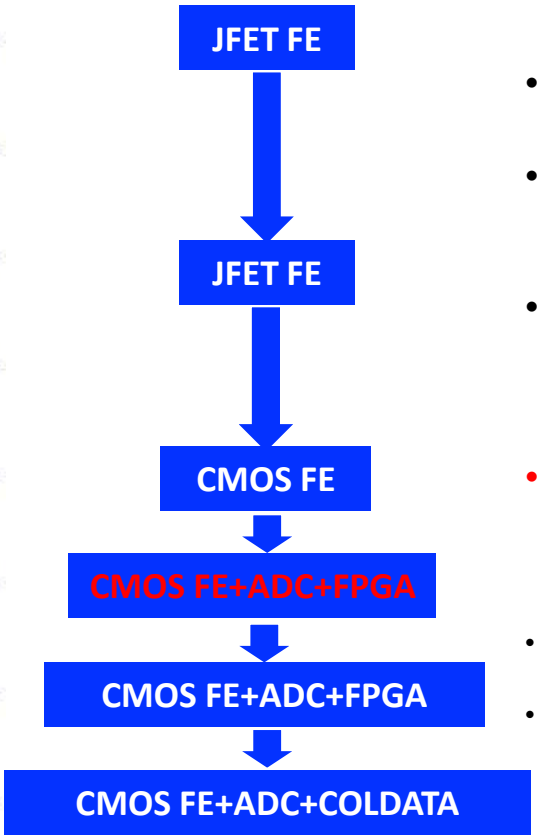
- ProtoDUNE-SP project at the CERN Neutrino Platform will provide validation of LArTPC technology, detector response and long-term stability for DUNE FD optimization
  - Readout electronics developed at BNL for low temperatures (77K-89K) is an enabling technology for noble liquid detectors for neutrino experiments
  - An integral design concept of APA + CE + Feed-through, and Warm Interface Electronics with local diagnostics and strict isolation and grounding rules is crucial for success of LArTPC experiments
  - Satisfactory noise performance
  - No measurable degradation is observed over 15 months operation
- Well-organized ProtoDUNE-SP QC campaign is proved valid and successful
  - 5-level (component, board, assembly, reception, infrastructure) QA/QC procedures assure a high-quality, functional cold electronics system is delivered on a tight schedule.
  - SBND cold electronics adopts similar QC plan and procedures, a good reference for ProtoDUNE-II and DUNE Far Detector

Backups

Long History of Noble Liquid Development



Advancement of Cold Electronics



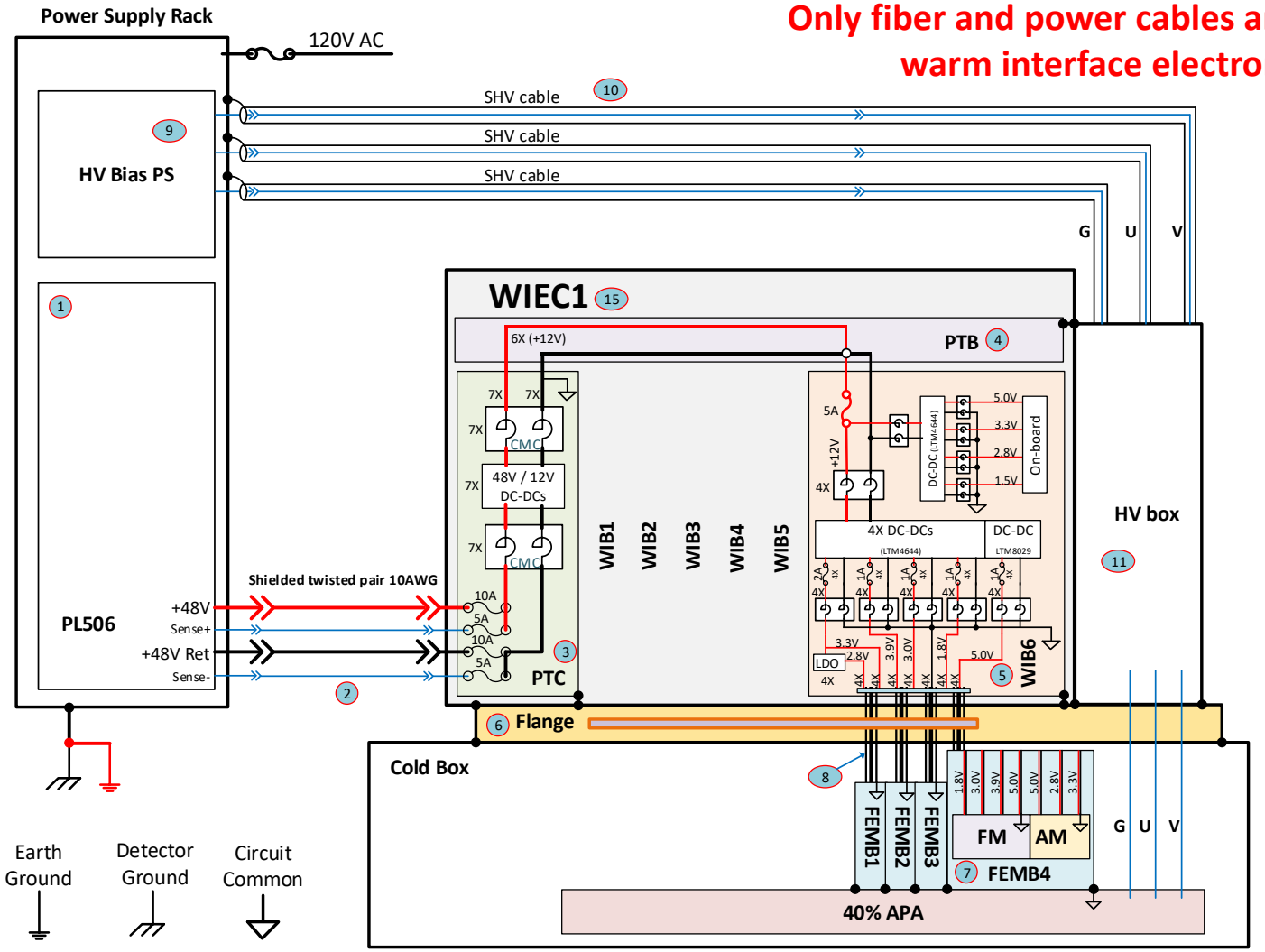
- BNL pioneered LAr based detector technology in 1974 [1]
- Physics/Engineering expertise which has made essential contributions to various programs, e.g. ATLAS, MicroBooNE
- Unique experience in cryogenic electronics and micro-electronics
- The R&D effort makes the experiments possible; the experiments, in turn, feed information back into the R&D process
- Cold electronics development is making continuous advancement, from JFET to CMOS, from analog front-end to mixed signal ADC and FPGA
- ***A strong cold electronics team is built up as a core BNL competence, in close collaboration with other institutes, to realize various LAr TPC experiments***
- *[1] W. Willis, V. Radeka, Nucl. Instr. Methods, 120 (1974) 221*
- *[2] COLDATA is being developed by Fermilab*

Grounding and Isolation Rules

- ProtoDUNE TPC uses extremely sensitive electronics to measure the charge from the TPC wires
  - A grounding scheme has been developed to isolate the detector and local detector electronics racks from all other electrical systems
- Following experience from ATLAS and MicroBooNE experiment
  - APA frame should be connected to the COMMON of all FE ASICs
  - All electrical connections (power and signal) from APA shall lead to a single feed-through.
  - The COMMON of the FE ASIC and of the rest of cold readout shall be connected to the common plane/enclosure of the cold FE module (FEMB)
  - The flange of feed-through should be the only connection of the APA frame to the cryostat
  - The APA frame to the cryostat should be insulated
  - Avoid ground loops

40% APA LV Diagram (Including Grounding Scheme)

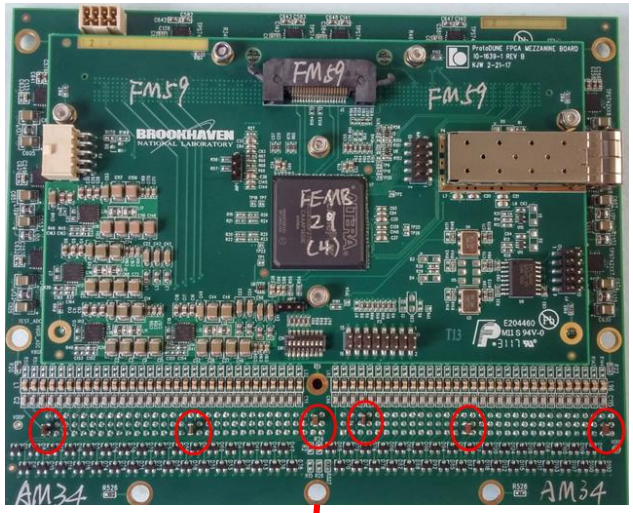
Only fiber and power cables are coming out of warm interface electronics crate



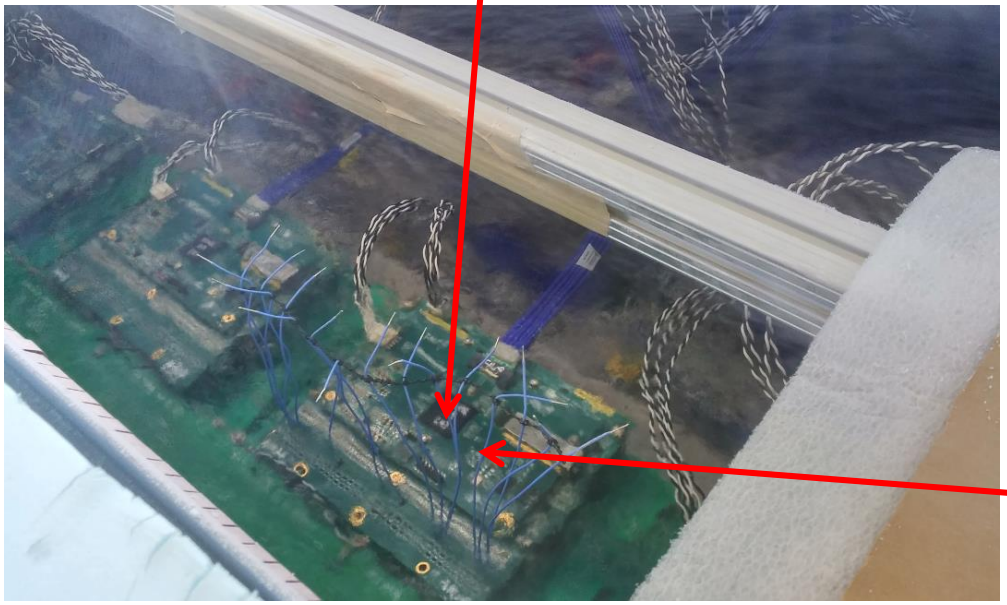
1: Weiner PL506 provided by Fermilab
2: 48V power cable provide by Fermilab
3: PTC (Power and Timing Card)
SBND-DocDb-9329
10A Fuse P/N: 7040.3190
5A Fuse P/N: 3404.0017.11
Choke P/N: PLT10HH501100PNL
4. PTB (Power and Timing Backplane)
SBND-DocDb-9329
5: WIB (Warm Interface Board)
SBND-DocDb-9329
5A Fuse P/N: 3404.0017.11
2A Fuse P/N: 0468002.NR
1A Fuse P/N: 0468001.NR
Choke P/N: PLT5BPH5013R1SNL
6: Flange Board
SBND-DocDb-6086
7: FEMB (Front End Motherboard)
SBND-DocDb-9326
FM: FPGA Mezzanine
AM: Analog Motherboard
8: 7m cold power cable
SBND-DocDb-6080
9: HV bias power supply
10: SHV cables
11: HV box
With filter inside.

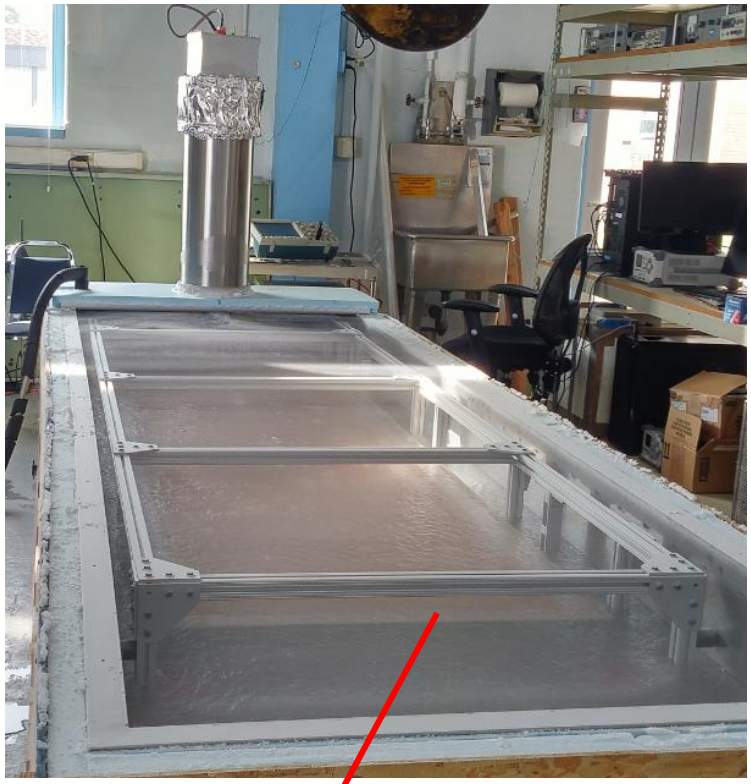
Notes
(1) PTB is mounted with the brass standoffs as a grounding connection
(2) The grounding connection between WIBs and WIEC is through front panels and side bars
(3) The grounding connection between PTB and WIEC is through front panels and side bars
(4) Flange (and flange board) is the place that the FEMB circuit common is referenced to the cryostat (detector ground)

More Pictures



Some channels with extra 82pF/150pF MICA caps

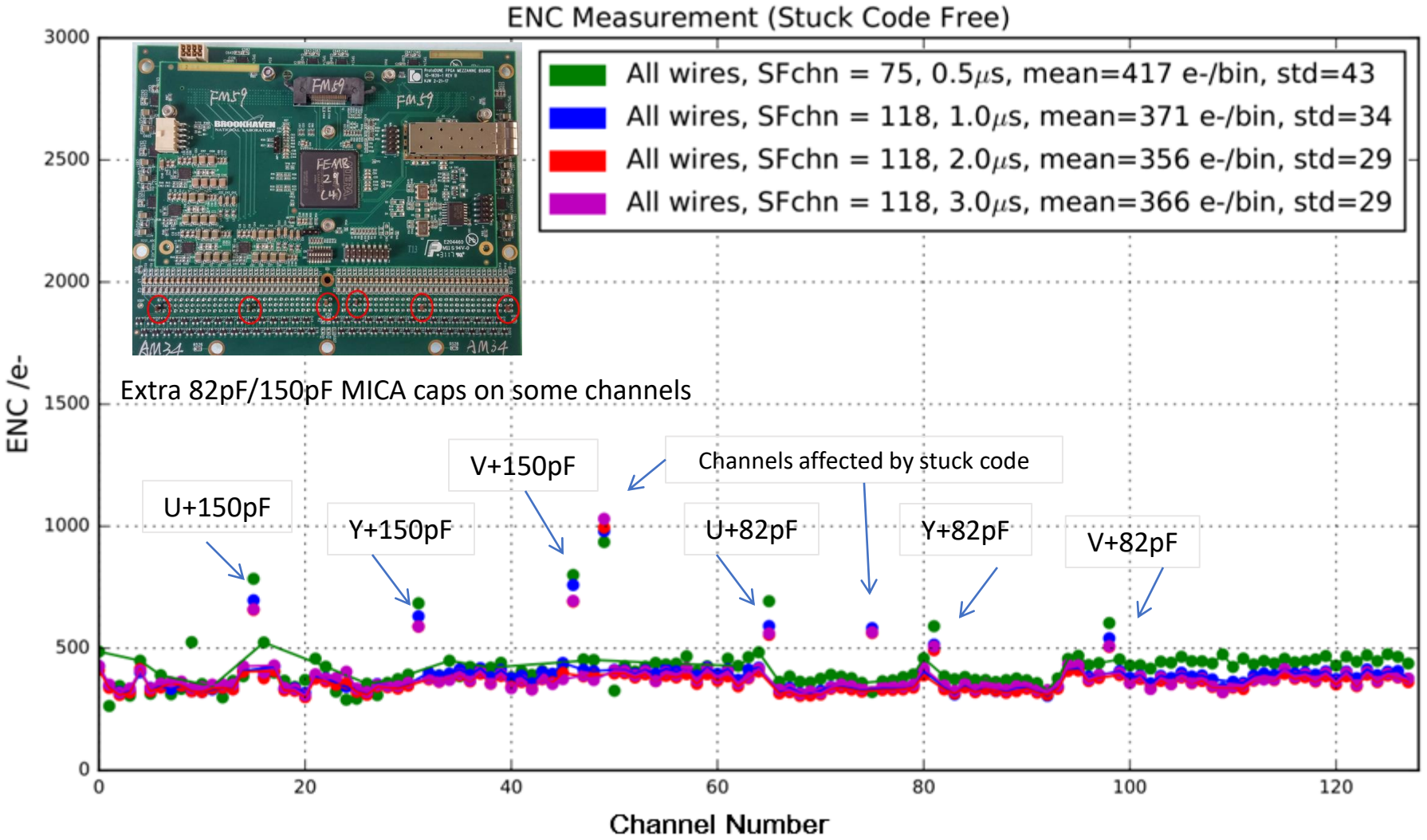




After cold test, 40% APA were still fully submerged in LN2
(~ 400 gallons LN2 was consumed)

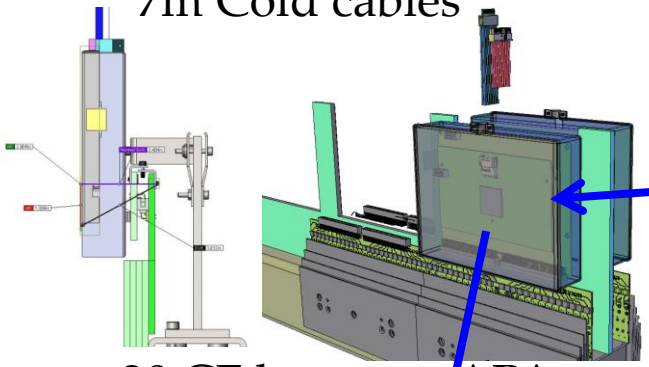
APA and FEMBs were fully submerged in LN2

ENC Measurement at LN2

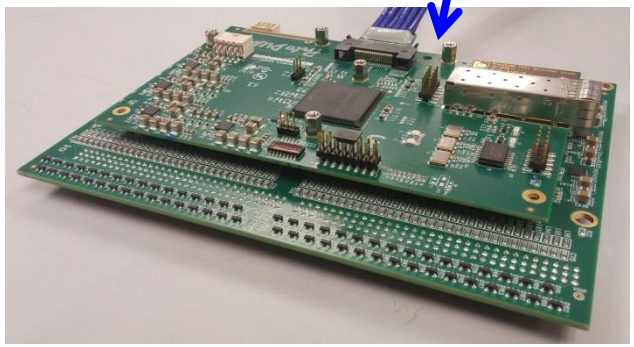


ProtoDUNE-SP FE Electronics

7m Cold cables

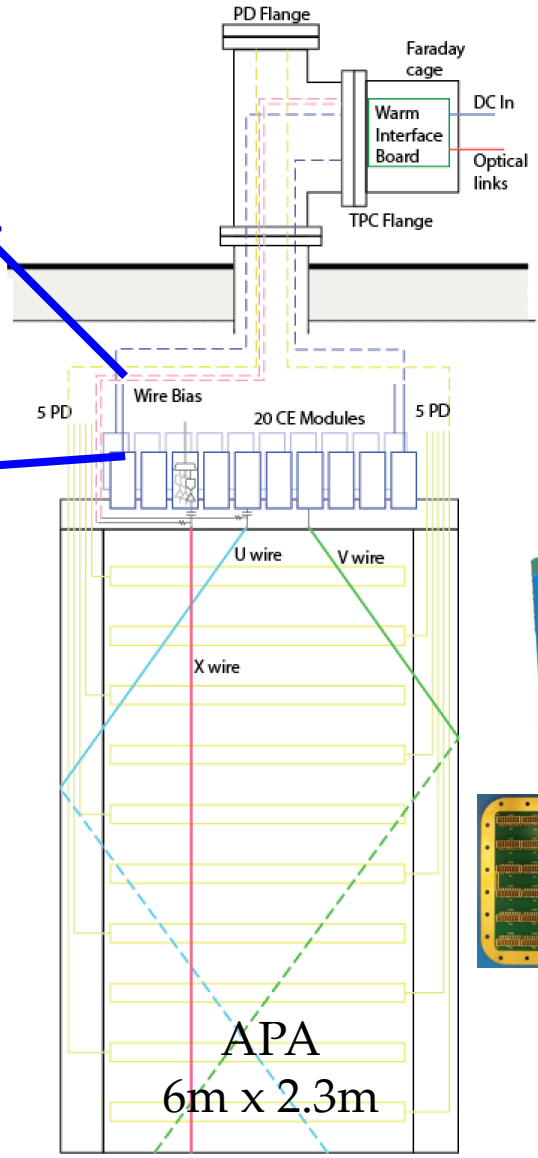


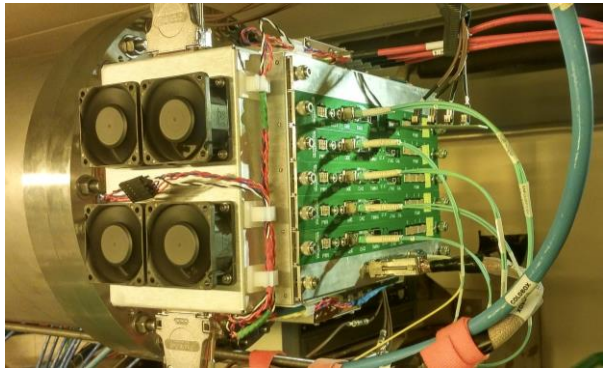
20 CE boxes on APA



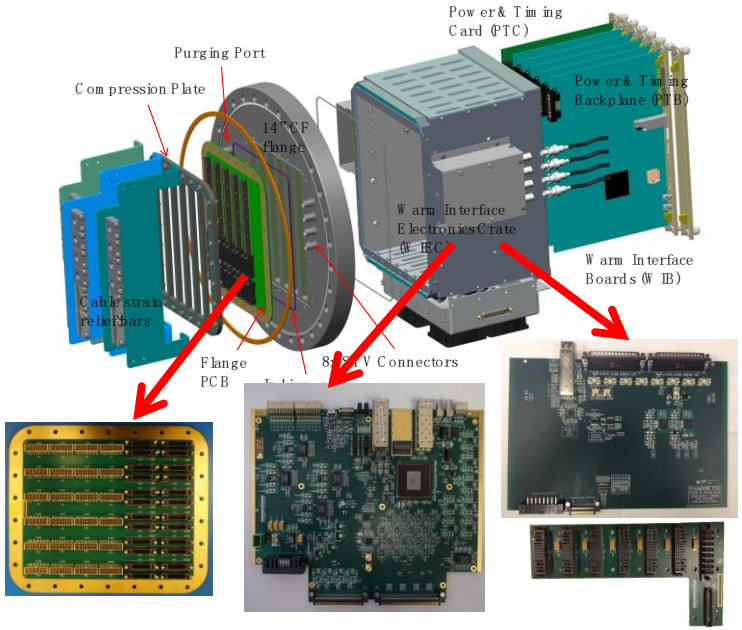
FEMB (inside CE box)

Cold Side





Signal Feed-through Assembly



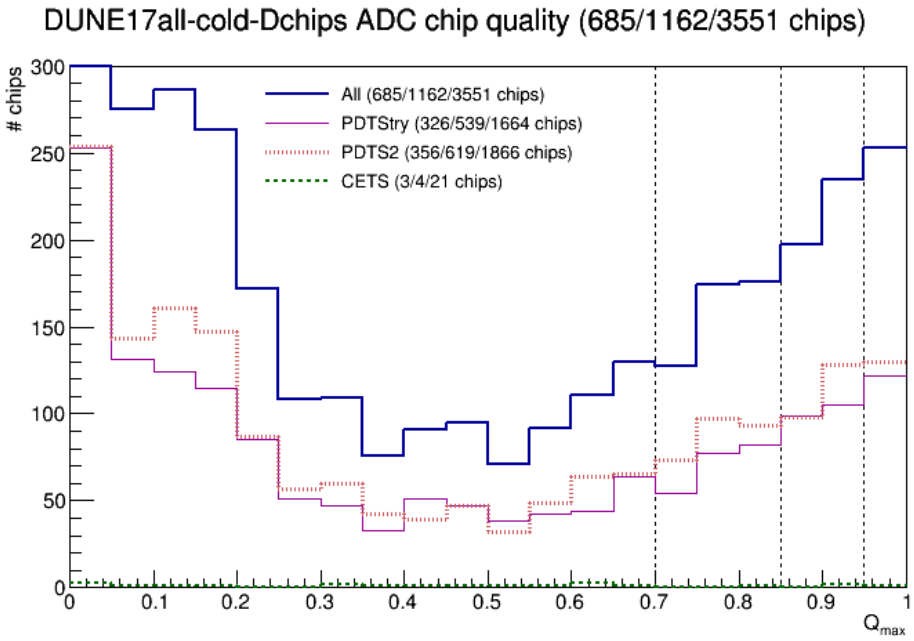
Flange Board, WIB, PTC, PTB

Warm Side

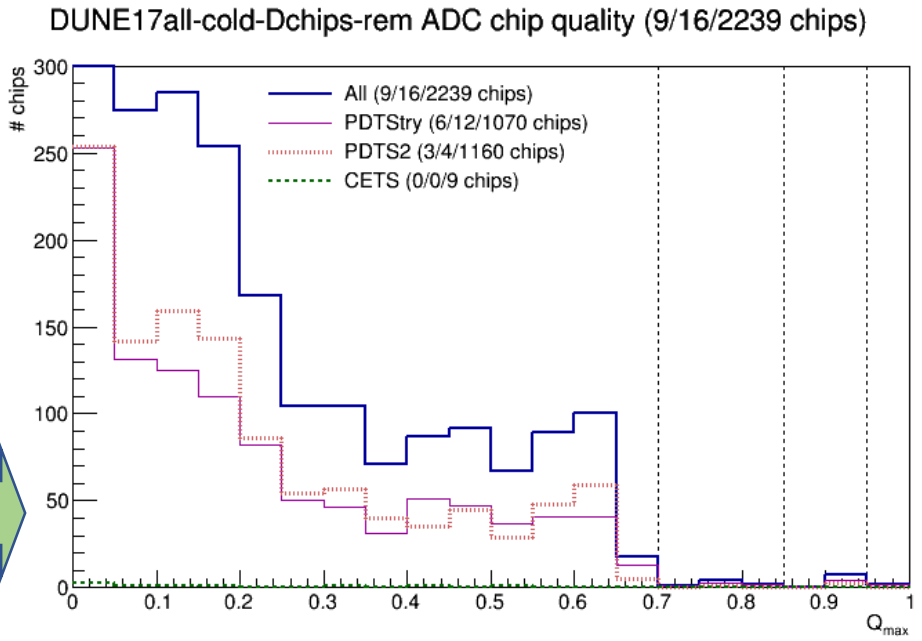
P1 ADC ranking (by Q)

ADC Q score is the efficiency for all input ranges in all channels multiplied (explored by David Adams) - detailed definition, check David Adams

Before selection (all ADCs)



After selection (all ADCs)



1,312 ADCs selected

ADCs selected in 6 lots (one per APA) roughly every month during the production testing
ADCs for APAs 2-6 had Q>0.7 (30%), the final selection for APA7 took Q>0.65

Statistics of Total 15360 TPC channels

09/13/2018 09/23/2018

Priority (1 is highest)	Item	test#1	test#5	test #18	test #35
/	**Drift**	**off**	**120kV%**	**160kV**	**180kV**
/	**Bias**	**off**	**on**	**on**	**on**
1	ADC Sync Error	**112**	112	0	**0**
2	FE Start up	**13**	40	16	**0**
3	**FE Inactive**	**0**	**2**	**4**	**4**
4	FE Calibration Error	**0**	0	0	**0**
5	FE Gain > 180e-/ADC	2	2	2	2
6	FE Gain < 90e-/ADC	**0**	0	0	**0**
7	Pedestal with unremovable stuck code	**48**	52	59	**45**
8	**Broken Connection ENC < 350 e-**	**41**	38	39	**34**
9	ENC > 2000 e-	**2**	0	1	**3**
10	2000 e->= ENC > 1000 e-	**295**	348	405	**386**
11	1000 e->=ENC > 800 e-	**446**	466	655	**627**
12	**Channels (good & <800e-)**	**14397**	14297	14179	**14259**
/	Active FE channels	**15229**	15201	15338	**15354**
/	Active TPC channels	**15188**	15163	15299	**15320**
/	**Channels (good & <800e-) / 15360 channels**	**93.73%**	**93.08%**	**92.31%**	**92.83%**
/	**Active FE channels / 15360 channels**	**99.15%**	98.96%	99.86%	**99.96%**
/	**Active TPC channels / 15360 channels**	**98.88%**	98.72%	99.60%	**99.74%**

Update CFG paras to fix ADC Sync error

No dead channel existed when LAr filling is done (07/08/2018)

4 more channels identified by no response to real event by David Adam

99.74% of TPC channels are active
92.83% of TPC channels are good with excellent noise performance (ENC < 800e$^-$)

Failure Modes Based on FEMB (CE Box) at CERN

Failure Mode	# of CE box				
	Reception	cold box checkout before cool down	Cold box chekcout during cooldown	Cryostat warm checkout (07/08/2018)	cryostat cold checkout(09/13/2018)
FEMB with one or more dead channels	3 (note.A)	2 (note.B)	0	1 (note.C)	3 (note.D)
Cabling misoperation (e.g. wire cut)	0	1 (note.E)	0	0	0
Broken Data Cable Connector	1 (note.F)	6 (note.G)	1 (note.H)	1 (note.I)	1 (note.M)
Misjudge	0	0	1 (note.J)	0	0
FE start-up	0	0	1 (note.K)		3 (note.L)

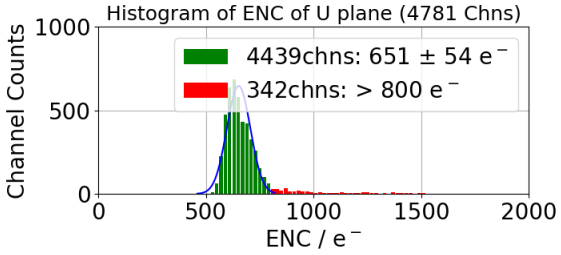
CE boxes can be replaced and repaired at BNL

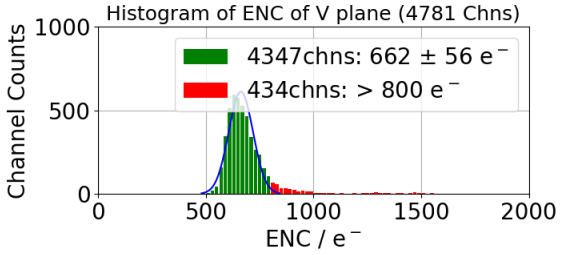
CE boxes can't be replaced

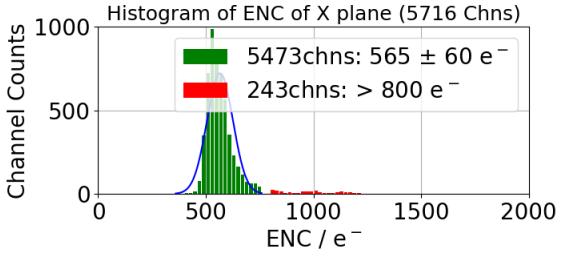
Notes:

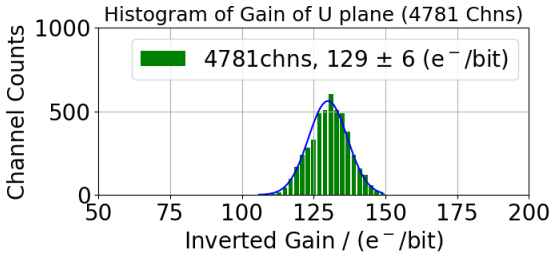
A. FEMB#49CH49, FEMB#18CH56, FEMB#69CH?
B. FEMB#24CH(64,65,109), FEMB#9CHN65
C. A channel on A115(FEMB#08) was inactive at warm, but came back to alive at cold (possible contaminated)
D. FEMB#119(B605CH52), FEMB#14(A120CH30), FEMB147(A515CH15, CH53)
E. FEMB#20: 1 LV return wire cut during cabling on APA
F. FEMB#146
G. FEMB#(39, 18, 49, 85, 106, 122)
H. FEMB#75
I. FEMB#112, replaced with a new FEMB in cryostat
J. FEMB#123
K. FEMB#22, 1 FE ASIC with start-up issue.
L. 6 FE ASICs on 4 FEMBs suffer start-up issue: FEMB#60_A316(FE#6, FE#8), FEMB#61_B407(FE#1), FEMB#120_A514(FE#2, FE#5), FEMB#108_A519(FE#5) . Fixed by changing FE baseline to 900mV
M. FEMB#56_B302: 100MHz clock link is broken, fixed by new firmware with onboard XO.

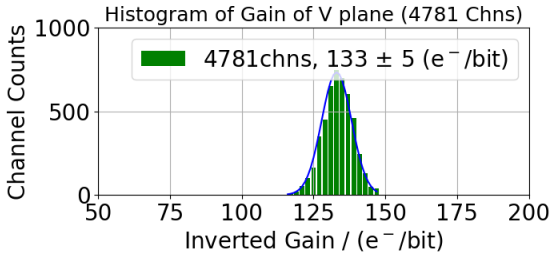
Test#35 (09/23/2018)
CE Performance Evaluation (**Drift = 180kV, Nominal Bias**)

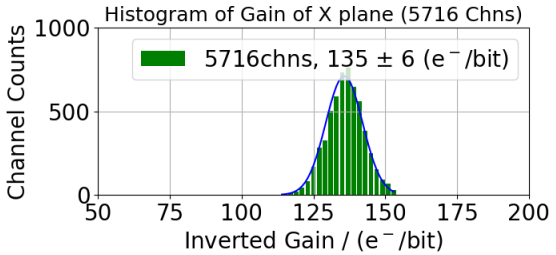


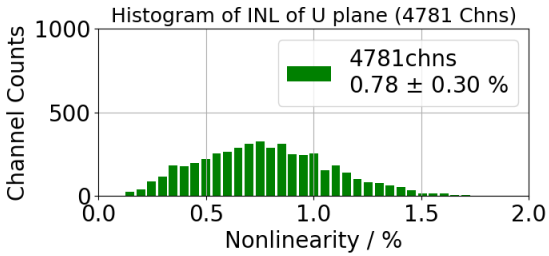


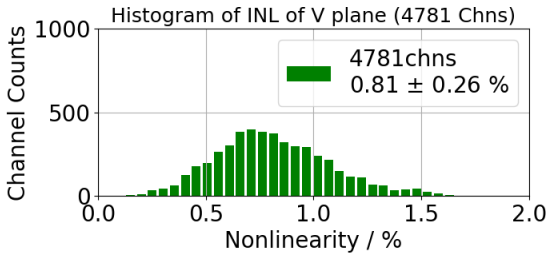


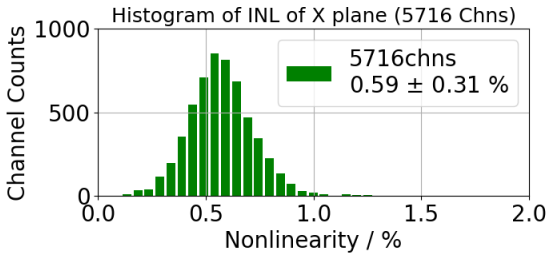












Provided by BNL CE Group