FEMBs
Design of FEMBs with LArASIC, ColdADC, FPGA/COLDATA

Jack Fried on behalf of the CE group

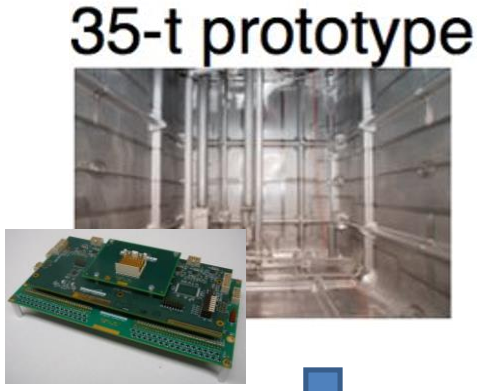
February 6 , 2020

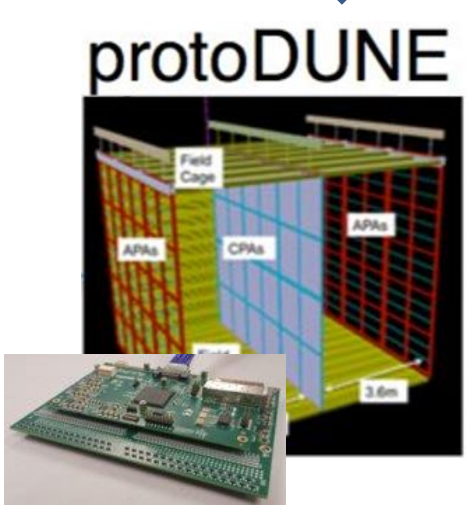
Outline

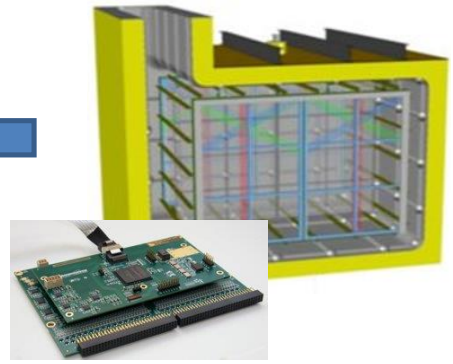
- FEMB History
- FEMB Versions
  - LArASIC + P1 ADC + FPGA
  - LArASIC + ColdADC + FPGA
  - LArASIC + ColdADC + COLDATA
- FEMB Data Cable
  - FPGA
  - COLDATA
- FEMB Power Cable
  - FPGA
  - COLDATA
- FEMB lessons learned
  - FEMB diagnostics
  - Connector issue
  - FEMB unique address

Frontend Board Experience

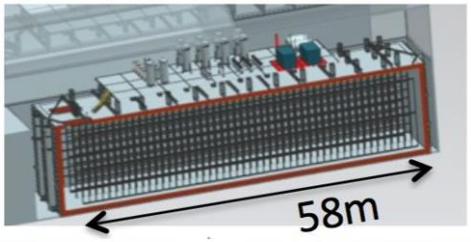
- Cold electronics development
  - MicroBooNE
  - 35-ton
  - ProtoDUNE-SP







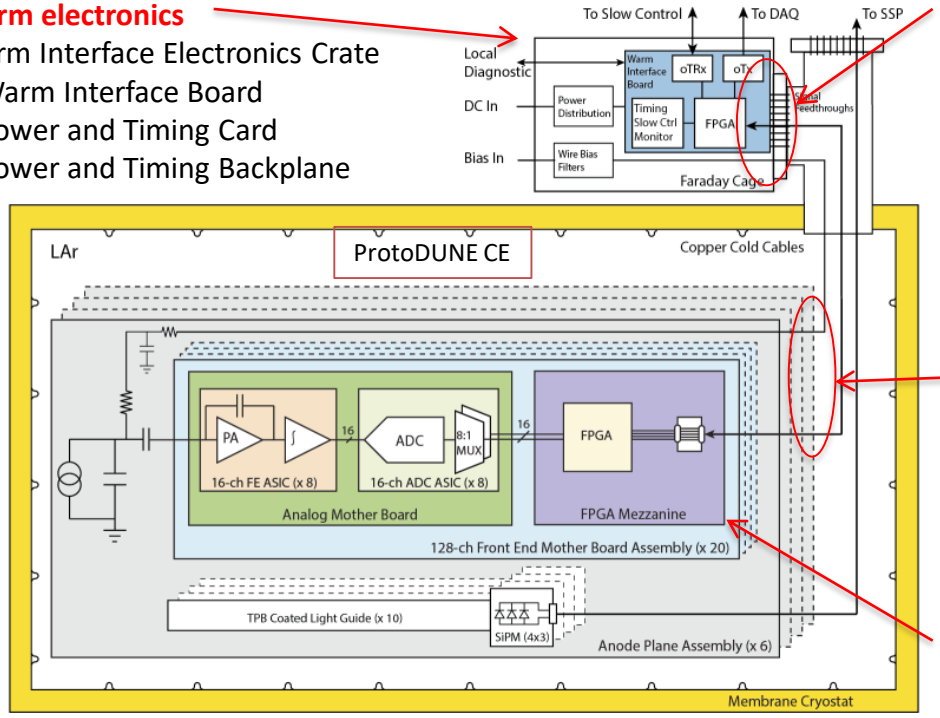
DUNE Reference Design
basis for first 10 kt module



Cold Electronics

Warm electronics

Warm Interface Electronics Crate
- Warm Interface Board
- Power and Timing Card
- Power and Timing Backplane



CE flange

Flange assembly with cable strain relief and flange PCB for cable/WIB connection

Cold cables

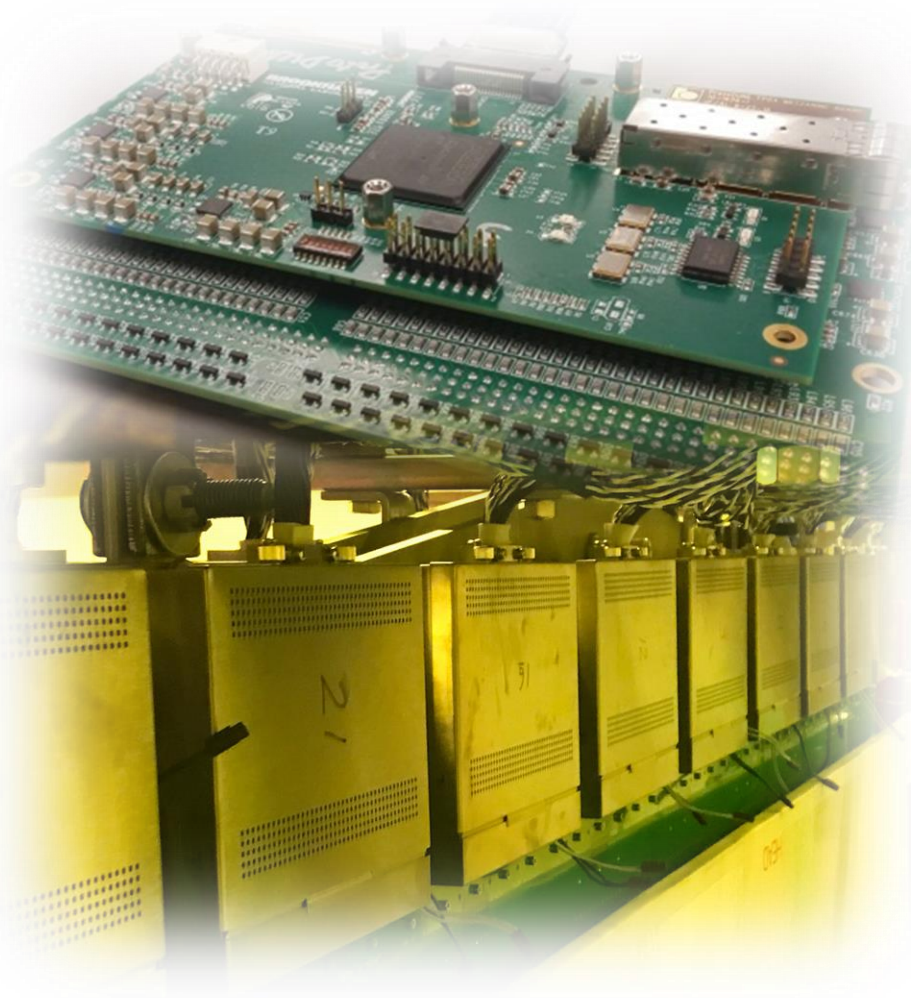
Cables used for low voltage and data/clock transport to FEMB's

Front End Motherboard

(FEMB) 128 channels of digitized wire readout enclosed in CE Box

What all FEMBs have in common

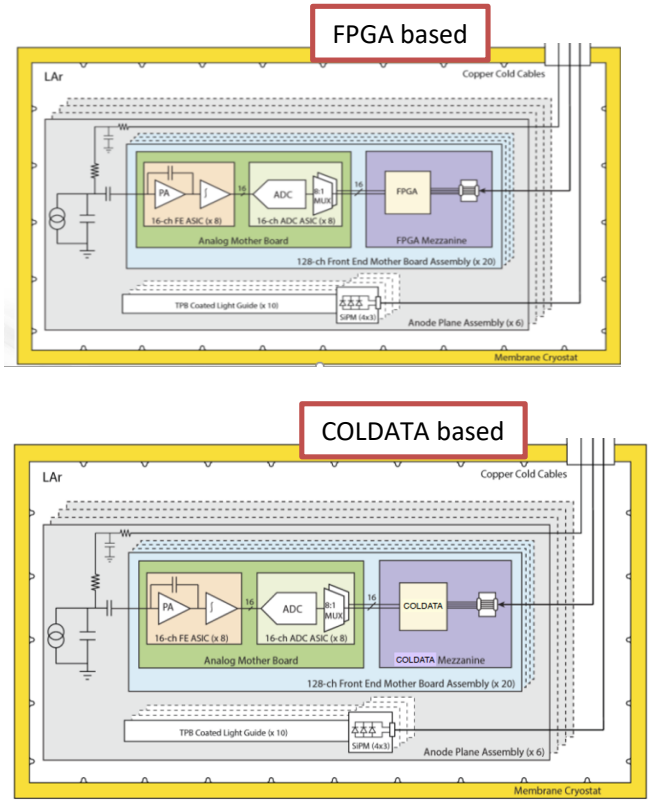
- 128 input channels
- Discrete input protection
- Data cable
  - TX link to warm
  - Slow control
  - Synchronous timing control
- Cold regulators
- Low voltage cable
- CE BOX



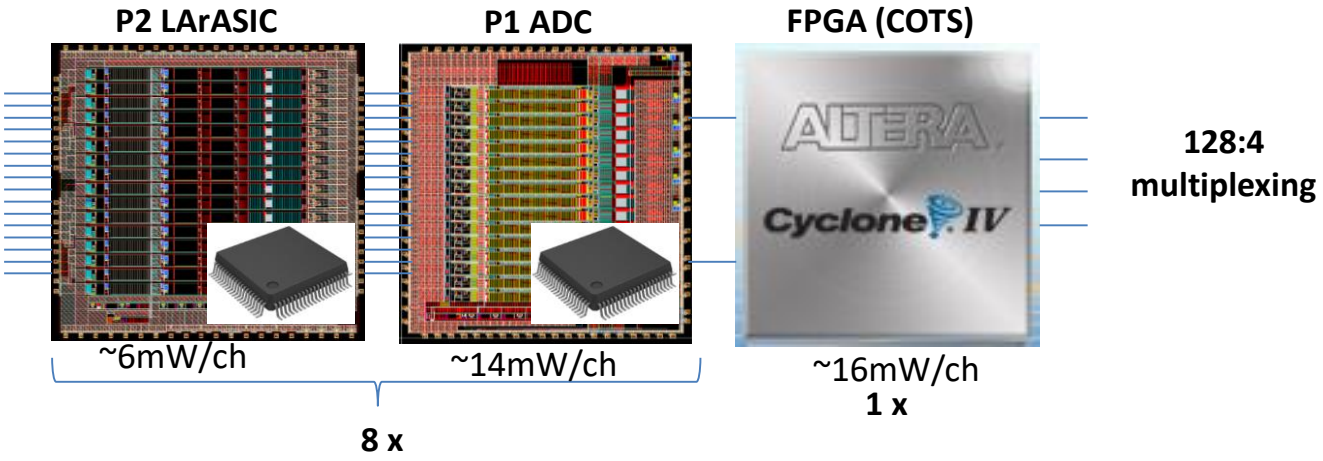
Cold Electronics FEMB

- FPGA based
  - LArASIC + P1 ADC + FPGA
  - LArASIC + ColdADC + FPGA
- COLDATA based
  - LArASIC + ColdADC + COLDATA

Signal & power needs for each type



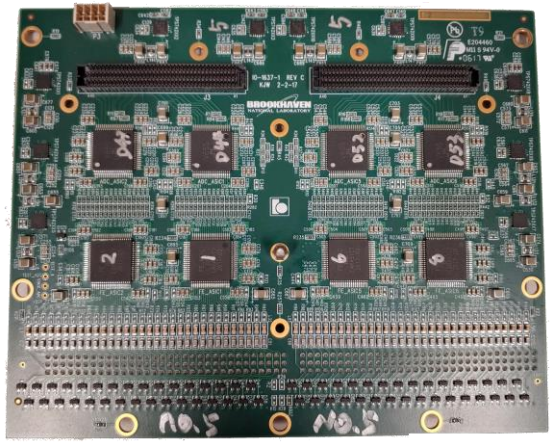
ProtoDUNE FEMB



ProtoDUNE FEMB

- Currently in use at ProtoDUNE
  - **120 boards used for over one year with no board failures**
- Consists of two boards
  - FPGA Mezzanine -- 14 Layer PCB
  - Analog Motherboard --10 Layer PCB
- FPGA Mezzanine
  - One Altera Cyclone IV FPGA
  - 3.6V, 2.8V,1.5V & 5V bias over 4 pairs on power cable
  - Analog monitor over power cable
- 128 channel DUNE Analog Motherboard (AM)
  - 8 x P2 LArASIC ASIC's
    - Four on top four on bottom
  - 8 x P1 ADC ASIC's
    - Four on top four on bottom
  - 2.2V and 5V bias supply over 4 pairs
- 12 pair Samtec data cable
- 9 pair Samtec power cable

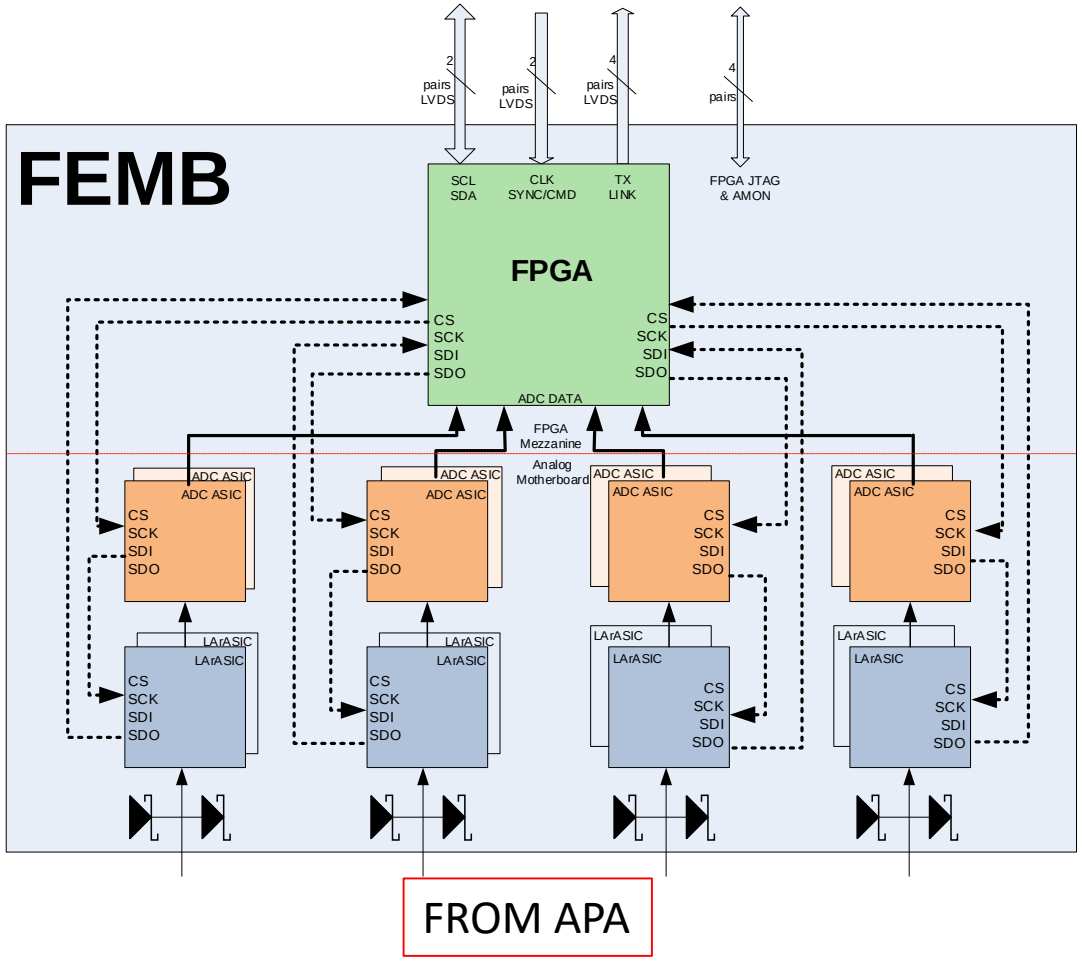
FPGA Mezzanine (FM)



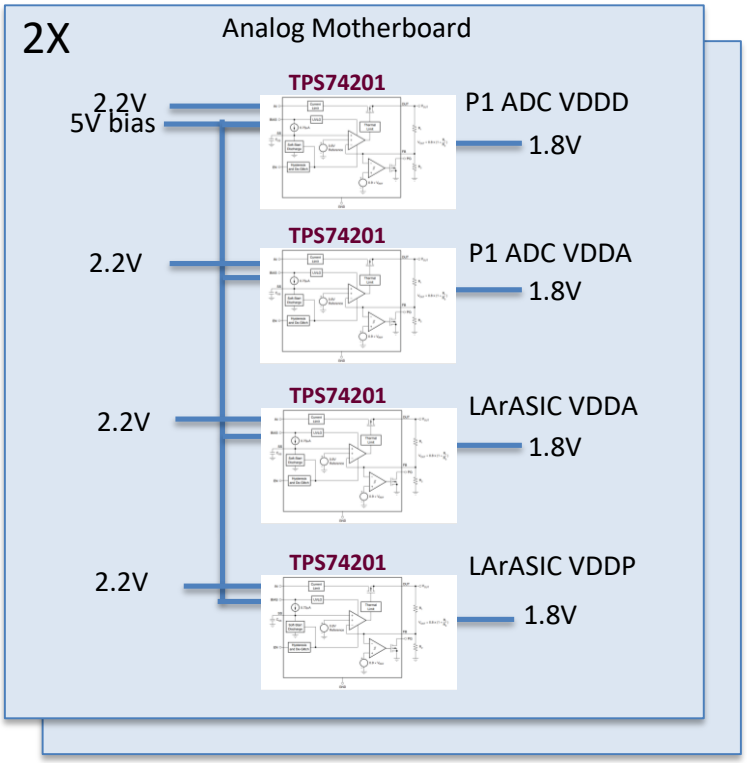
Analog Motherboard (AM)

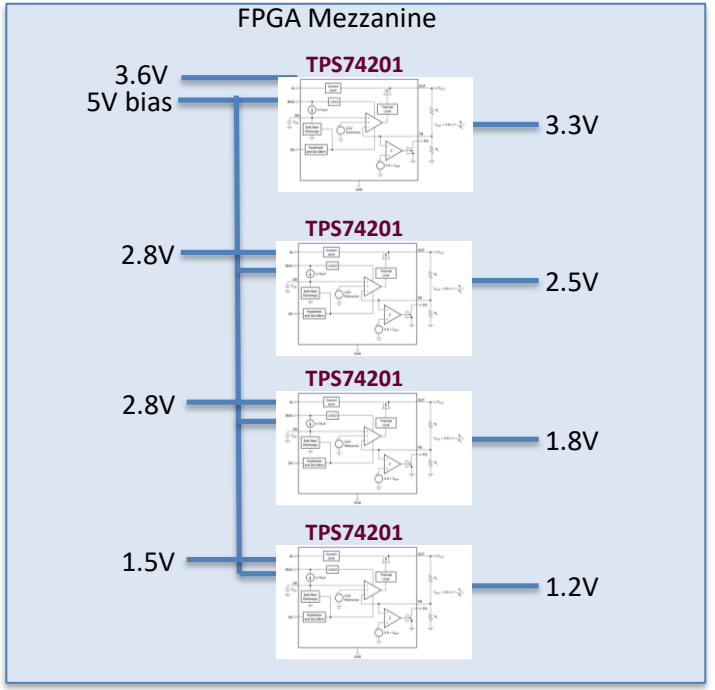
LArASIC + P1 ADC + FPGA

- Data Cable IO (12 Pairs)
  - 1.28Gb TX data link (4 pairs)
  - I2C link (2 pairs)
    - SDA bidir bussed LVDS
    - SCL standard LVDS
  - 100MHz Clock
  - SYNC/CMD
    - 2MHz DC balanced PWM signal (synchronous commands)
  - JTAG (4 pairs)
    - Single ended signals used to update FPGA firmware
- FEMB ASIC configuration
    - Eight independent SPI links controlled by the FPGA
    - Each SPI link has one ADC and LArASIC

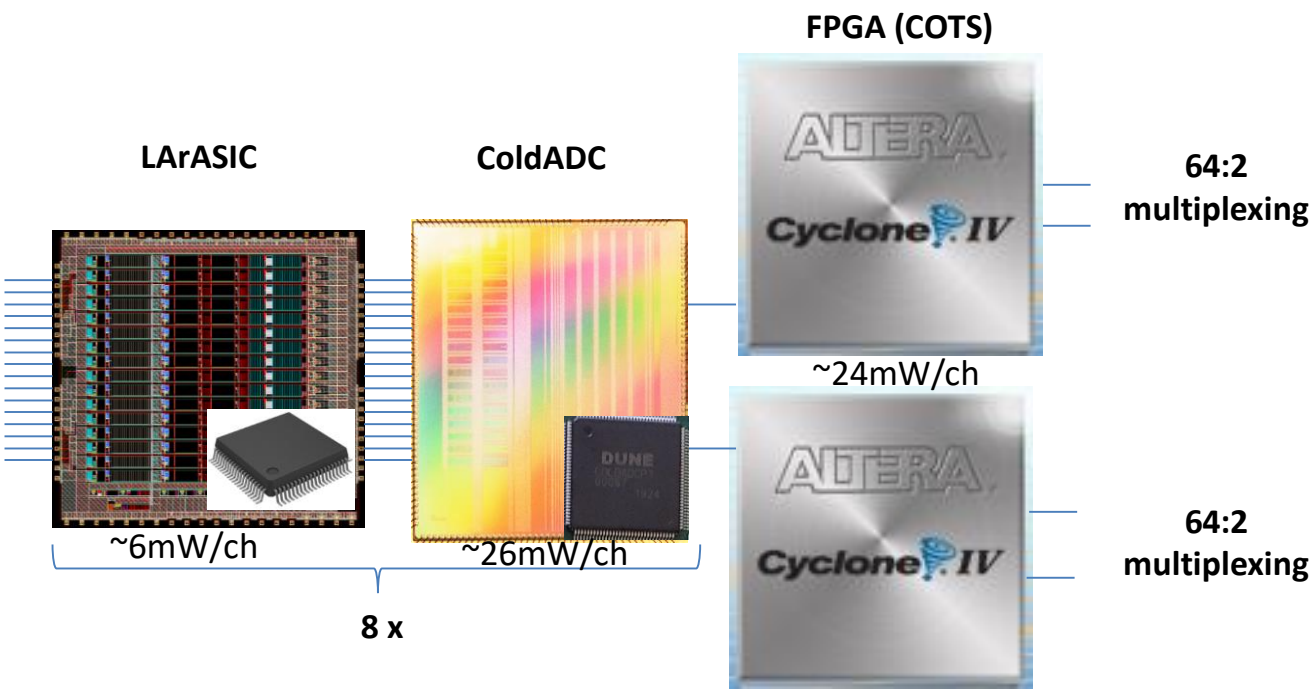


LArASIC + P1 ADC + FPGA Regulators





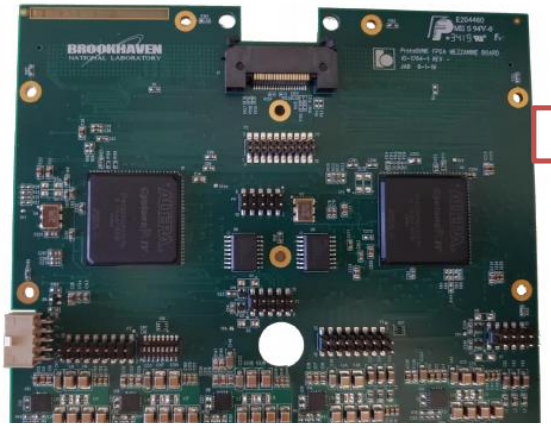
LArASIC + ColdADC + FPGA



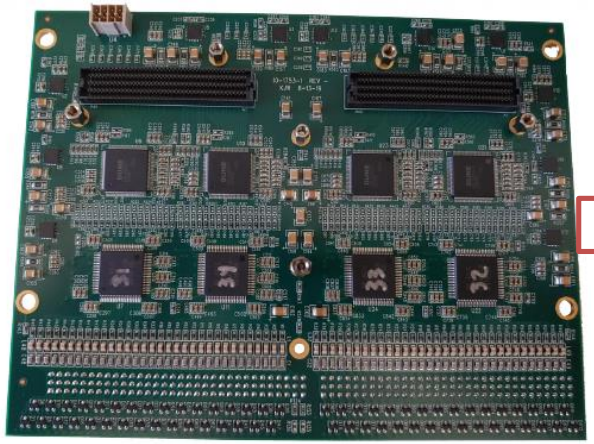
ColdADC runs at 64MHz instead of 200MHz calling for a wider bus, requiring two FPGA for meet IO needs

"LArASIC + ColdADC + FPGA" FEMB

- **First FEMB with new ColdADC**
- Consists of two boards
  - FPGA mezzanine -- 16 Layer PCB
  - Analog Motherboard --10 Layer PCB
- FPGA Mezzanine
  - Two Altera Cyclone IV FPGA
  - 3.6V, 2.8V,1.5V & 5V bias over 4 pairs
  - Analog monitor over power cable
- 128 channel DUNE Analog Motherboard (AM)
  - 8x ColdADC V1 chips ~22mW/ch
  - 8x LArASIC P2/P3 chips ~6mW/ch
  - POWER AM
    - 4.2V and 5V bias supply over 4 pairs (ProtoDUNE WIB)
    - 2.8V , 2.2V and 5V bias supply over 4 pairs (new DUNE WIB)
- Fully compatible with current ProtoDUNE WIB hardware and Firmware*
  - Identical data format/channel mapping as ProtoDUNE FEMB
  - *4 resistors on WIB to be replaced for raising AM supply voltage
  - *Configuration scripts will require an update to control ColdADC



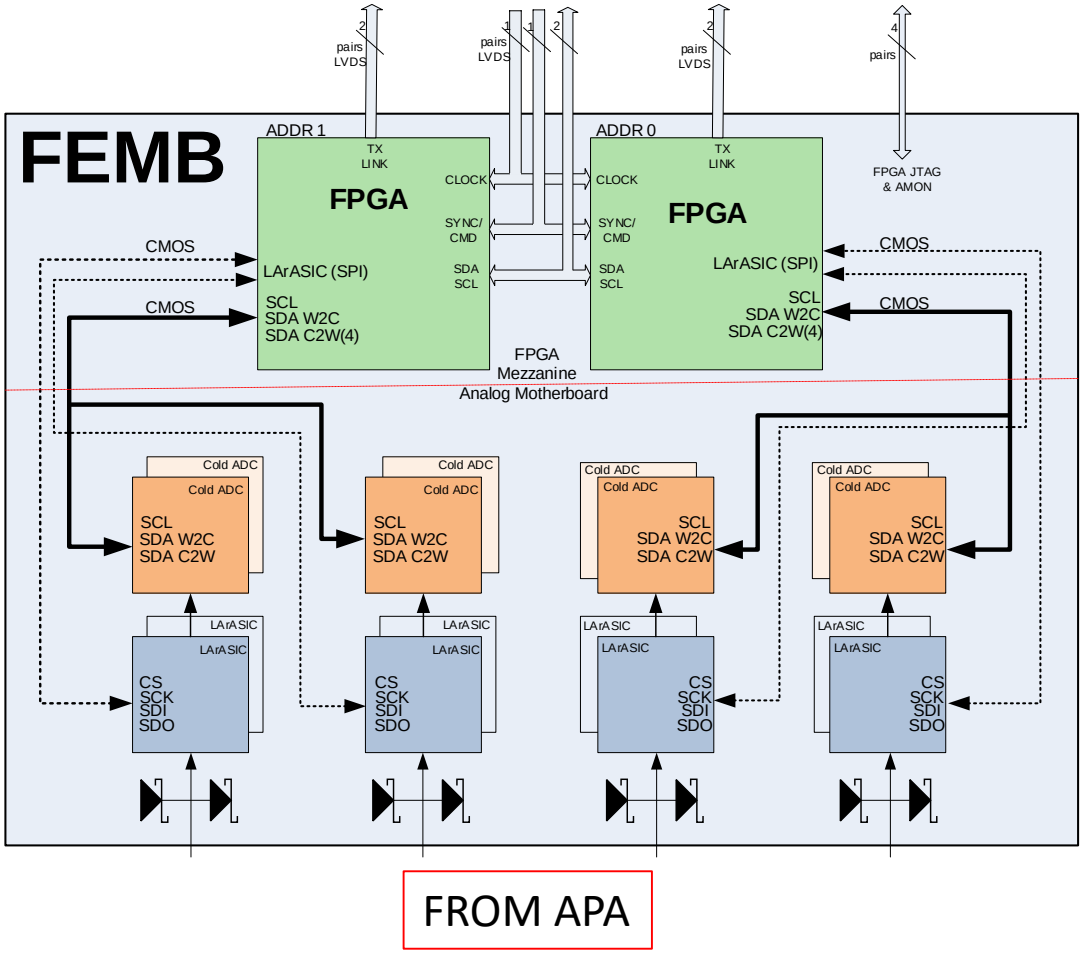
FPGA Mezzanine (FM)



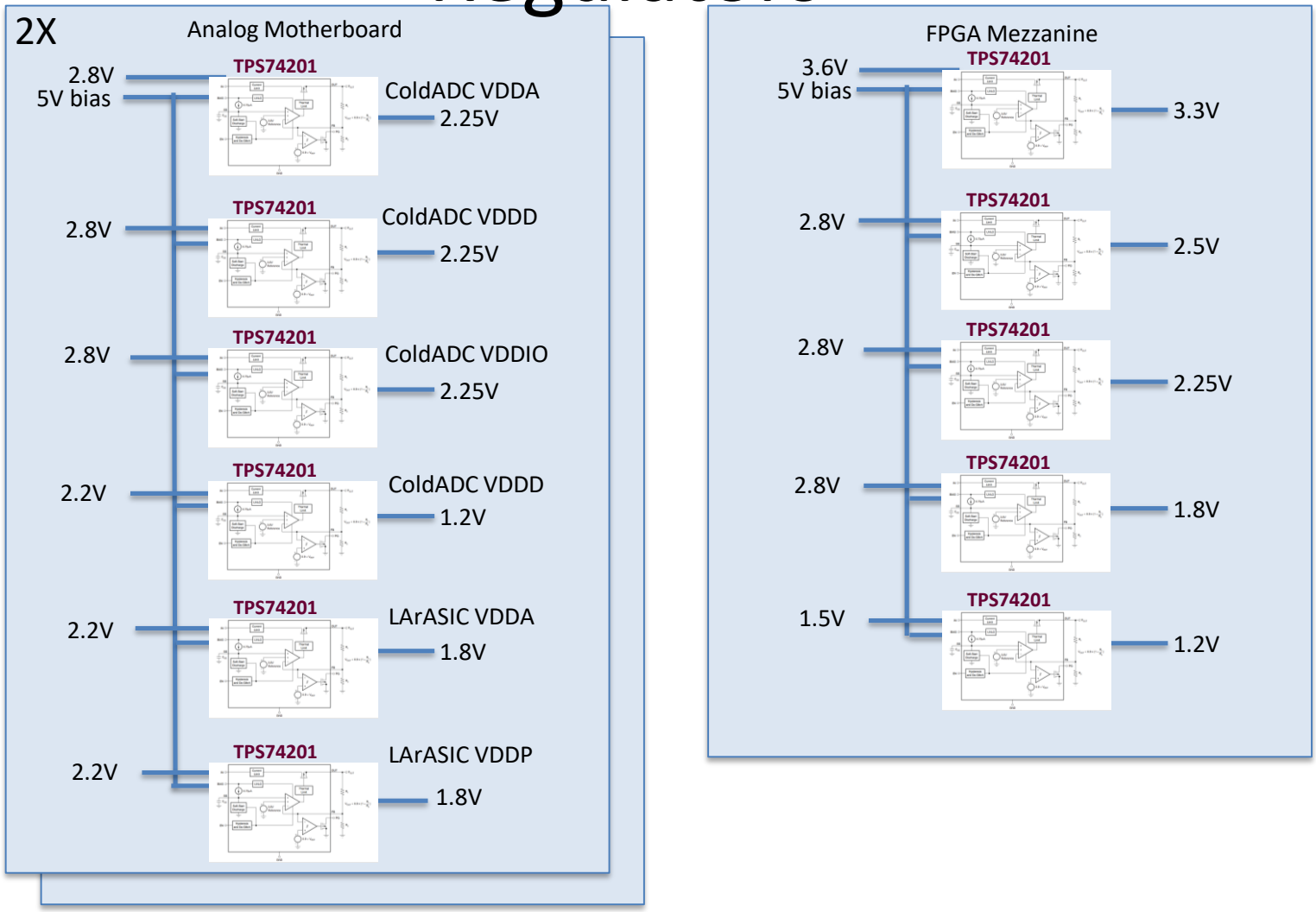
Analog Motherboard (AM)

LArASIC + ColdADC + FPGA

- Data Cable IO (12 Pairs)
  - 1.28Gb TX data link (4 pairs)
    - 2 for each FPGA
  - I2C link (2 pairs)
    - SDA bidir bussed LVDS
    - SCL standard LVDS
  - 100MHz Clock
  - SYNC/CMD
    - 2MHz DC balanced PWM signal (synchronous commands)
  - JTAG (4 pairs)
    - Single ended signals used to update FPGA firmware
    - TDO can be used as an analog monitor
- FPGA Shared signal form WIB
  - 100MHz clock
  - SYNC/CMD
  - I2C link
- FEMB ASIC configuration
  - Eight independent SPI links for LArASIC's
  - Eight ColdADC I2C links four per FPGA

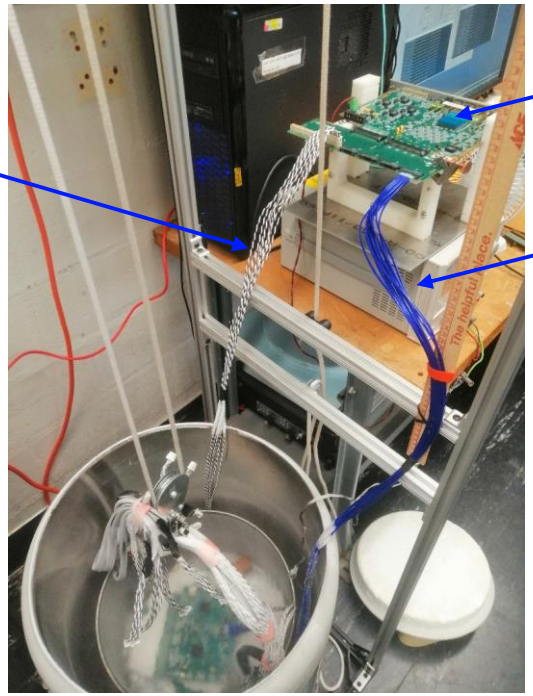


“LArASIC + ColdADC + FPGA” FEMB Regulators

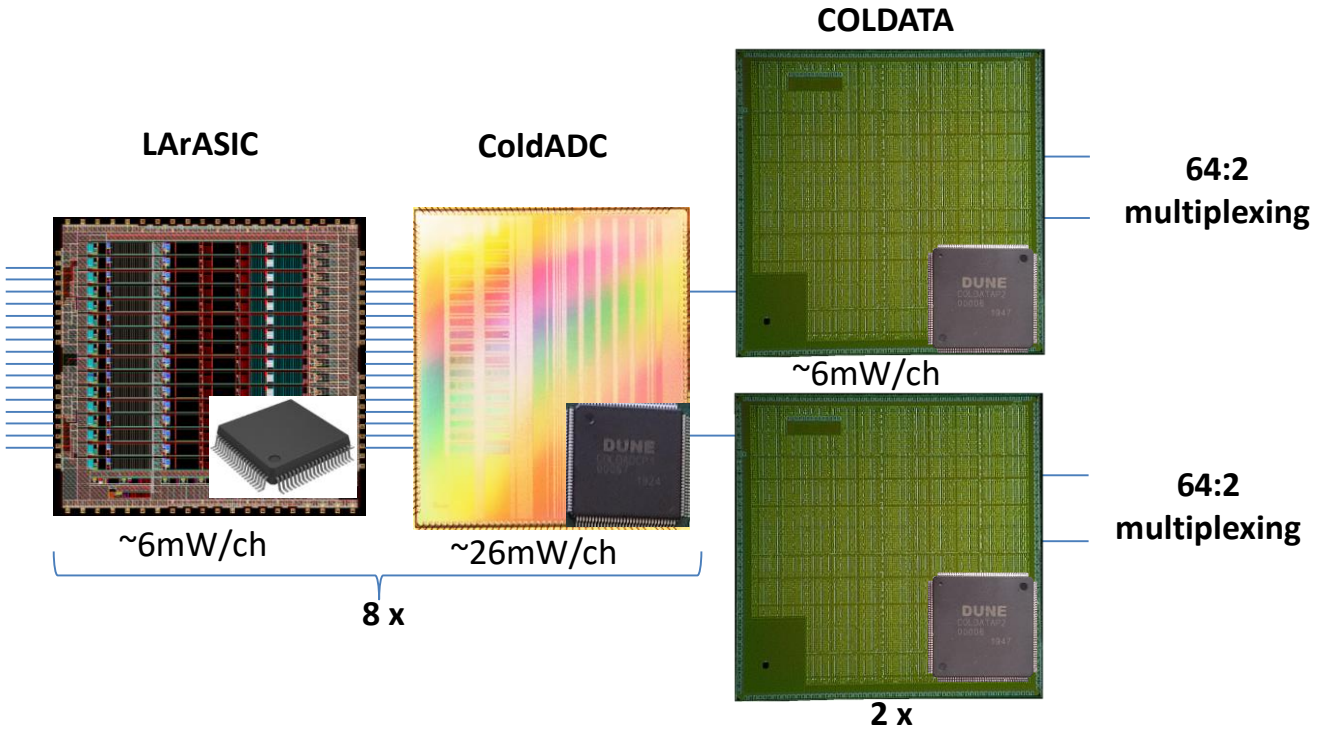


"LArASIC + ColdADC + dual FPGA" FEMB

Tested at both RT and LN



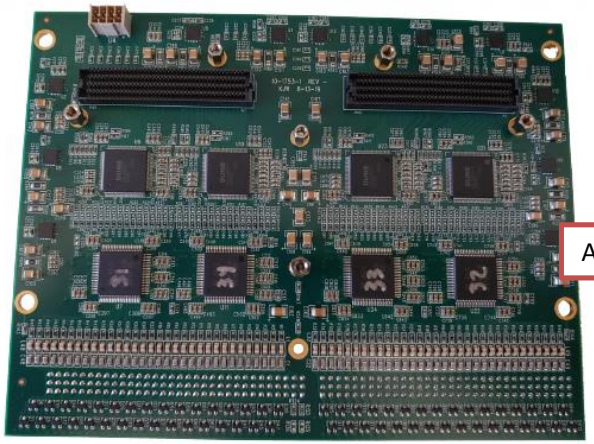
LArASIC + ColdADC + COLDATA



LArASIC + ColdADC + COLDATA

- Consists of two boards
  - COLDATA mezzanine -- 12 Layer PCB*
  - Analog Motherboard --10 Layer PCB
- COLDATA Mezzanine
  - Two COLDATA ASIC's
  - 2.8V, 2.0 & 5V bias over 3 pairs
- 128 channel DUNE Analog Motherboard (AM)
  - 8x ColdADC V1 chips
  - 8x LArASIC P2/P3 chips
  - Identical to FPGA version
  - POWER AM
    - 4.2V and 5V bias supply over 4 pairs (ProtoDUNE WIB)
    - 2.8V , 2.2V and 5V bias supply over 4 pairs (new DUNE WIB)
- ProtoDUNE WIB Firmware is not compatible with this FEMB
  - New firmware required
  - Resistors on ProtoDUNE WIB need to be moved and replaced
  - Configuration scripts will require an update

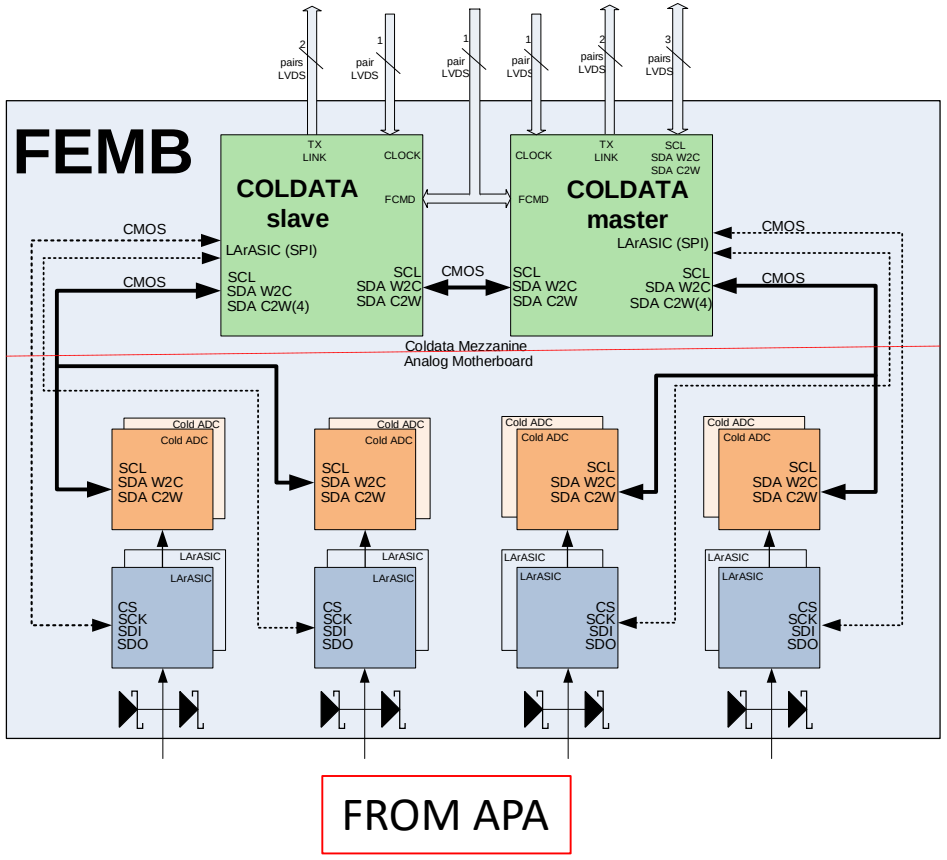
COLDATA Mezzanine (FM)



Analog Motherboard (AM)

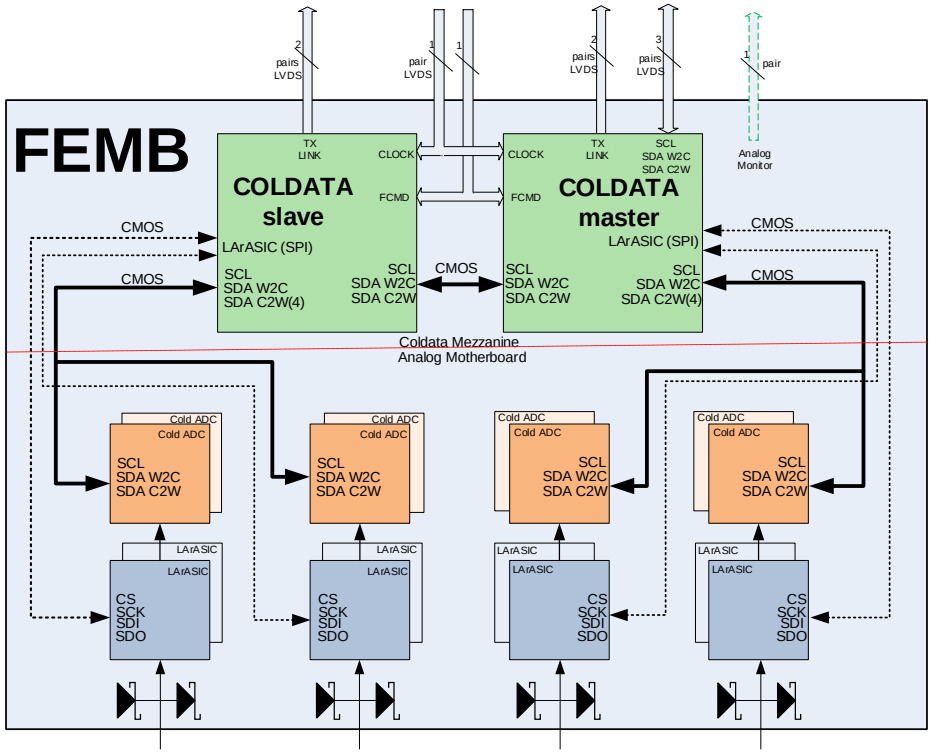
LArASIC + ColdADC + COLDATA

- Data Cable IO (10 Pairs)
  - 1.28Gb TX data link (4 pairs)
    - 2 for each COLDATA
  - I2C link (3 pairs)
    - SDA_W2C standard LVDS
    - SDA_C2W standard LVDS
    - SCL standard LVDS
  - 2 X 62.5MHz Clock
  - FAST COMMAND
    - Synchronous commands
- COLDATA Shared signal form WIB
  - Fast Command
- COLDATA I2C relay
  - COLDATA has a master slave topology the master COLDATA ASIC interfaces to the WIB using standard LVDS and relays the I2C link to the slave COLDATA and the eight ColdADC ASIC's
- Eight independent SPI links for LArASIC's four links per COLDATA



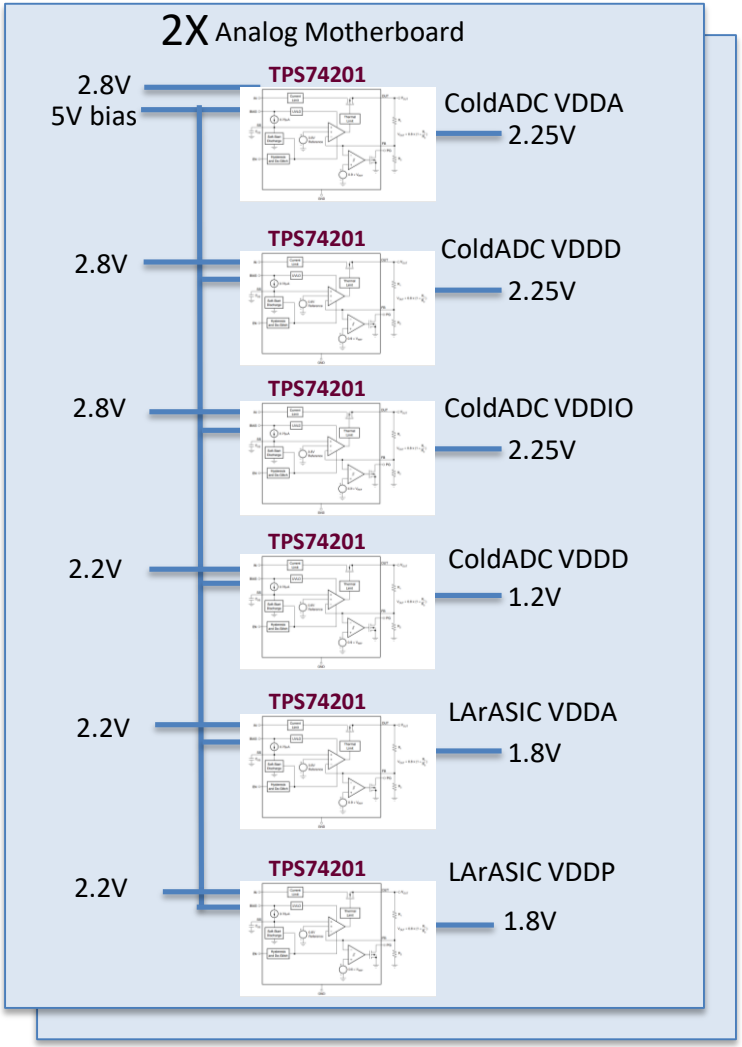
LArASIC + ColdADC + COLDATA

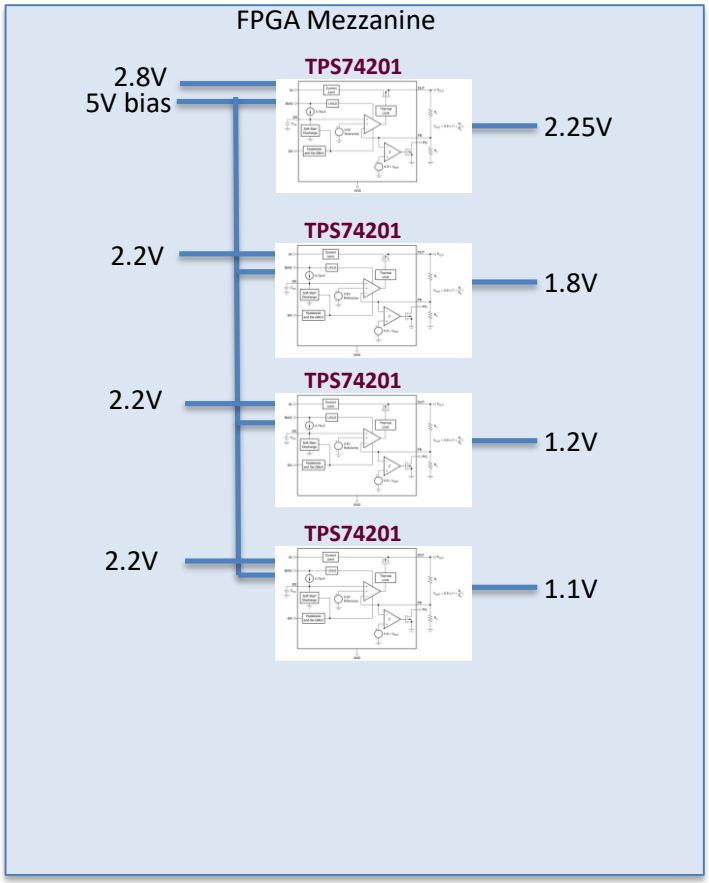
- Data Cable IO (10 Pairs)
  - 1.28Gb TX data link (4 pairs)
    - 2 for each COLDATA
  - I2C link (3 pairs)
    - SDA_W2C standard LVDS
    - SDA_C2W standard LVDS
    - SCL standard LVDS
  - 62.5MHz Clock
  - FAST COMMAND
    - Synchronous commands
  - ANALOG MONITOR
- COLDATA Shared signal form WIB
  - 62.5MHz clock
  - Fast Command
- COLDATA I2C relay
  - COLDATA has a master slave topology the master COLDATA ASIC interfaces to the WIB using standard LVDS and relays the I2C link to the slave COLDATA and the eight ColdADC ASIC's
- Eight independent SPI links for LArASIC's four links per COLDATA



FROM APA

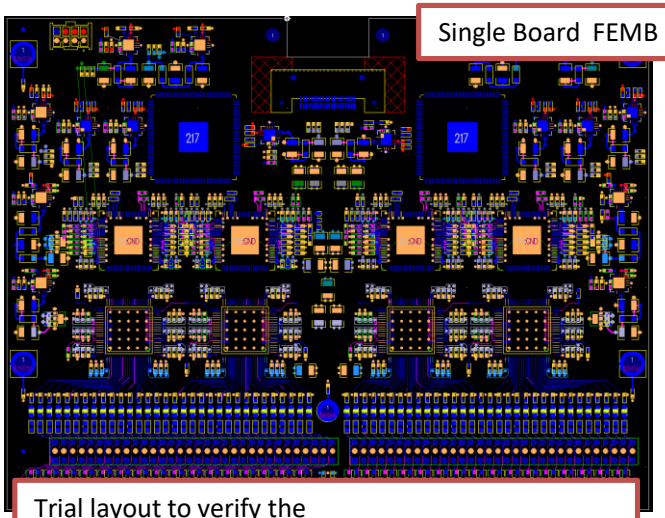
LArASIC + ColdADC + COLDATA Regulators





LArASIC + ColdADC + COLDATA Signal Board FEMB (SB FEMB)

- Single Board FEMB
  - Estimated layer count 12
- Two COLDATA ASICs
- 128 channel DUNE Analog Motherboard (AM)
  - 8x ColdADC V1 chips
  - 8x LArASIC P3/V4 chips
    - Both P3 and P4 versions are being explored SE VS DIFF
- Data and power cable scheme compatible to COLDATA mezzanine version
- Board dimensions are similar to previous FEMB
- New CE box enclosure is needed
  - Modify strain relief location
  - No modification of box dimension are required
- Trial layout to verify the feasibility, so far it is promising



ProtoDUNE Data Cable
DUNE Reduced Data Cable

ProtoDUNE Data Cable FPGA

Signal name	Type	# of Pairs
4xData Links	Differential	**4**
100MHz Clock	Differential	**1**
CMD Clock	Differential	**1**
I2C SCK	Differential	**1**
I2C SDA	Differential	**1**
TMS/RTN (JTAG)	SE	**1**
TCK/RTN (JTAG)	SE	**1**
TDI/RTN (JTAG)	SE	**1**
TDO-AM/RTN (JTAG)	SE	**1**
	Total Pairs	**12**

12 Twinax Pairs

DUNE Data Cable COLDATA

Signal name	Type	# of Pairs
4xData Links	Differential	**4**
62.5MHz Clock	Differential	**1**
Fast Command	Differential	**1**
I2C SDA out	Differential	**1**
I2C SDA in	Differential	**1**
I2C SCL	Differential	**1**
62.5MHz Clock OR Analog Monitor & RTN	Differential /SE	**1**
	Total Pairs	**10**

Proposed 10 Pair Cable

Currently in process to demonstrate that we can share the clock between the two ASICs

The pair count and or connector will be changed if we decide to go with 10 pairs of cable

ProtoDUNE Power Cable
DUNE Reduced Power Cable

LArASIC + P1 ADC + FPGA (measured at FEMB)

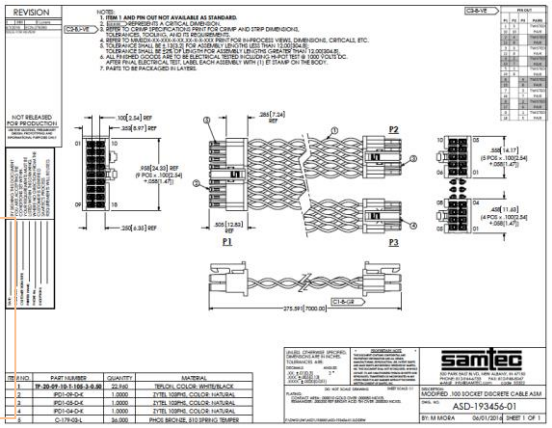
Signal name	Pairs	Measured Voltage (V)	Measured Current(mA)
BIAS FM/AM	2	5	28
3.6V for FM	1	3.54	62
2.8V for FM	1	2.78	368
1.5V for FM	1	1.49	513
2.8V for AM	3	2.17	1620
Monitor	1	-	-
Total	9		

Measurements done with ProtoDUNE 7M power cable on **FEMB side**

LArASIC + ColdADC + 2xFPGA (measured at WIB)

Signal name	Pairs	Measured Voltage / V	Measured Current /mA
BIAS FM/AM	2	5	32
3.6V for FM	1	4.2	61
2.8V for FM	1	2.89	635
1.5V for FM	1	1.71	418
4.2V for AM	3	4.24	1915
Monitor	1		
Total	9		

Measurements done with ProtoDUNE 7M power cable on **WIB side.**
NOTE: Values have not been optimized for voltage drop across cable

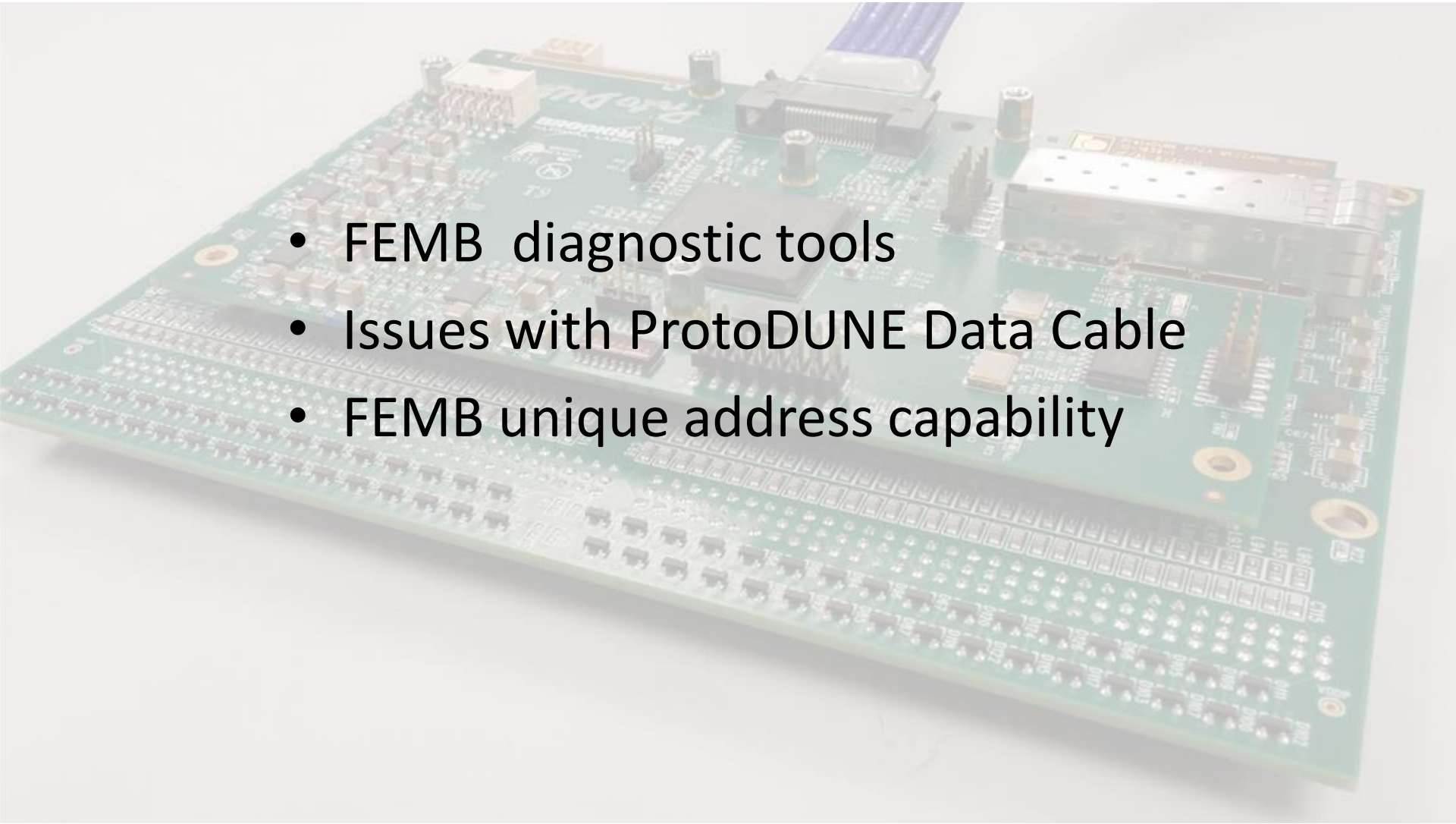


LArASIC + ColdADC + COLDATA

Signal name	Pairs	Estimated Voltage / V	Estimated Current /mA
BIAS CM/AM	2/1	5	32
2.8V for CdM	1	2.8	180
2.0V for CdM	1	2.0	105
2.8V for AM	3/4	2.8	1467
2.2V for AM	1	2.2	500
Total	8		

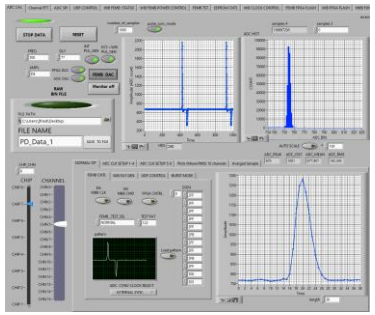
The pair count and or connector will be changed if we decide to go with 8 pairs of cable

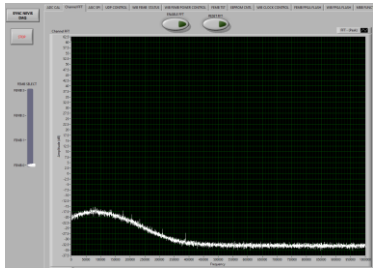
Lessons learned

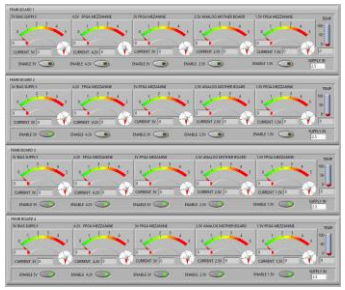


- FEMB diagnostic tools
- Issues with ProtoDUNE Data Cable
- FEMB unique address capability

ProtoDUNE CE Installation Diagnostic Tools

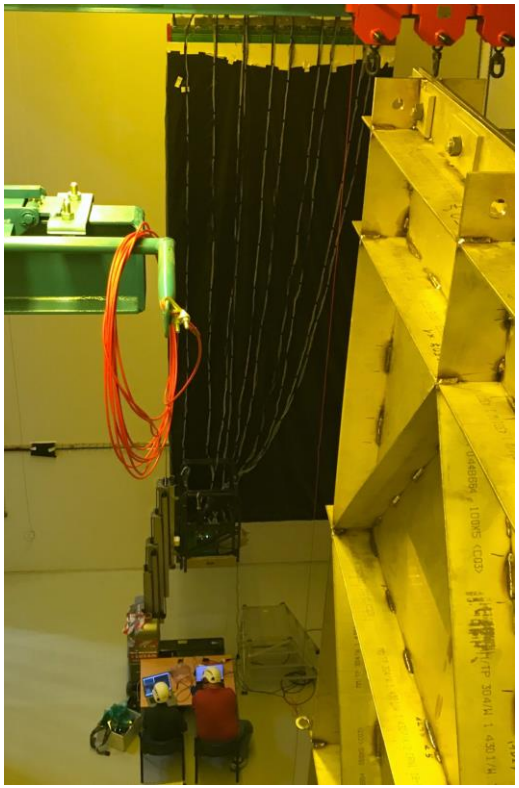






- Basic functionality test
  - Python & Labview
- Noise analysis
- APA wire connectivity / shorts

Manhong Zhao and Ken Sexton installing CE Box assemblies



Shanshan Gao and Jack Fried: noise tests

What was the dominant cause of FEMB failure during ProtoDUNE installation?

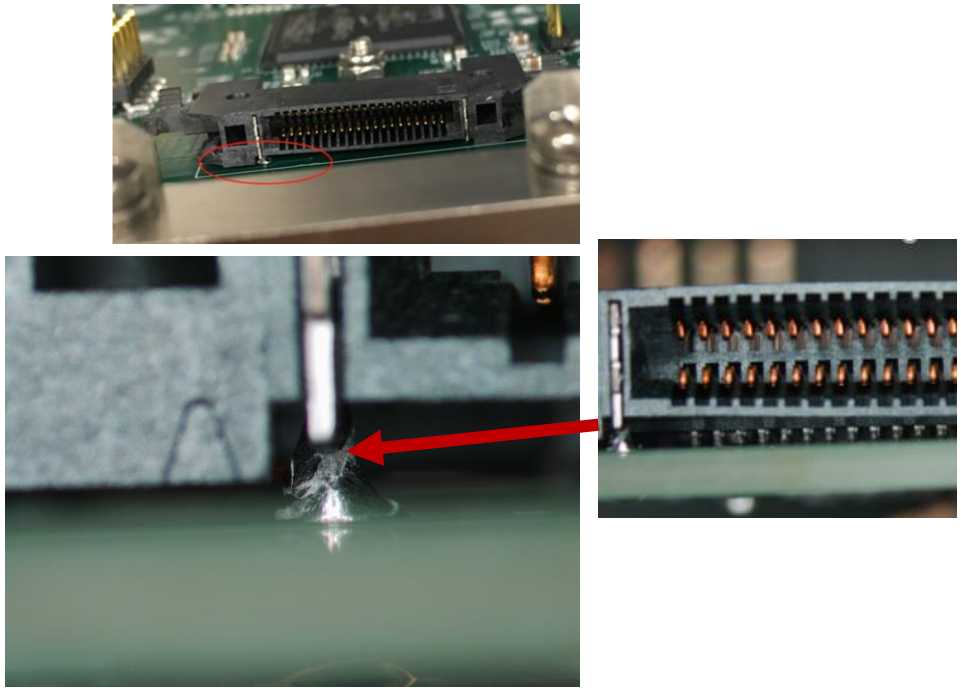
CE Boxes failures at CERN during installation

- Dominated by data cable connector issues

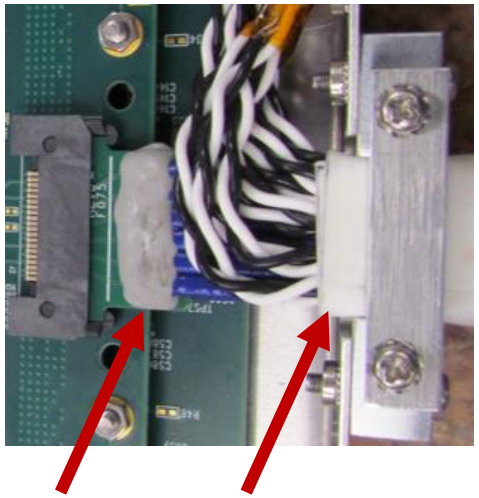
APA	CE Box Issue	Box IDs Replaced	Testing Stage Identified
1	1 dead FE channel at RT	009	QC at BNL
	1 LV return wire cut during cabling on APA	020	Installation
	3 dead FE channels at RT	024	Installation
2	Data cable connector failed	039	Cold Box
3	1 dead channel at RT	069	Installation
	Data cable connector failed	018	Cold Box
	Data cable connector failed	049	Cold Box
	Data cable connector failed	075	Cold Box
	1 FE ASIC (16 channels) failed during GN2 cooldown	022	Cold Box
4	1 dead channel at RT	091	Reception
	Data cable connector failed	085	Cold Box
5	2 links failed at RT in cold box	122	Cold Box
	Data cable connector failed	106	Cold Box
	Data cable connector failed	123	Cold Box
6	Data cable connector failed	112	Cabling
	Data cable connector failed	146	Reception

Connector Mechanical Stress

Inspection reveals damage to the data cable connector on the mezzanine

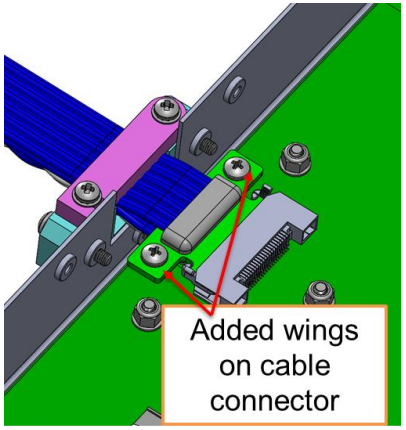


Cause for failure

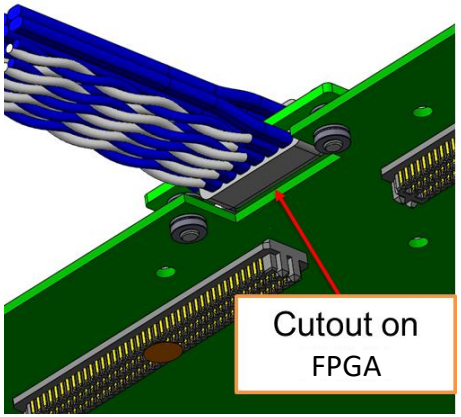


1: Uneven application of epoxy
2: Movement by Teflon sleeve

New Connector Design

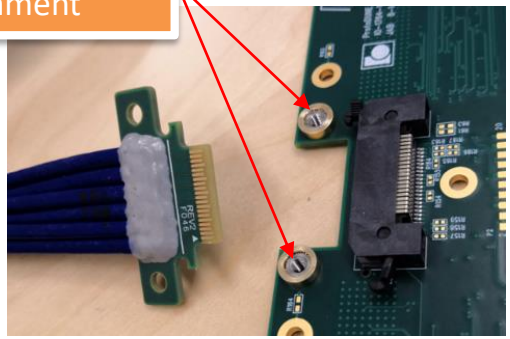


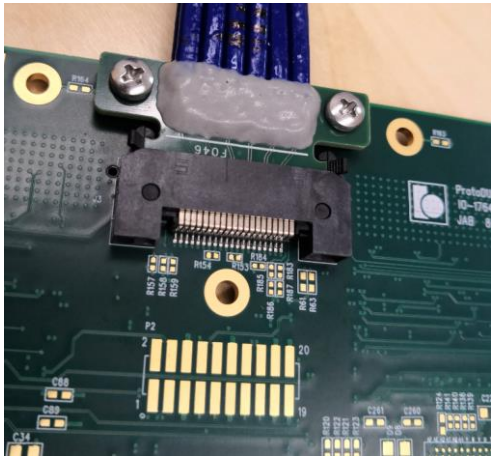
The printed circuit board on the cable connector is extended with two wings to secure the connector to the FPGA mezzanine board.



A small cutout added on the FPGA mezzanine board to accommodate the uneven application of epoxy on the cable connector.

Standoff to maintain perfect alignment





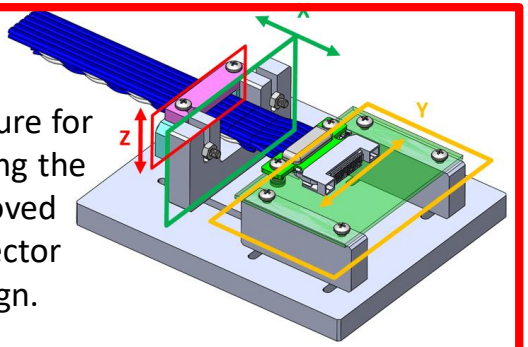
Data Cable Testing Procedure

A test setup is designed to verify the robustness of the redesigned connection. Misalignments of the connection along X, Y and Z directions can be realized by adjusting moveable parts of the test setup.

The redesigned connection has passed the mechanical fit check, all temperature cycling tests, liquid nitrogen immersion tests with misalignments from -1mm to +2mm in the Z direction and days at RT.

Temperature cycling in environmental chamber -65°C ~ 60°C

Liquid nitrogen cycling test



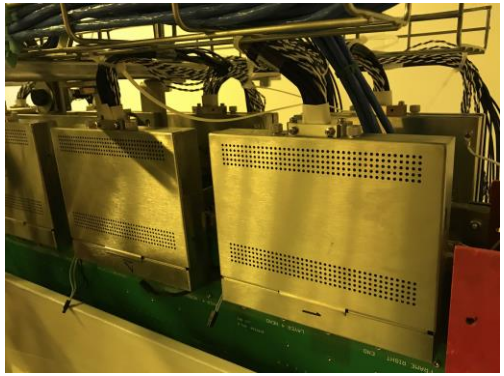
Test fixture for validating the improved connector design.

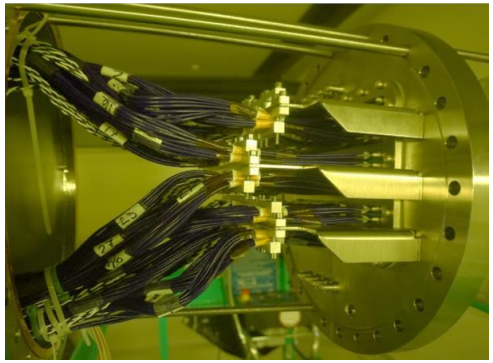
Summary of Test Result

Sample	Cable	Test Board	Misalignment	Temperature	Duration	Result
1	old	1	+2mm	RT	1.5 hour	PASS
					90 hour	FAIL
2	old	2	+1mm	RT	35 day	PASS
3	new	3	0	RT	25 day	PASS
				-65°C ~ 60°C	37 cycle	PASS
				LN ~ RT	10 cycle	PASS
4	new	4	+1.2mm	-65°C ~ 60°C	37 cycle	PASS
				LN ~ RT	10 cycle	PASS
5	new	5	+2mm	-65°C ~ 60°C	30 cycle	PASS
				LN ~ RT	10 cycle	PASS
6	new	6	-1mm	-65°C ~ 60°C	30 cycle	PASS
				LN ~ RT	10 cycle	PASS

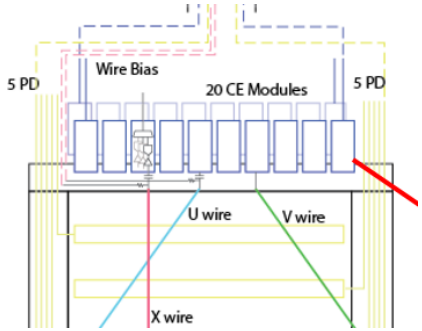
The redesigned connection has passed the mechanical fit check, all temperature cycling tests, liquid nitrogen immersion tests with misalignments from -1mm to +2mm in the Z direction and days at RT.

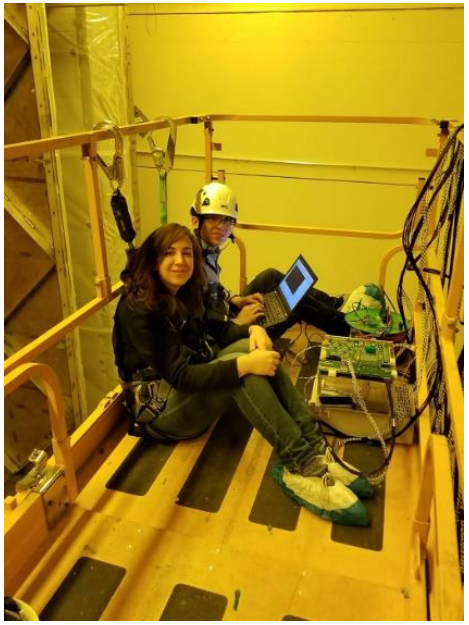
CE BOX APA address location



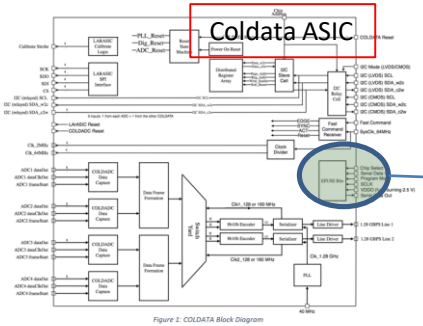


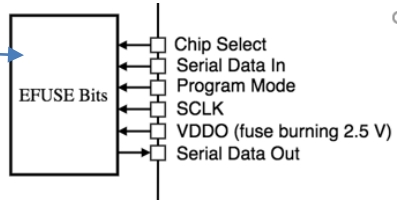
- Both the FPGA and COLDATA versions of the FEMB have a method to program a unique identifier
  - ProtoDUNE CE BOX APA address location programmed during install (portion of unused FPGA flash memory used)
  - COLDATA EFUSE bits are programmed during QA/QC
- CE BOX identifier values are recorded during installation to indicate its position on the APA
- Identifier values can be readout though the DAQ system to verify system cabling form APA to DAQ.

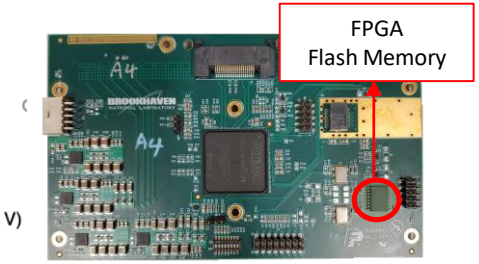




Block Diagram





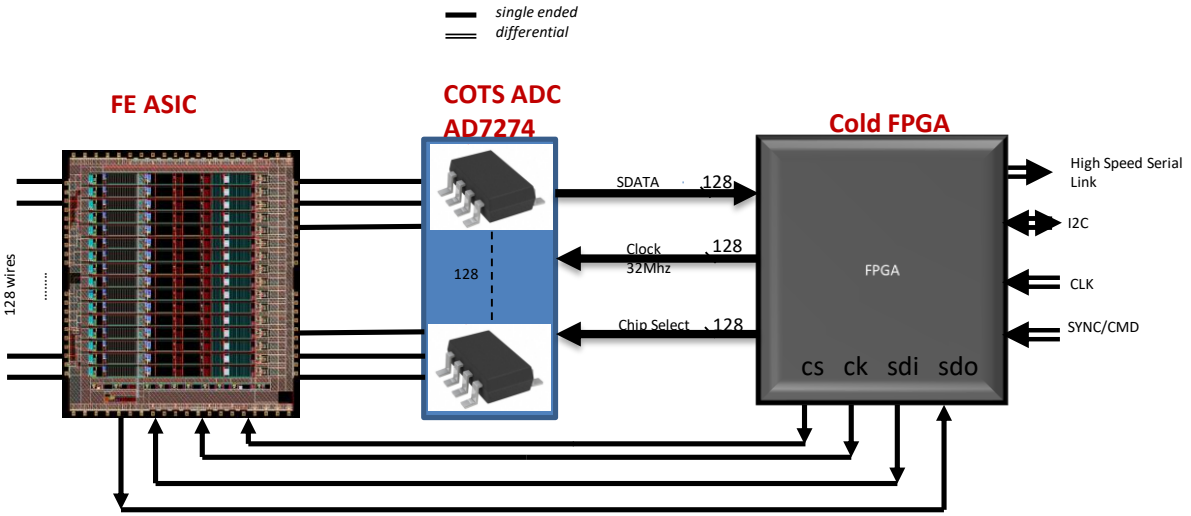


Summary

- ProtoDUNE FEMB
  - Running for over 1 ½ years with no failures after commissioning
- ColdADC + FPGA FEMB Prototype
  - Currently in production to be tested on AP7
- LArASIC + ColdADC + COLDATA
  - COLDATA mezzanine schematics are currently under development
    - Will be used to study FEMB clock scheme for data cable
  - Current study of a NON-Mezzanine version of FEMB are very promising

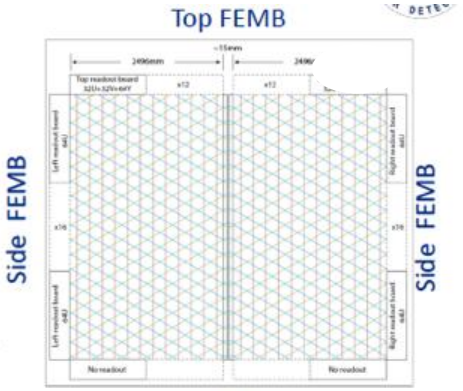
BACKUP

SBND FEMB Readout Chain



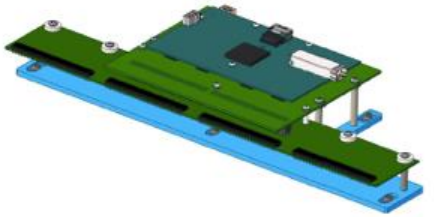
SBND Front End Mother Board Assembly

- 128 channels of digitized TPC wire readout
  - 88 assemblies for 11,264 SBND TPC channels
- Analog mother board (AM)
  - 8x 16-chn FE ASIC and 128x AD7274 chips
  - Side AM and Top AM
- FPGA mezzanine (FM)
  - multiplexing of digitized signals to 4x 1.28Gbps links
- Side FEMB Adapter board
  - Passive board with only mating connectors



Top AM

Side AM



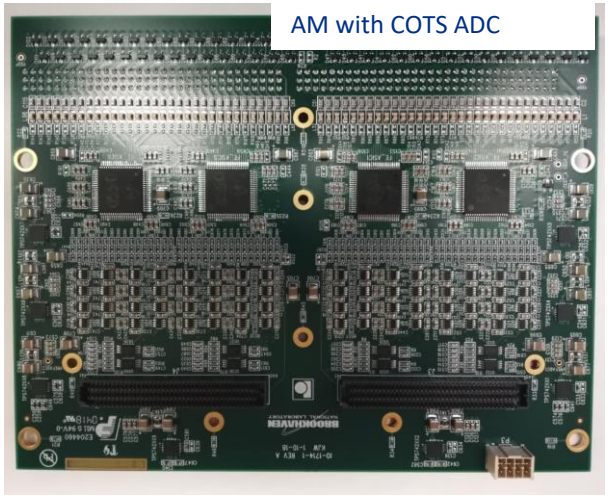
Side FEMB Adapter Board

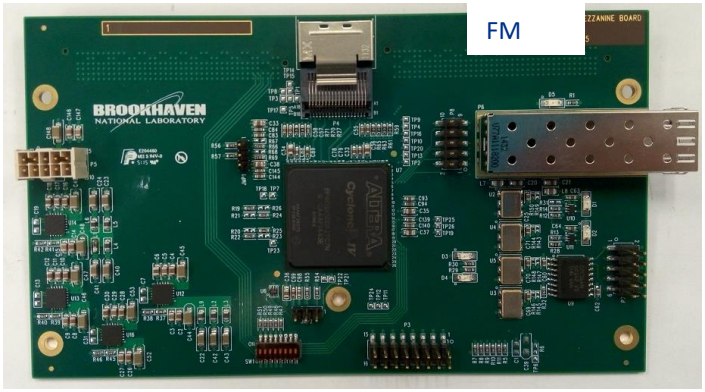
FPGA Mezzanine

SBND FEMB

AM: Analog Motherboard
- 8 FE ASICs
- 128 AD7274 chips
- 128 FE channels
- Cold regulators: TI TPS74201
  - 1.8V FE ASIC
  - 1.8V ADC reference
  - 2.5V ADC AD7274

FM: FPGA mezzanine
- Cyclone IV GX FPGA
- MiniSAS connector


AM with COTS ADC



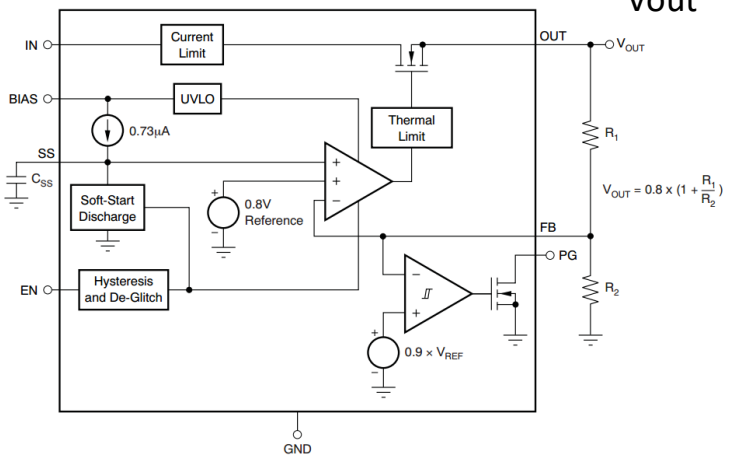
FM

Cold Regulator

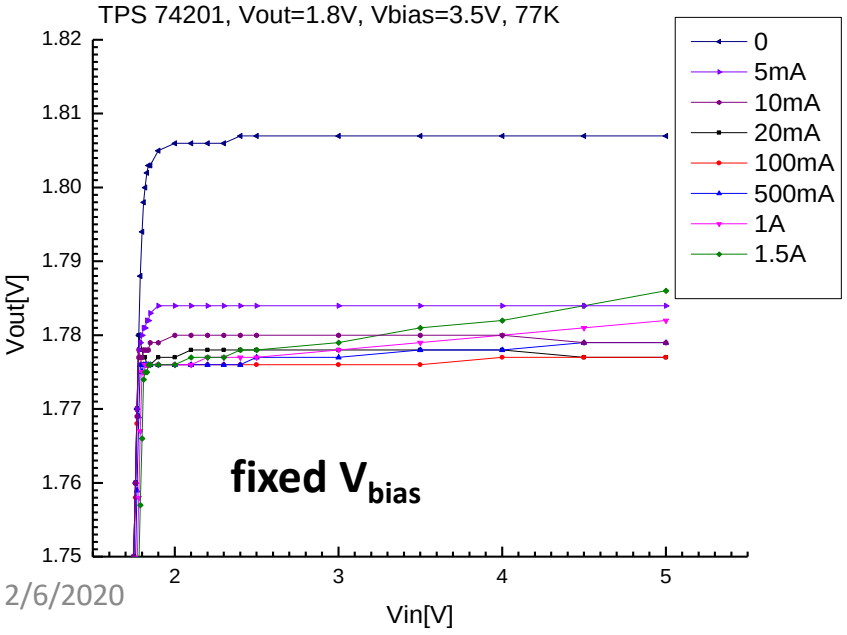
Vin

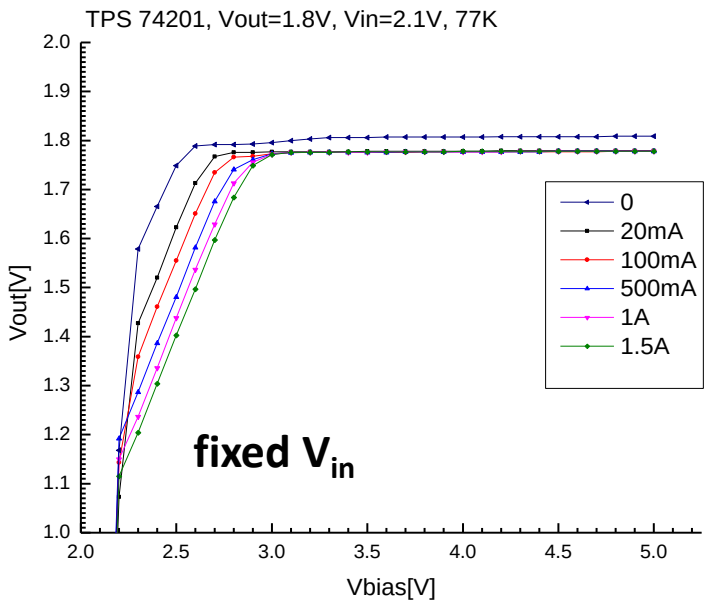
Vbias

TI TPS74201

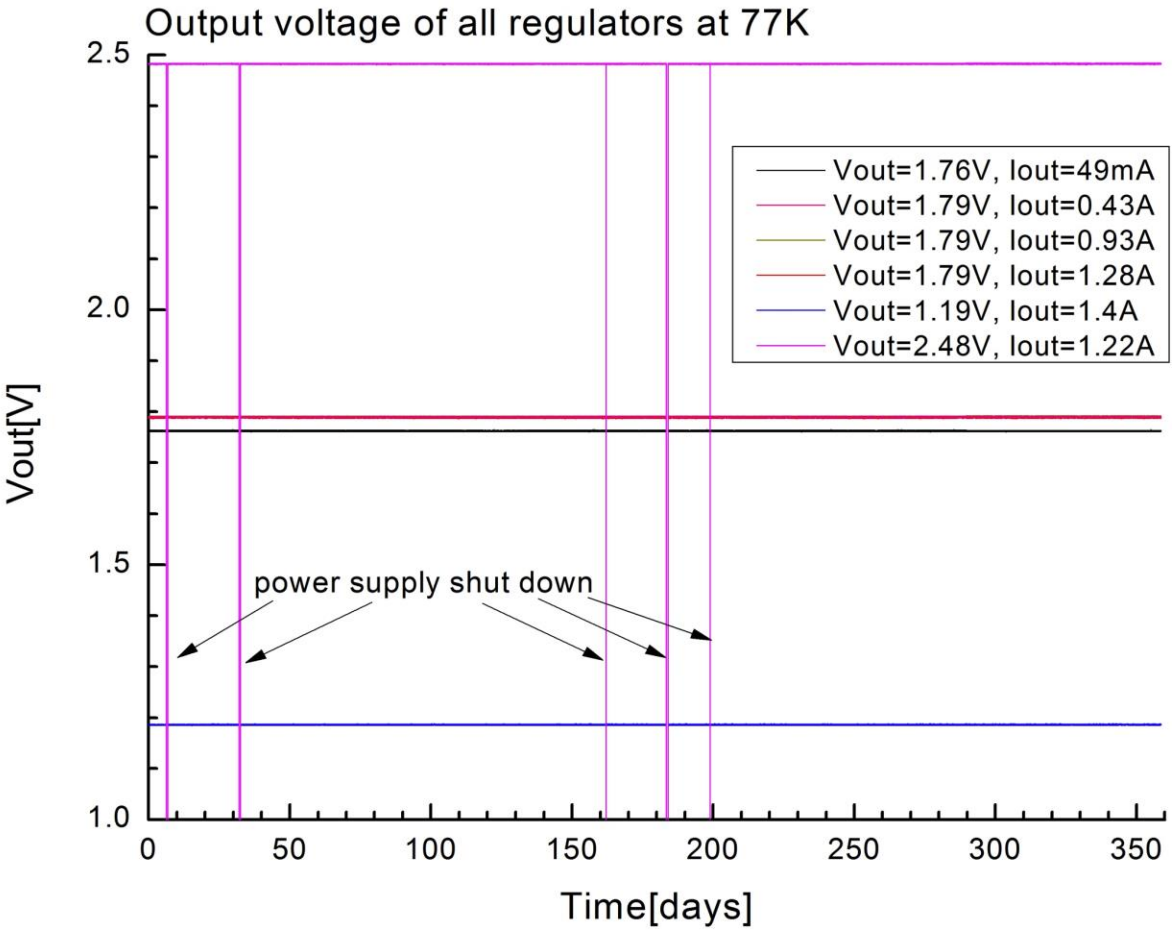


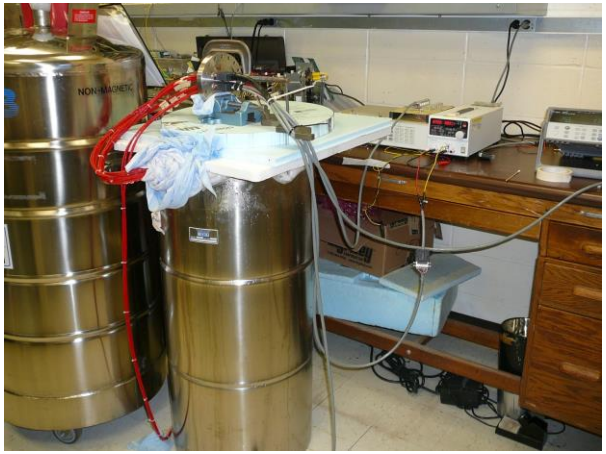
- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature
- .8V-5.5V V_{in}, 0.8V-3.6V adjustable V_{out}, 1.5A max I_{out}, and separate Vbias allows for a max 120mv dropout at 1.5A makes it is an ideal candidate for all of the cold electronics chain





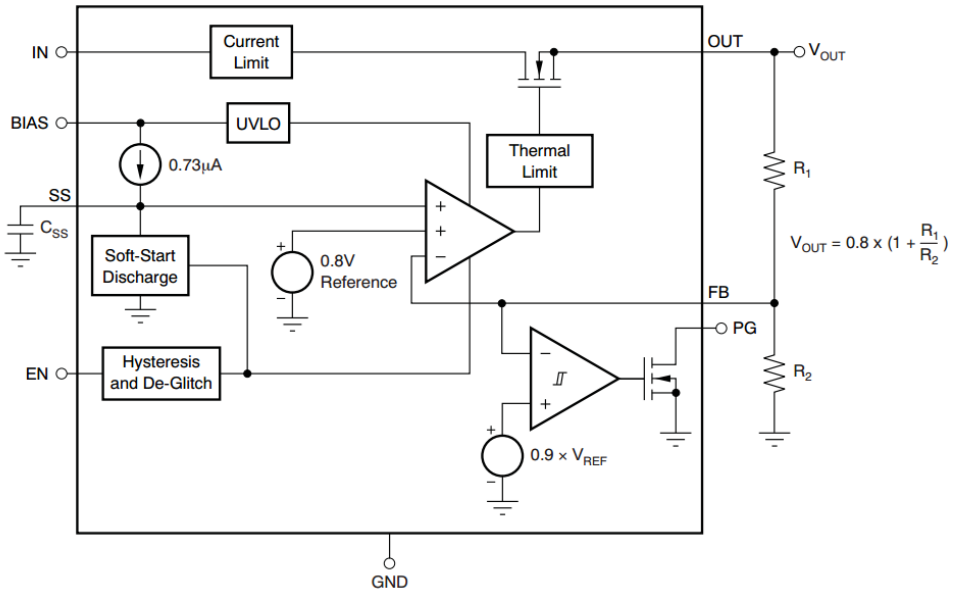
Cold Regulator – Lifetime testing

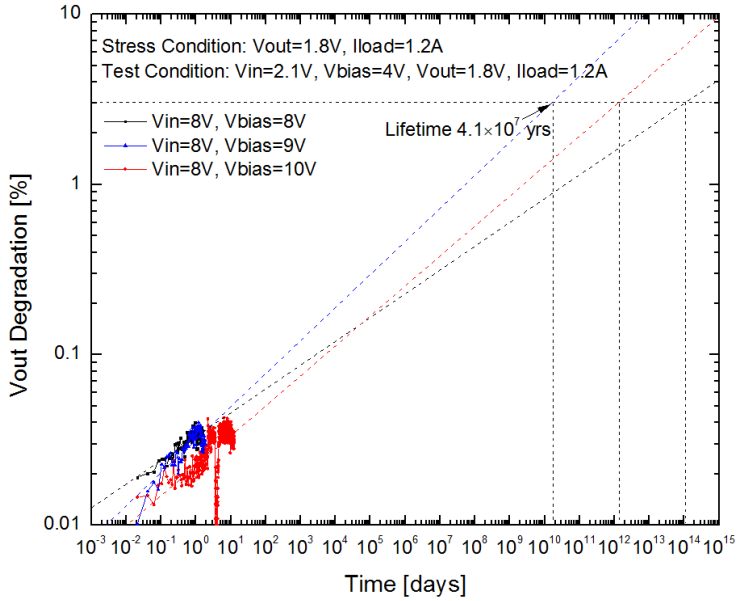




- A long term test of several **TPS74201 in LN2** has been going on **since June 24th, 2013**
- Voltage regulators are working normally for ~ 24 months, the test has been wrapped up in June 2015

Regulator Stress Test



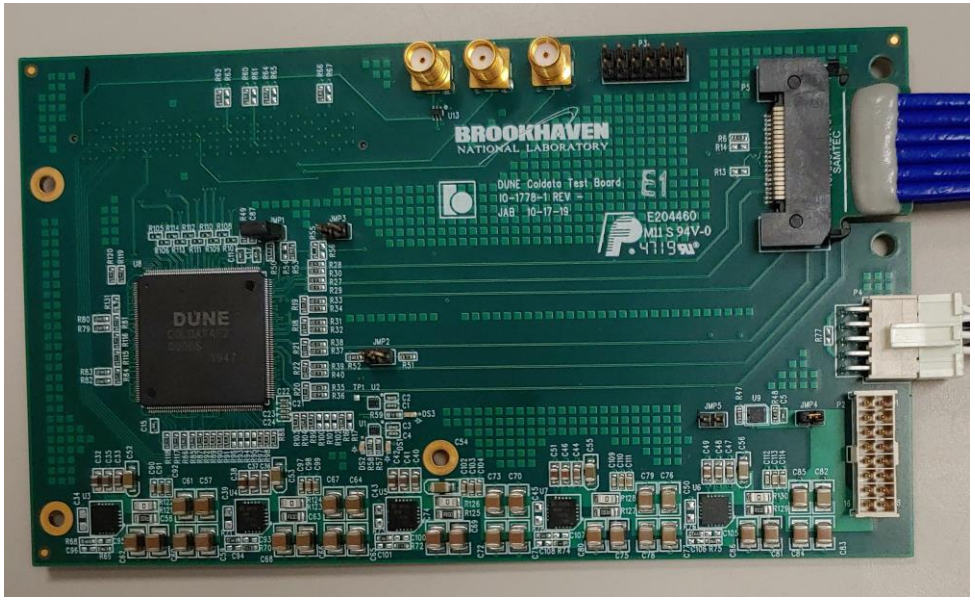


Block diagram of TPS74201 from the datasheet. Pin IN is the input voltage of the regulator while BIAS is the bias voltage for the internal logics. The absolute maximum voltage for both voltages is 5.5V.

Regulators are stressed under different voltages. For criteria of 3% degradation, the regulator under stress (Vin=Vbias=8V) exhibits a lifetime of more than 10^7 years. Therefore, the operation of the regulator under normal operation at 77K is not a concern.

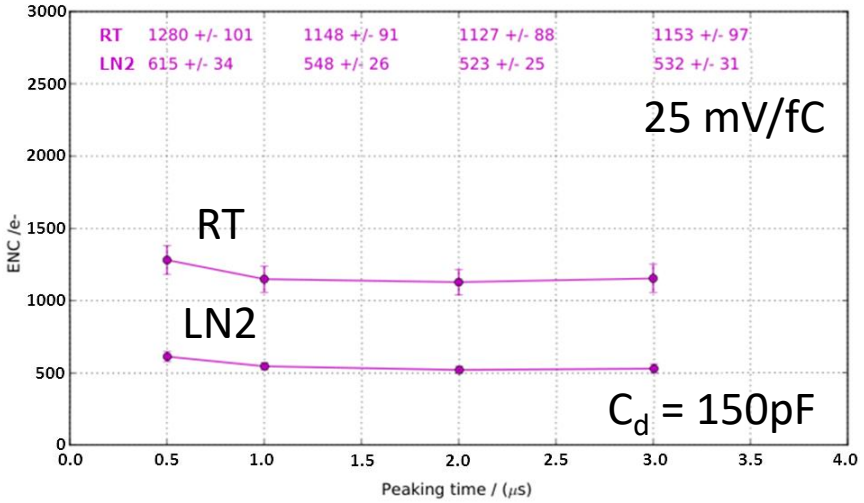
COLDATA ASIC Test Board

- Powered by WIB
- Verify WIB communication
  - 62.5MHz clock
  - Fast Command
  - I2C link
  - 1.28Gbs links
- Using ColdADC test board the COLDATA test board can communicate to one ColdADC and one LArASIC

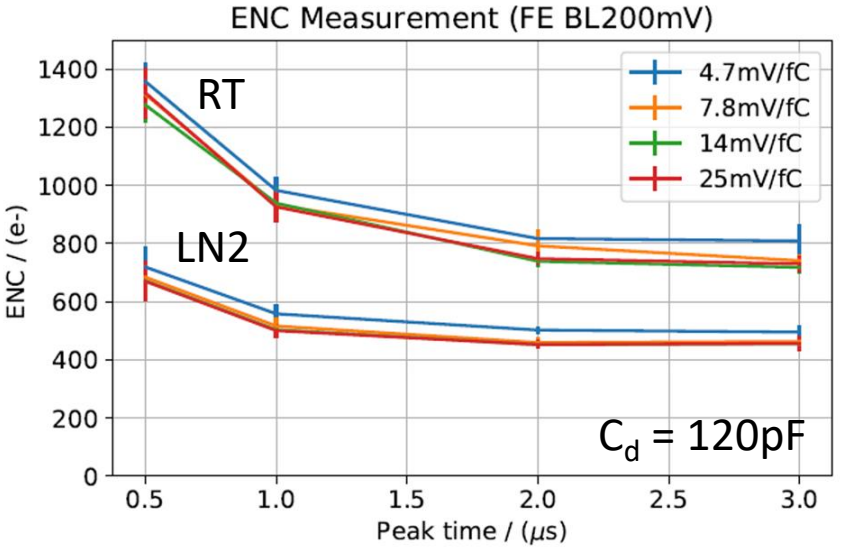


ENC Comparison

Noise performance is comparable.



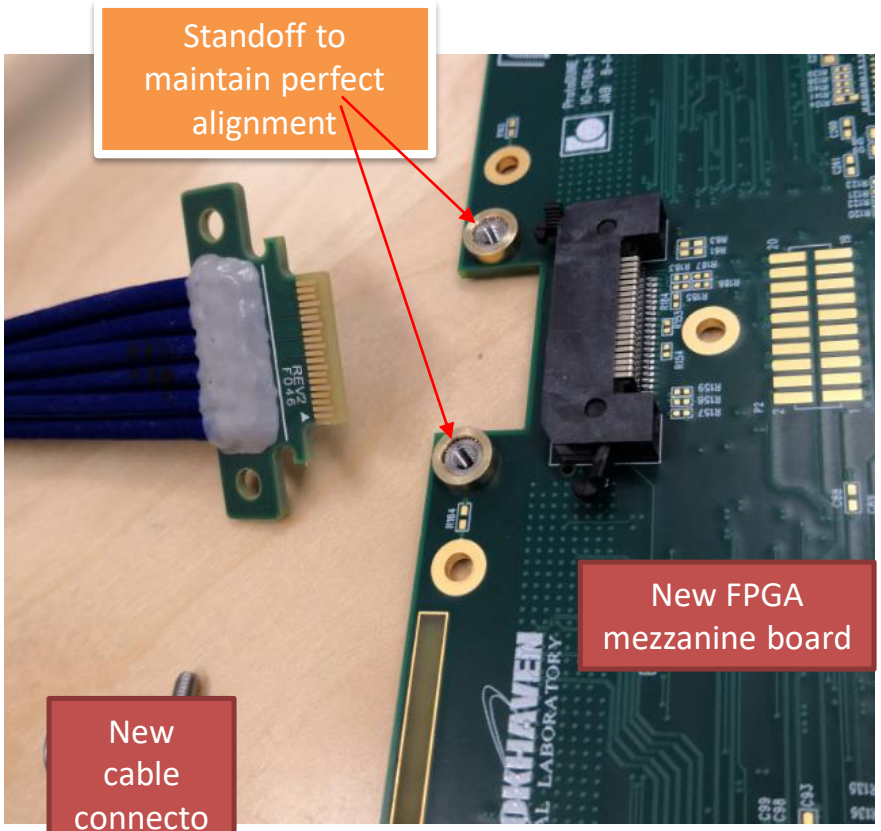
ProtoDUNE FEMB with FE + P1 ADC + FPGA

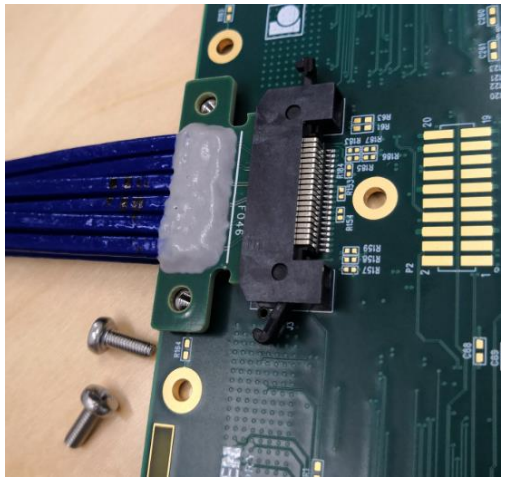


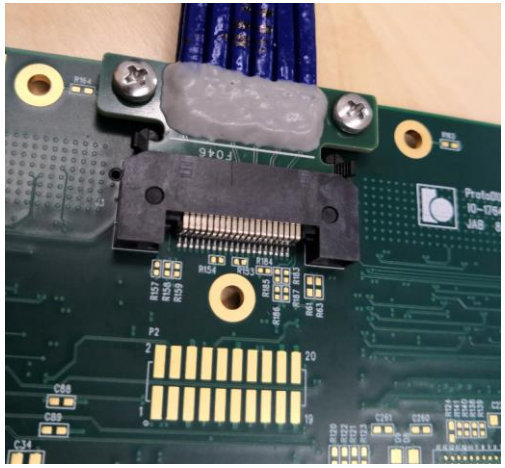
DUNE FEMB with FE + ColdADC + FPGA

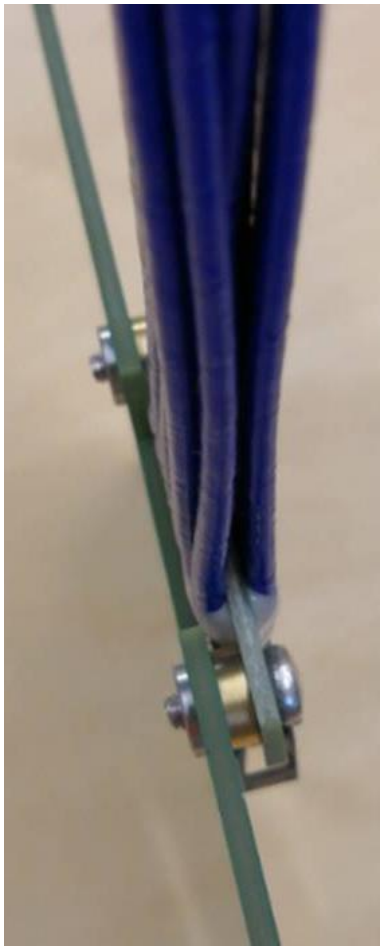
note: With protection diodes at FE inputs at room temperature, the leakage current of protection diode increase the noise. Since part numbers of protection diode for ProtoDUNE and DUNE FEMB are different, the ENC plots at room temperature looks different. At cryogenic temperature, the leakage current is minimized to the negligible level

Fit Check of Redesigned Connection

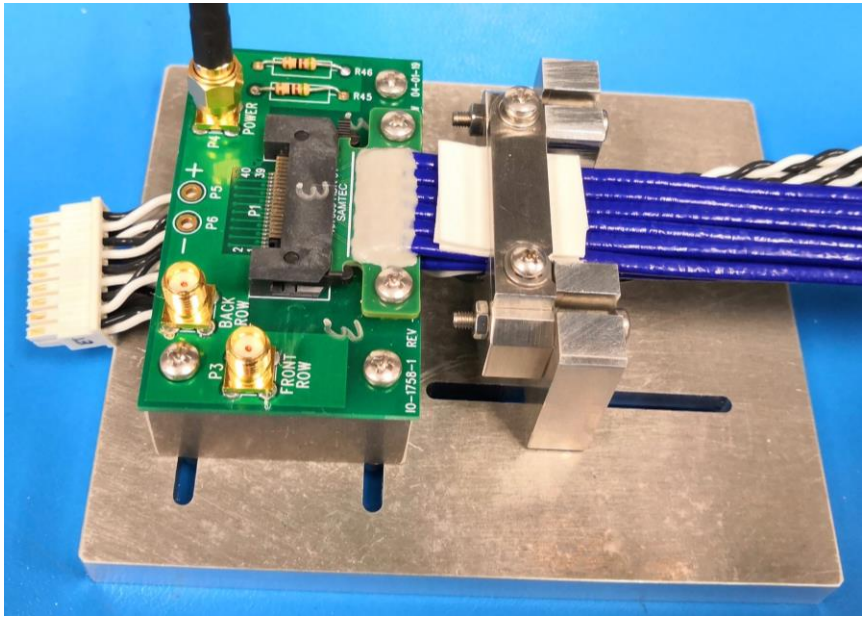




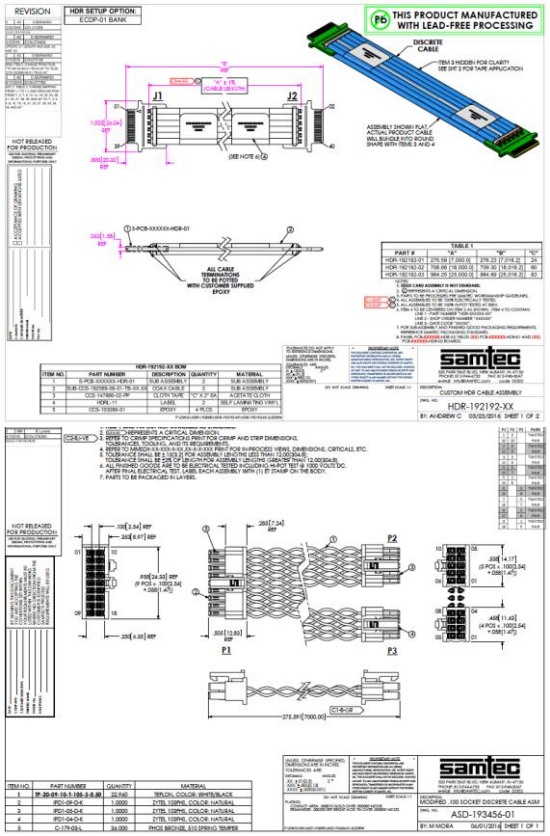




Qualification Tests
of
Redesigned Cold Control/Data Connection



Cold Cable



- 12 pairs of 26 AWG copper twin-axial cable from Samtec
  - Viable candidate for all lengths of cable required in DUNE FD
  - LAr compatibility test successful at Fermilab MTS
- Twisted pair 20AWG Teflon power cable from Samtec
- Small order placed for both data cable and power cable
  - Order will be received by August
- 8 weeks estimated lead time for final purchase (140 bundles)