DUNE Preliminary Design Review of ASICs and Front-End Motherboards Introduction

Marco Verzocchi

Fermilab

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Outline

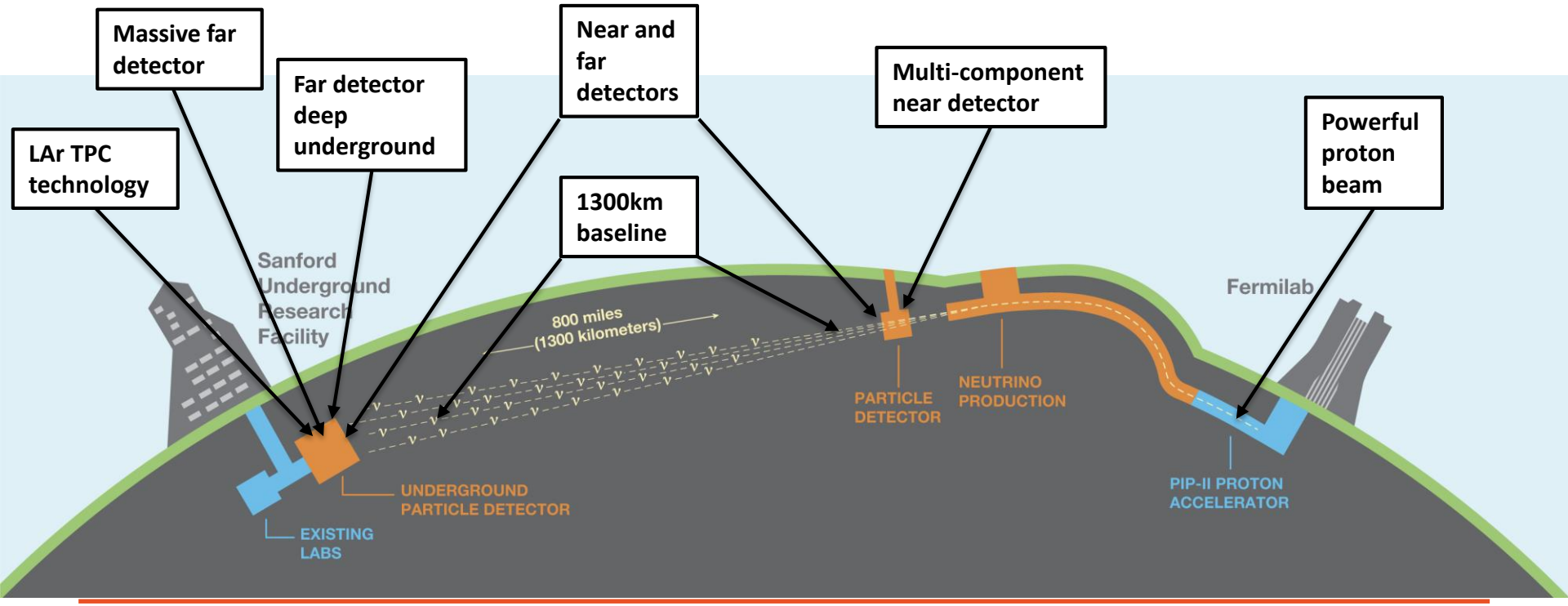
- Introduction to DUNE
- Electronics for the readout of the TPC
- Requirements for the front-end electronics
- Operating ASICs in liquid argon
- Goals of the review
- Agenda

Introduction to DUNE

- The DUNE experiment is being built with 3 main physics goals:
  - Precise measurements of neutrino oscillation parameters including study of CP violation in the neutrino system (i.e. differences in oscillation parameters between neutrinos and antineutrinos)
    - Possible source for matter – antimatter asymmetry in the universe
  - Search for proton decay
    - Physics beyond the standard model / grand unification
  - Observation of neutrinos from supernova explosion
    - Get a time-lapse movie of the stellar collapse
- Requirements for experiments of this kind
  - Large sensitive mass, long baseline and intense neutrino source, underground
  - Two technologies: water Cerenkov (HyperK, Japan), liquid argon TPC (DUNE)

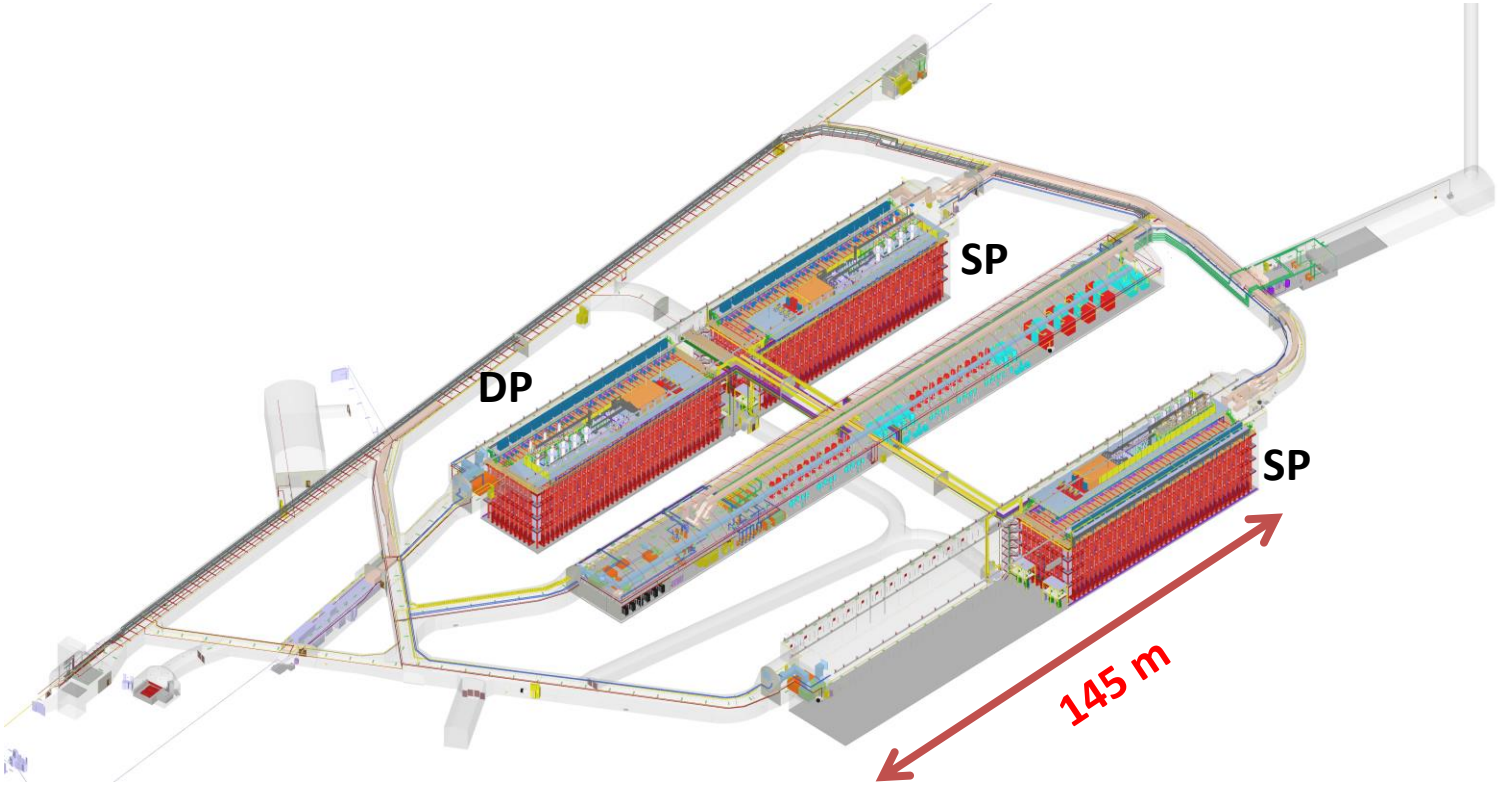
Introduction to DUNE

- LBNF is the facility (beam from Fermilab to South Dakota, near and far site caverns, infrastructure, cryostats)
- DUNE is the experiment (liquid argon time projection chamber)



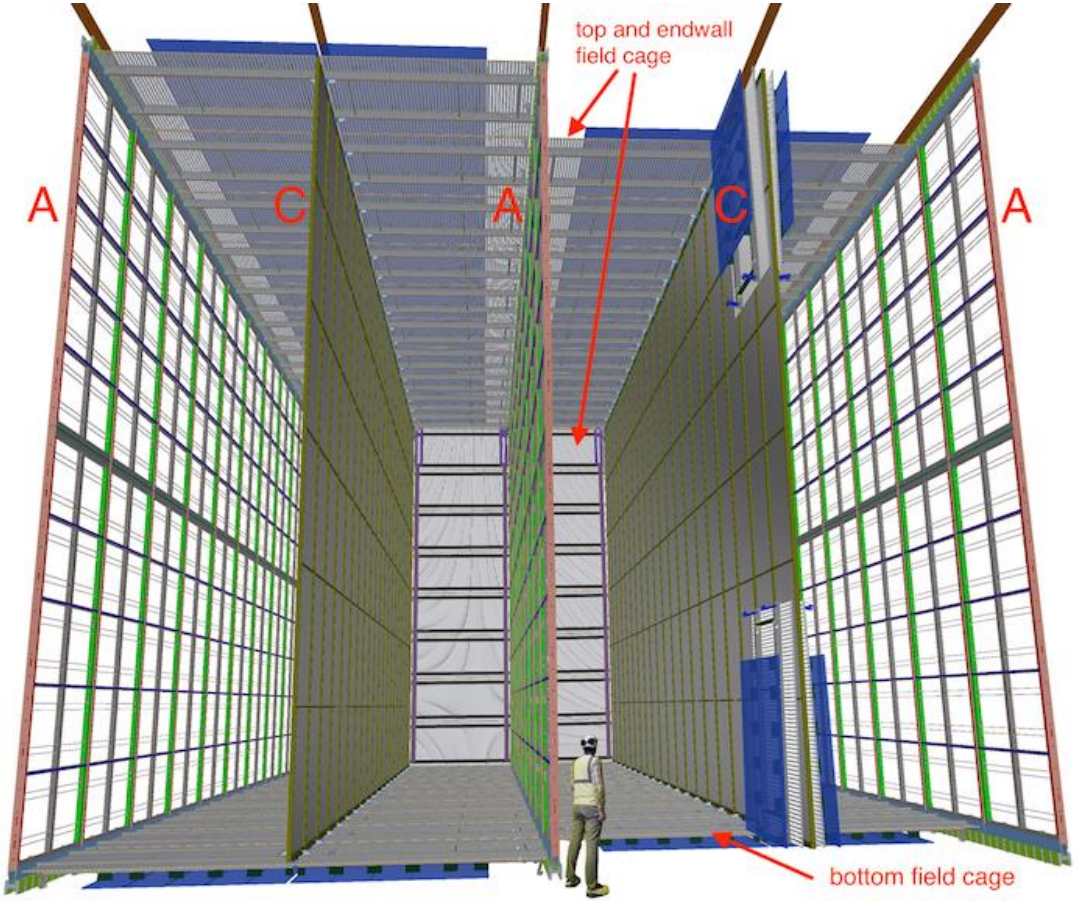
Introduction to DUNE

- Four separate 17 kt (> 10 kt fiducial) LAr TPCs
- 4 identically sized cryostats: 2 single phase (SP) + 1 dual phase (DP) +1 “opportunity” (this 2+1+1 plan is described in TDR)



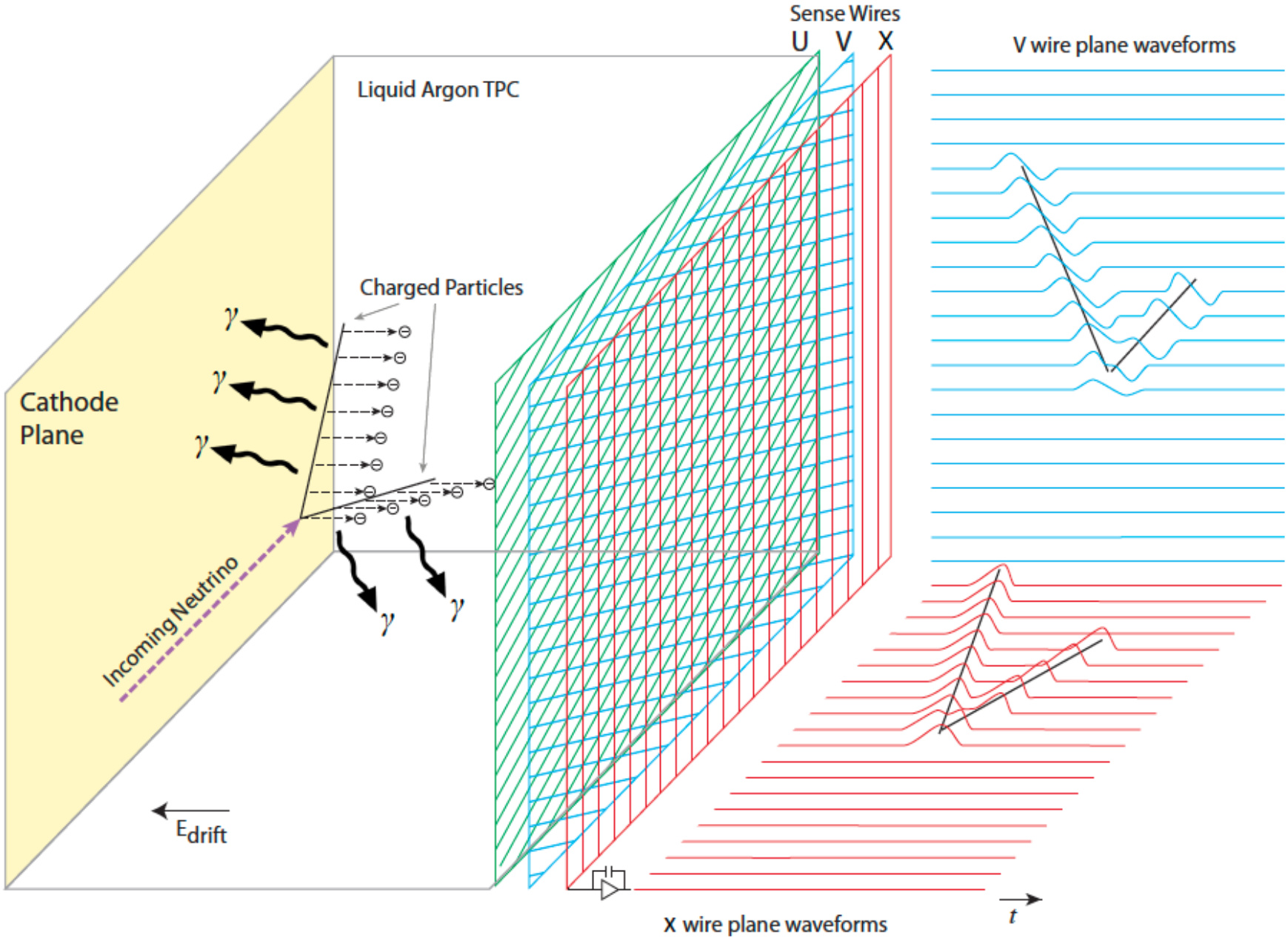
Introduction to DUNE

- Single phase detector:
- 4 drift volumes of 3.5m
- Read out by a total of 150 anode plane assemblies (APAs), each with 2560 wires
- 128 channels per front-end motherboard (FEMB), 20 per APA
- Total of 384k readout channels, 3000 FEMB total



Signal formation

- Wires organized in multiple readout planes (U, V, X) to allow for 3d reconstruction of ionization from tracks, unipolar signal (negative) on collection wires (X), bipolar signal (first negative then positive) on induction wires (U,V) as electron cloud travels past the wires
- Signal duration o(μs), narrower for collection plane
- 20-30k e^- collected on the X wires for ionization from MIP near the cathode (3.5m distance, assume drift field 500 V/cm, 6 ms electron lifetime in Ar)
  - Limited by immediate recombination (30%), losses caused by recombination along the drift distance (depends on drift field and argon purity)
- No amplification in liquid


Sense Wires
U V X
V wire plane waveforms
Liquid Argon TPC
Charged Particles
Cathode Plane
γ
γ
γ
γ
γ
Incoming Neutrino
E drift
X wire plane waveforms
t

Requirements on FE electronics

- Low noise
  - Compensate for possible reduced drift field, shorter lifetime
  - Requirement: equivalent charge noise (ENC) < 1000 e^-
    - Consistent with having S/N>10 on the collection wires even if the drift field and electron lifetime are both reduced by factor 2
    - Asymmetric requirements applied for S/N in pattern recognition (lower on induction wires)
  - Goal: ENC as low as possible
    - S/N>15 allows for reconstruction of MeV scale photons (target nucleus de-excitation, final state neutrons)
    - May open path to using ^{39}Ar decays for calibration purposes
    - Improves reconstruction / data compression

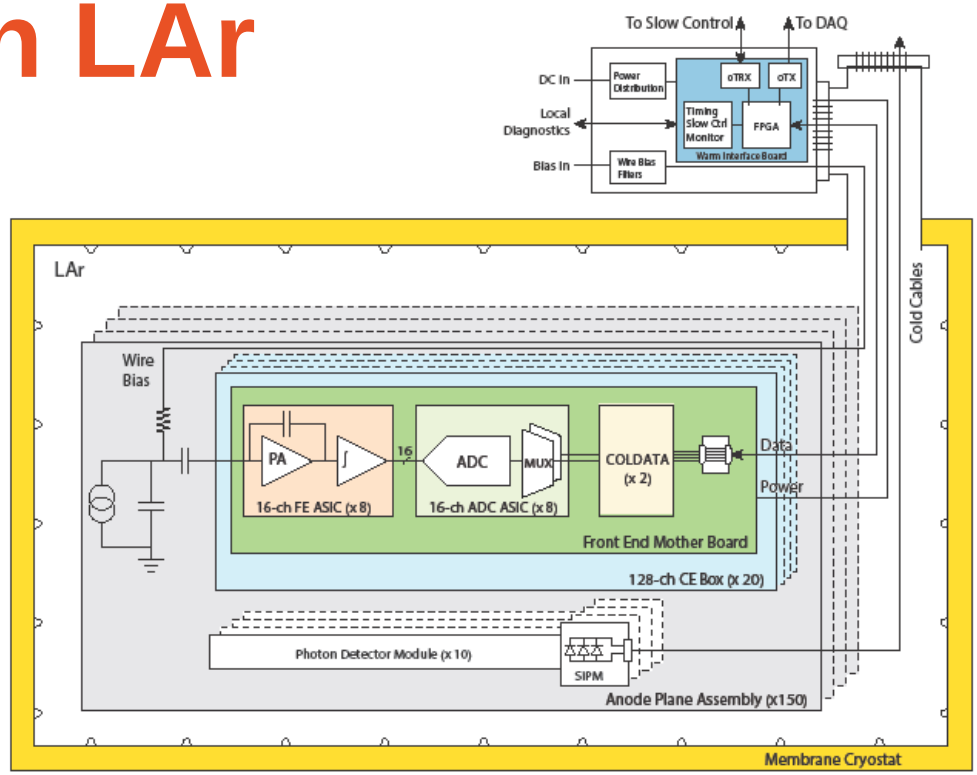
Requirements for the electronics

Label	Description	Specification (Goal)	Rationale	Validation
SP-FD-2	System noise	$< 1000\ e^-$	Provides >5:1 S/N on induction planes for pattern recognition and two-track separation.	ProtoDUNE and simulation
SP-FD-13	Front-end peaking time	1 µs	Vertex resolution; optimized for 5 mm wire spacing.	ProtoDUNE and simulation
SP-FD-14	Signal saturation level	500,000 e^- (Adjustable so as to see saturation in less than 10 % of beam-produced events)	Maintain calorimetric performance for multi-proton final state.	Simulation
SP-FD-19	ADC sampling frequency	$\sim$ 2 MHz	Match 1 µs shaping time.	Nyquist requirement and design choice
SP-FD-20	Number of ADC bits	12 bits	ADC noise contribution negligible (low end); match signal saturation specification (high end).	Engineering calculation and design choice
SP-FD-21	Cold electronics power consumption	< 50 mW/channel	No bubbles in LAr to reduce HV discharge risk.	Bench test
SP-FD-25	Non-FE noise contributions	$<< 1000\ e^-$	High S/N for high reconstruction efficiency.	Engineering calculation and ProtoDUNE
SP-FD-28	Dead channels	< 1 %	Minimize the degradation in physics performance over the > 20-year detector operation.	ProtoDUNE and bench tests

Minimizing noise

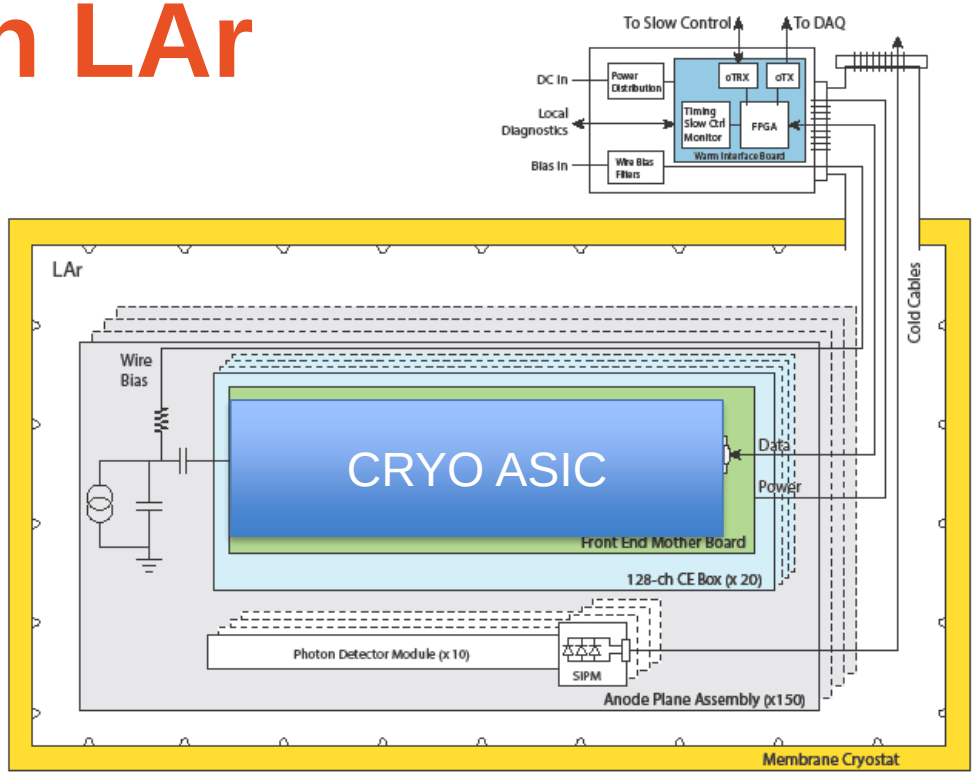
- Place FE electronics inside liquid argon
  - Charge carrier mobility higher, thermal fluctuations lower compared to room temperature
  - Higher gain, lower noise at LAr temperature
- Place FE electronics as close as possible to the wires
  - Minimize input capacitance, further contributes to noise reduction
- Digitize and serialize signals inside the LAr
  - Minimize need for cable penetrations, reduce number of required cryostat penetrations and of cables exiting the cryostat
- Careful design (and implementation) of grounding scheme
  - not for discussion in this review

Electronics in LAr



- Baseline solution has 8 front-end ASICs (LArASIC) on each FEMB (24k total), plus 8 digitizers (ColdADC, 24k total), and 2 data serializers (COLDATA, 6k total) on each FEMB
  - LArASIC / ColdADC: 16 wires per ASIC
  - COLDATA: handles data from 64 wires

Electronics in LAr

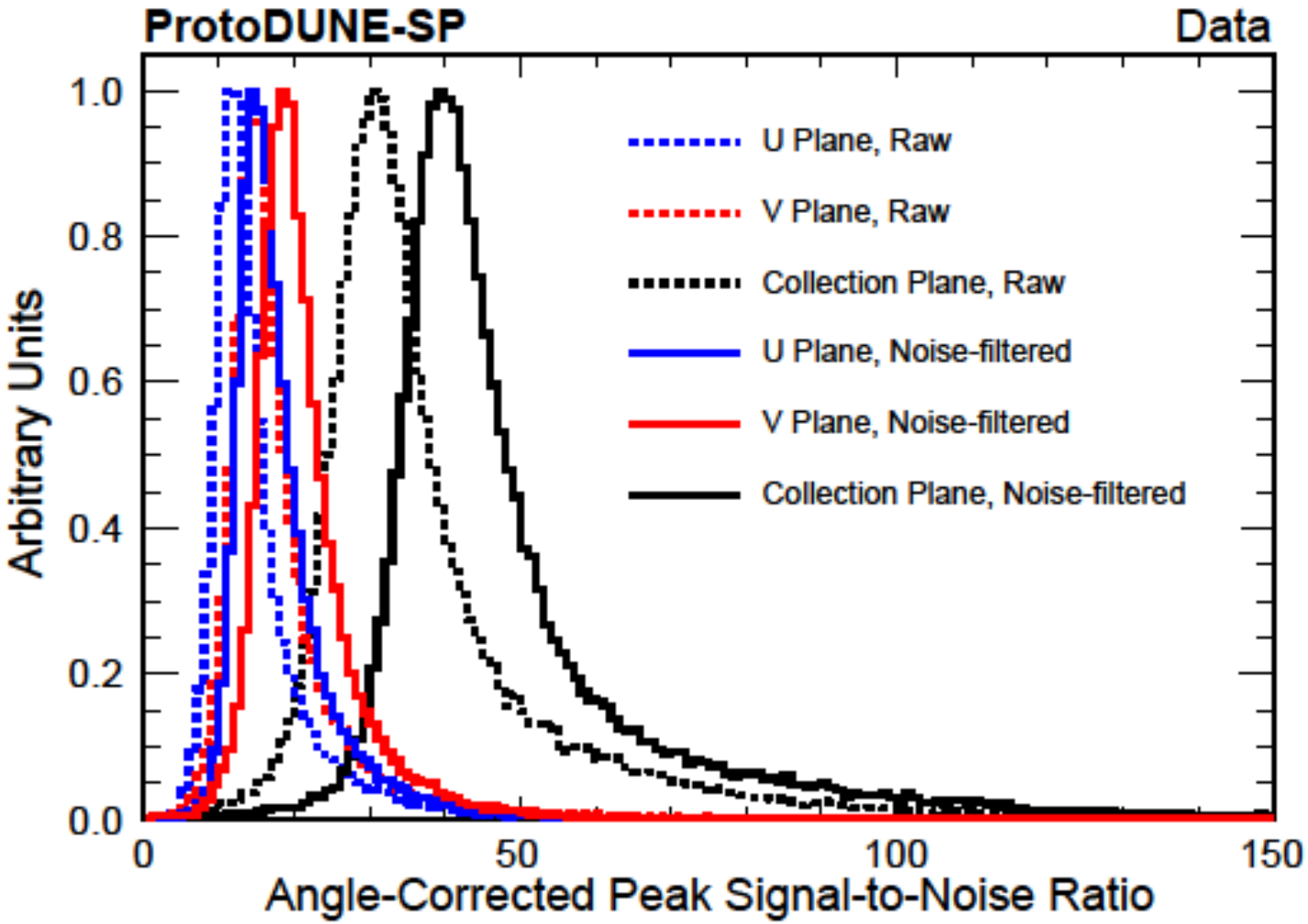


- We are also considering an alternative where the FEMB houses two CRYO ASICs: CRYO development originally planned exclusively for nEXO experiment
- CRYO handles the data from 64 channels, only 2 chips needed on each motherboard

Experience

- BNL group of DUNE has pioneered the development of ASICs to be operated in LAr, starting from FE amplifier
- Already deployed successfully in microBoone, reached noise levels of O(500 e^-)
- ProtoDUNE-SP and SBN detector are the first example where also the digitization and data serialization take place inside the LAr
- Excellent results from ProtoDUNE-SP despite some known limitations of current generation of ASICs
  - Saturation in the FE amplifier
  - Poor yield in the QC process and stuck codes in the ADC

ProtoDUNE results



ASIC operation in LAr

- Higher carrier mobility helps with performance, but also leads to hot-carrier effect that limits ASICs lifetime (faster aging)
- To mitigate hot carrier effect maximum E field in transistor channels must be smaller than typical one at room T
- To this effect operate transistors at lower voltage for the technology used and increase length of transistor channels
- Transistor models obtained from measurements at LN2 temperature used for designs in 65 nm and 130 nm
  - We are working on obtaining models of the same quality for 180 nm technology but we are fighting against legal issues (NDAs)

Why are we having this review ?

- New generation of ASICs under development for DUNE
  - Replace P1 ADC “domino architecture” with completely new design (ColdADC), new architecture
  - In ProtoDUNE use FPGA for data serialization, replace with COLDATA to ensure long term reliability
  - Further improve LArASIC (and address saturation issues observed in ProtoDUNE)
- In parallel the Long Baseline Neutrino Committee recommended that we pursue alternative solution(s) in case some of these developments were not successful
  - 3-in-1 CRYO ASIC
  - FEMB based on COTS ADC (used in SBND, single channel, now abandoned given good results from 1st generation of prototype)

Current Status

- 1st generation of prototypes for DUNE submitted between October 2018 and and April 2019
- Standalone tests completed, system tests (mount ASICs on FEMBs, attach FEMBs to a APA, test in realistic environment, investigate possible system related issues) in progress
- In the process of implementing design changes (bug fixes, small changes in requirements) in preparation of submission of next version of prototypes

Timeline

- Expect to have 2nd round of DUNE prototpyes submitted by June, complete standalone and system tests by January 2021, and at that time make a decision between the two ASIC solutions for DUNE
  - Very tight time schedule driven by the desire of populating APAs for 2nd run of ProtoDUNE-SP at CERN in the Fall of 2021 (need large number of ASICs, require engineering run in early 2021)
- Fabrication of ASICs / FEMBs for the DUNE detector to follow in 2022

Charge for the review committee

- Are we on the right track to ensure that the next prototype of the ASICs has a significant chance of meeting all the DUNE requirements and that we will be able to launch an engineering run in early 2021 such that we can populate the APAs for the second run ProtoDUNE-SP with final FEMB prototypes ?
- In detail

1. Are the requirements for the ASICs and FEMBs sufficiently well documented?
2. Do the chips and boards satisfy the requirements?
4. Are the full specifications of the ASIC designs and complete documentations for ASIC users available in EDMS or DocDB? Is the standalone testing of the ASICs complete and are the results of these tests available in public documents in DocDB or EDMS? Are there test results that are not yet fully understood and require further work before the ASIC design team(s) can proceed to a further iteration of the design? Should the COLDATA and CRYO ASICs develop in-situ time delay measurements to the WIB?

Charge for the review committee

5. Do the standalone tests of the new generation of ASICs indicate that the design goals have been achieved? Do these design goals meet the detector requirements? Have all issues observed in previous versions of the ASICs been addressed? Do the performance measurements obtained from test stands meet the expected performance? Does the response of the ASICs match the expectations obtained from simulation?
6. Is there an understanding of the reasons why issues with the ASIC design uncovered during testing (if any) were not observed during the simulation of the ASIC prior to the submission? Are the design methodology and the simulations of the ASIC response appropriate or are there improvements that could be made to avoid such problems future revisions? Is the internal review mechanism prior to the submission of an ASIC sufficient to identify possible failure mechanisms and to fully verify that the ASIC design is meeting the specifications? Should there be an external review of the ASIC design prior to the submission of the next iteration?

Charge for the review committee

7. Is the appropriate documentation of the FEMB design(s), the corresponding Gerber files and bill of material available in EDMS?
8. What is the status of fabrication for the various FEMB prototypes and what is the timeline for standalone tests of the FEMBs and later for system tests?
9. What are the plans and the timeline for the next iteration of the design of the ASICs and FEMBs? Have sufficient resources been put in place to meet the submissions deadlines? Are there lessons learned from the previous design iteration of the ASICs on the management of distributed design teams? Are processes in place to ensure that the next ASIC submissions will not encounter the delays observed for the first submissions? Are plans for required technical resources consistent with scope of remaining work? Should there be an external review of the ASIC design prior to the submission of the next iteration?

Charge for the review committee

10. What are the timeline and plans for obtaining results from system tests and from components lifetime tests on the current generation of ASICs and FEMBs? How will the results from these tests influence the decision on the submission of the next set of prototypes? What are the plans for testing to verify that the new ASICs/FEMBs will not cause additional system noise beyond that seen in ProtoDUNE?

12. Are there any issues with the design that will complicate the procurement strategy and manufacturing plans for the ASICs and the FEMBs? Does the design lead to complications in the development of the quality assurance program and what kind of tests / vendor qualifications are required before finalizing the design of these components?

Questions we would like to skip (i)

3. Have interfaces with other Cold Electronics detector components (e.g. WIB communications and data protocols, clock and power distribution, cabling and connectors) been addressed and documented? Are the electrical and mechanical interfaces with the APA fully defined and documented? Have lessons learned from ProtoDUNE been implemented?

   - Some of this will be discussed in the CRYO, COLDATA, and FEMB presentations, but some aspects are still being finalized
   - Mechanical interface with APA was discussed in another PDR last year and nothing has changed, electrical interface with APA has not changed since ProtoDUNE (but needs to be documented thoroughly)
   - We propose to postpone this question to the next PDR (system aspects) that is planned for March 11/12

Questions we would like to skip (ii)

11. What is the progress with the development of criteria for the selection of an ASIC solution for DUNE? What is the progress with the reliability committee and how will the results from this committee influence the ASIC selection process? Have the design rules for long lifetime in the cold been satisfied?

- For multiple reasons the current generation of new ASICs (ColdADC and CRYO in particular) is not suitable for perfoming the kind of testing required to demonstrate that all the design rules for operation in LAr have been implemented correctly and that the ASICs have a lifetime such that there will be a negligible number of failures during the lifetime (20-30 years) of the DUNE experiment
- While we believe that all the rules have been implemented correctly we are planning to make these tests and will have results in time for the ASIC selection (and FDR) early in 2021

Questions we would like to skip (iii)

11. What is the progress with the development of criteria for the selection of an ASIC solution for DUNE? What is the progress with the reliability committee and how will the results from this committee influence the ASIC selection process? Have the design rules for long lifetime in the cold been satisfied?

- The reliability committee agrees in general terms with our approach, but has not yet produced its final report (I am guilty of not applying sufficient pressure on the committee chair….)
- We have not made progress with the development of criteria for the ASIC selection, and this is something that we need to agree on between now and the beginning of the Summer

Agenda

- We are going through the various ASICs in a non-ideal order due to the time constraints for some of us
  - This morning: CRYO
  - This afternoon: ColdADC and COLDATA
  - Tomorrow morning: LArASIC
  - Tomorrow afternoon: FEMBs
- We hope that we have allocated sufficient time for ample discussions
- We have reserved a spot at the end of the Thursday afternoon session and at the beginning of the Friday morning session for additional presentations / question and answer session that you may require