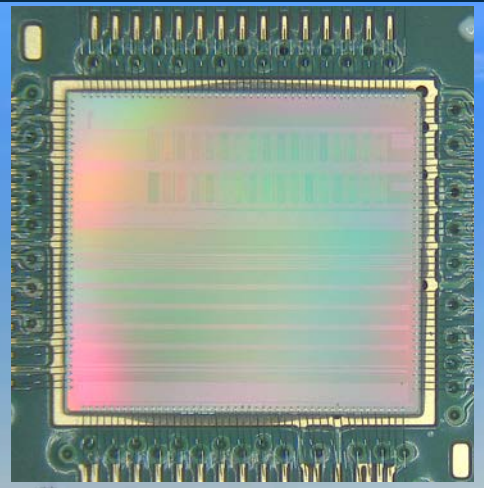
BERKELEY LAB Lawrence Berkeley National Laboratory

U.S. DEPARTMENT OF ENERGY

ColdADC Measurements



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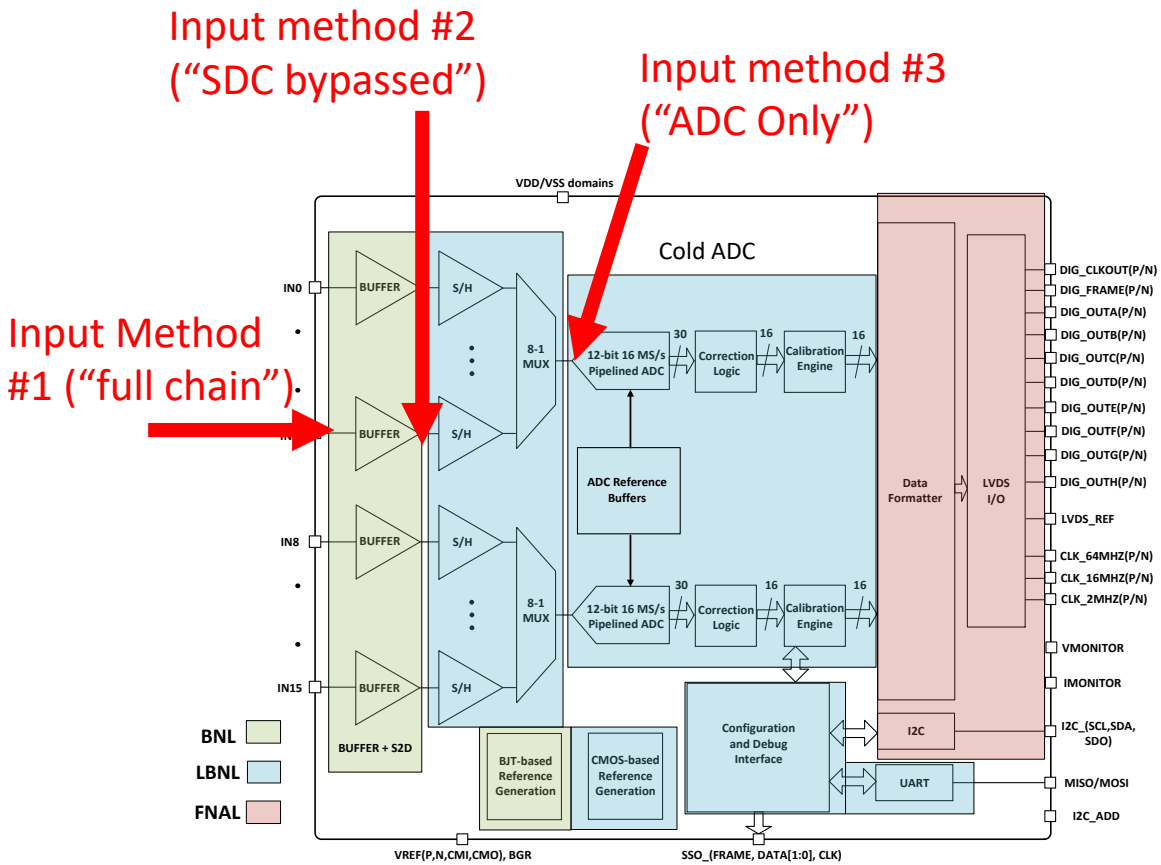
05 February 2020
DUNE PDR: TPC Electronics ASIC/FEMB Review @ CERN

Introduction

- ColdADC ASICs received from foundry in early 2019
- Extensive testing program at Fermilab, BNL and LBNL
- A number issues were identified relatively quickly
- ColdADC is highly configurable with many redundancies to mitigate risks
- Able to configure the chip to operate well
- Initial performance results are good
- Will present the findings/results in this talk. Carl will cover our understanding of the issues and changes planned in the next talk

Testing Terminology/Jargon



For standalone test using pulser for input signal, three input methods are available

When LArASIC is used, only input method #1 and #2 are available

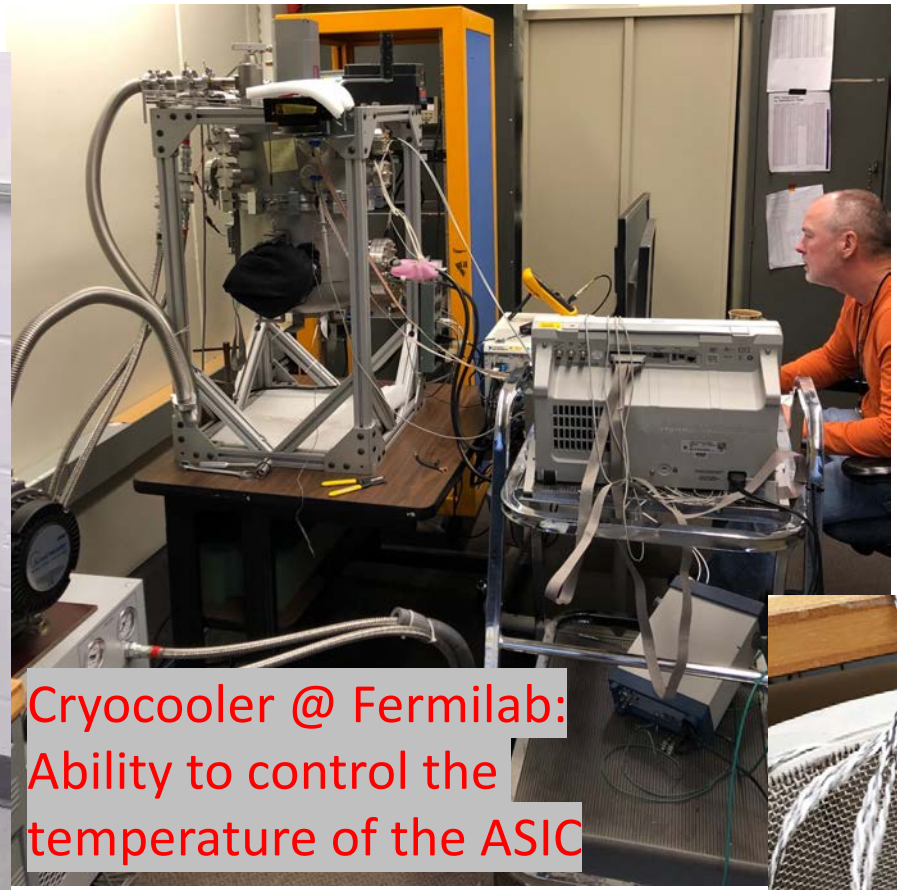
"Frozen SHA/MUX":

- MUX is disabled
- One specific channel is sent directly to pipelined ADC (sampled at 16 MHz)

Cryogenic Systems

Cryogenic Test System (CTS):

- Multiple units built by MSU. Available at all 3 labs
- Quick thermal cycling time
- Will use for production testing



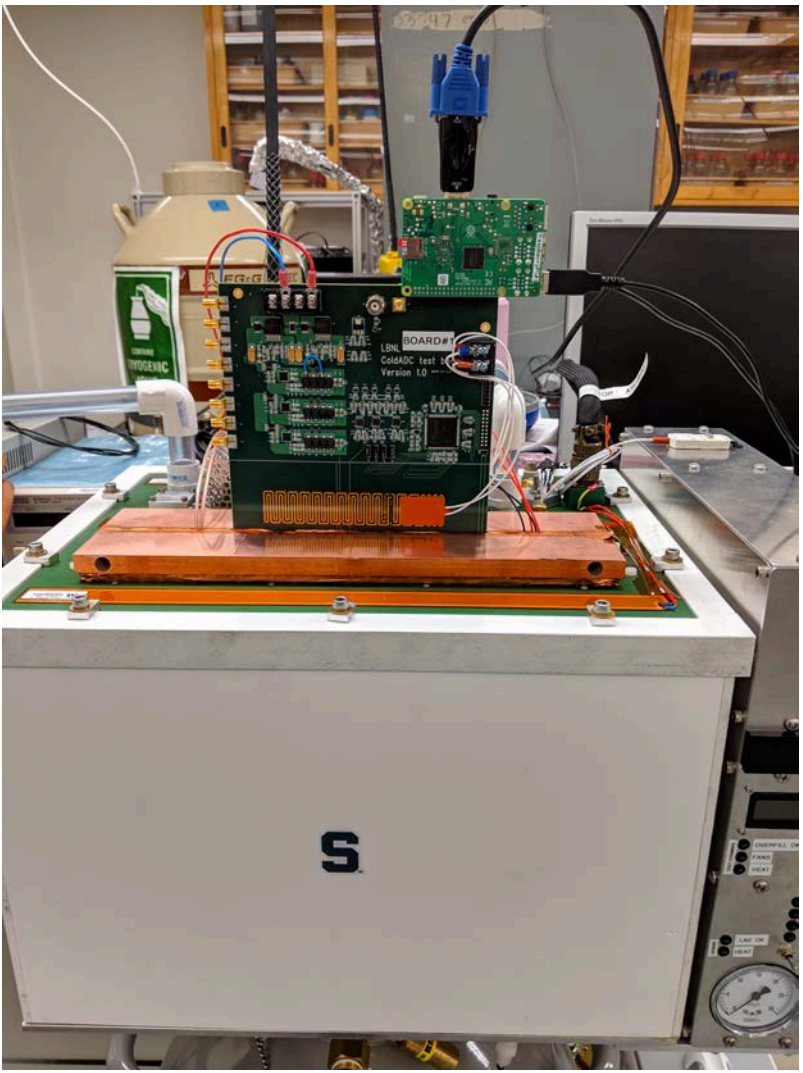
Cryocooler @ Fermilab: Ability to control the temperature of the ASIC

Open dewar

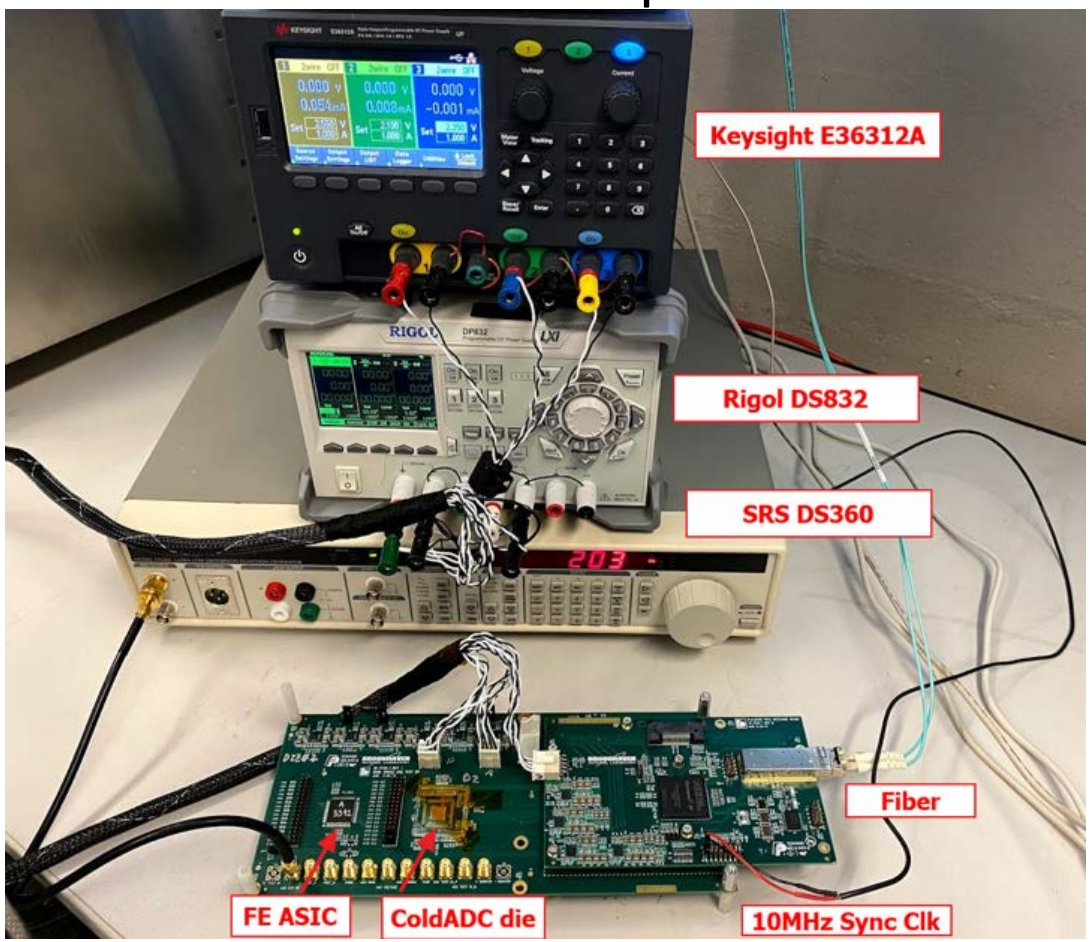
Test Boards

Fermilab cryocooler setup uses NI FPGA board for readout

LBNL Test Board in CTS



BNL Test Setup



ColdADC Performance Summary

Configuration for System Level Integration Test:

- VDDA2P5=VDDD2P5=2.5 V; VDDD1P2= 2.0 V; VDDIO=2.25 V
- CMOS Reference (VREFP=1.95 V, VREFN=0.45 V, VCMI=0.9 V, VCMO= 1.2 V)
- SDC bypassed

Specification	Value	Result	Note
Operation Temperature	Room Temp. (RT) and 88 K	Success	
Sampling Rate	2 MHz	2 MHz	
Noise	200 μV-rms –	189 μV-rms (302 μV-rms)	@ LN_2 temp (RT)
Differential Non-linearity (DNL)	$\pm$0.5 LSB (at 12-bit level)	+0.2 to −0.5 LSB	@LN_2 ; typical values
Integral Non-Linearity (INL)	$\pm$1 LSB (at 12-bit level)	+1.2 to −1.1 LSB	@LN_2, typical values
Effective-Number-of-Bits (ENOB)	11.0 bits	<mean>=10.6 bits rms=0.3 bits	@ LN_2
No Missing Codes Across Dynamic Range	N/A	Success	@LN_2 and RT
Crosstalk	No Specification	$< 0.5\%$ ($< 1\%$)	@LN_2 (RT)

Functional Tests

Core functions performed as expected:

- I2C, UART communications
- Chip reset
- LVDS I/O
- CLOCK generation
- Data formatter
- Etc.

Auto Calibration for Pipelined stages:

- Did not work. Issue understood
- Calibration is done offline and then weights are loaded back to the ADC registers
- Inconvenient but offline calibration is functionally identical to autocal

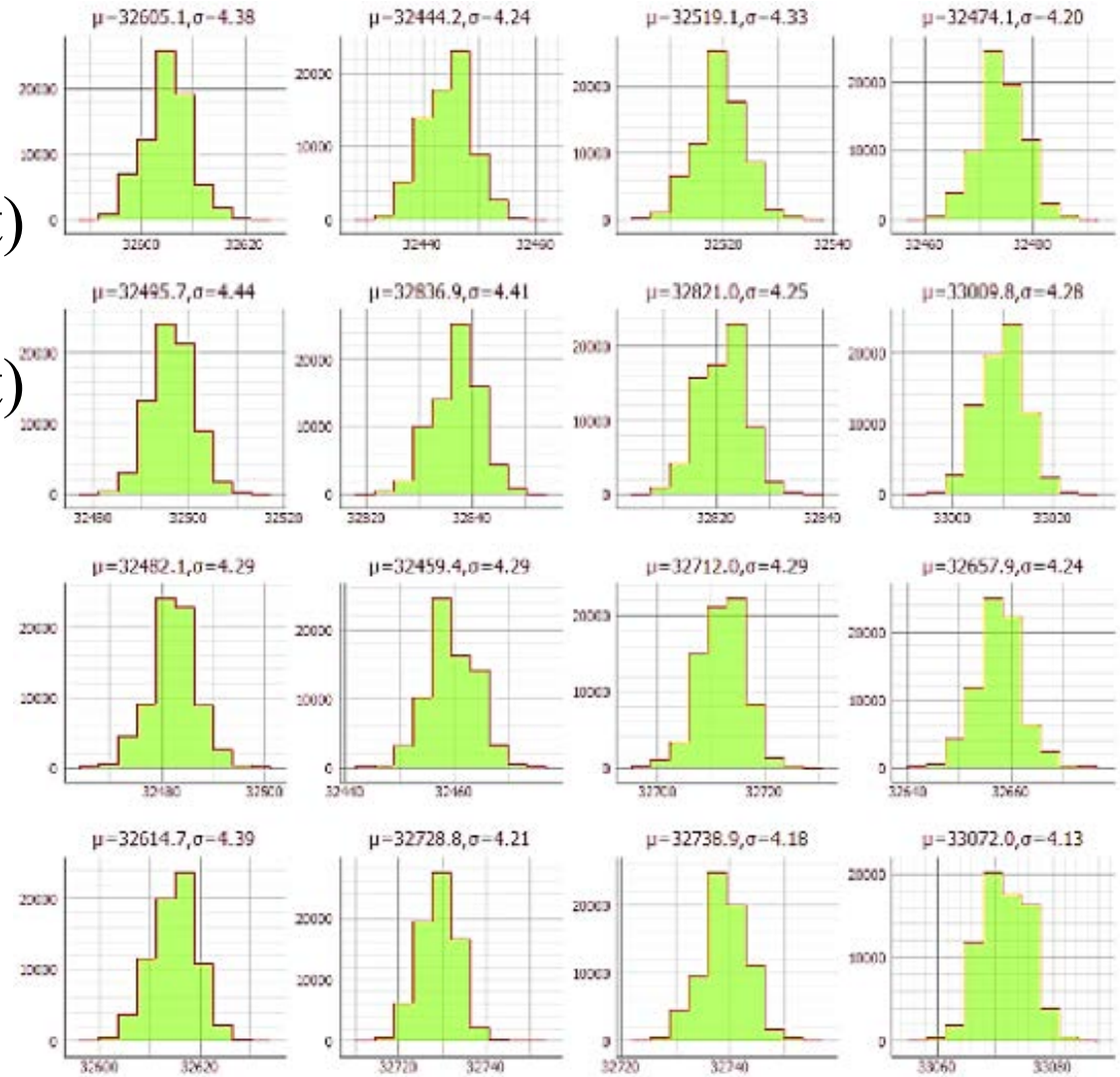
ADC Noise

ColdADC noise performance is excellent

Measured noise:

- 302 μV-rms (6.7 LSB 16-bit) at room temp
- 189 μV-rms (4.2 LSB 16-bit) at LN_2 temp

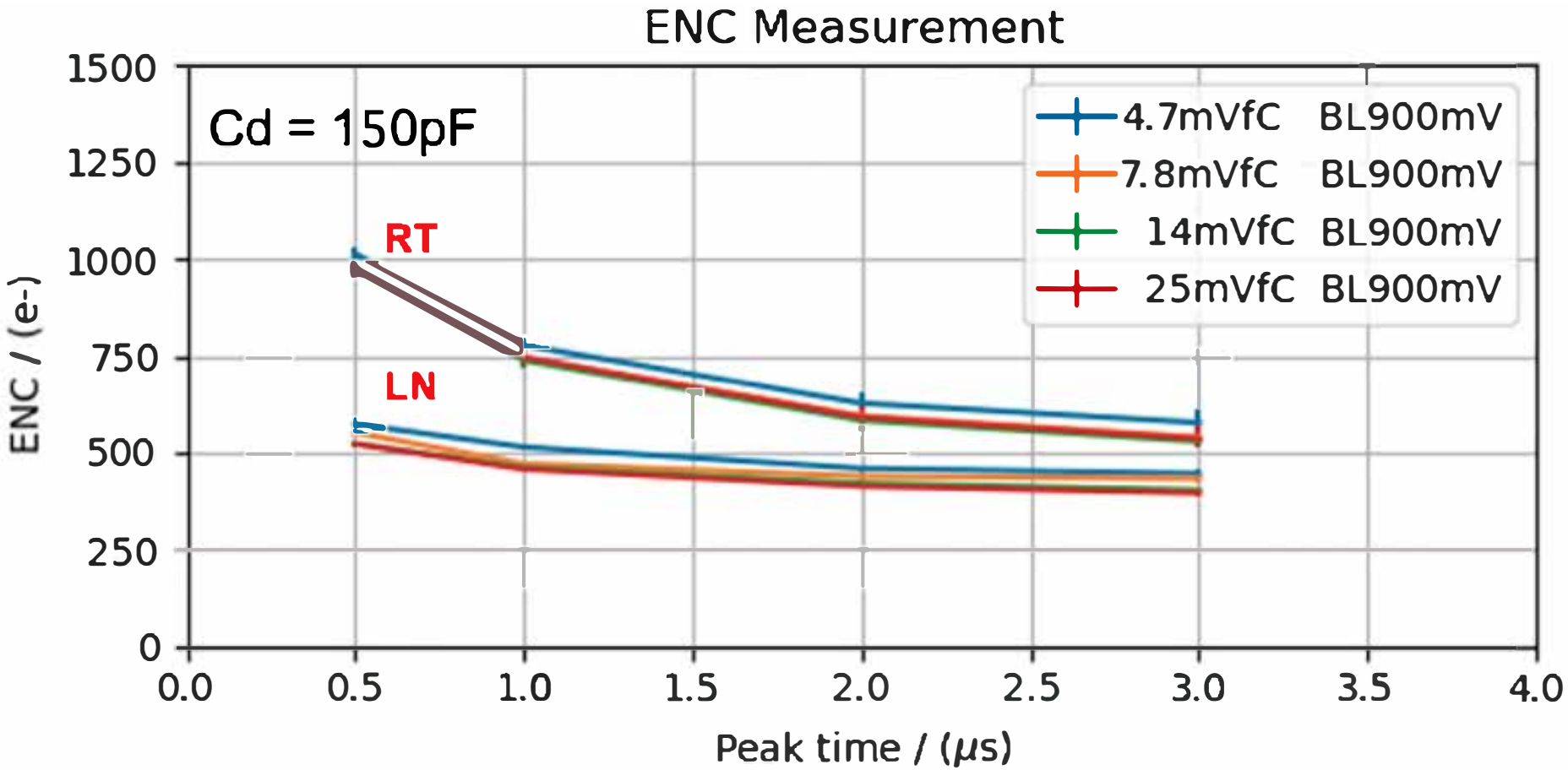
Measured with SDC bypassed.
SDC noise is negligible



LArASIC+ColdADC Noise

Noise for the full chain (LArASIC+ColdADC) also measured

With 150 pF capacitor at LArASIC input to simulate TPC sense wire capacitance

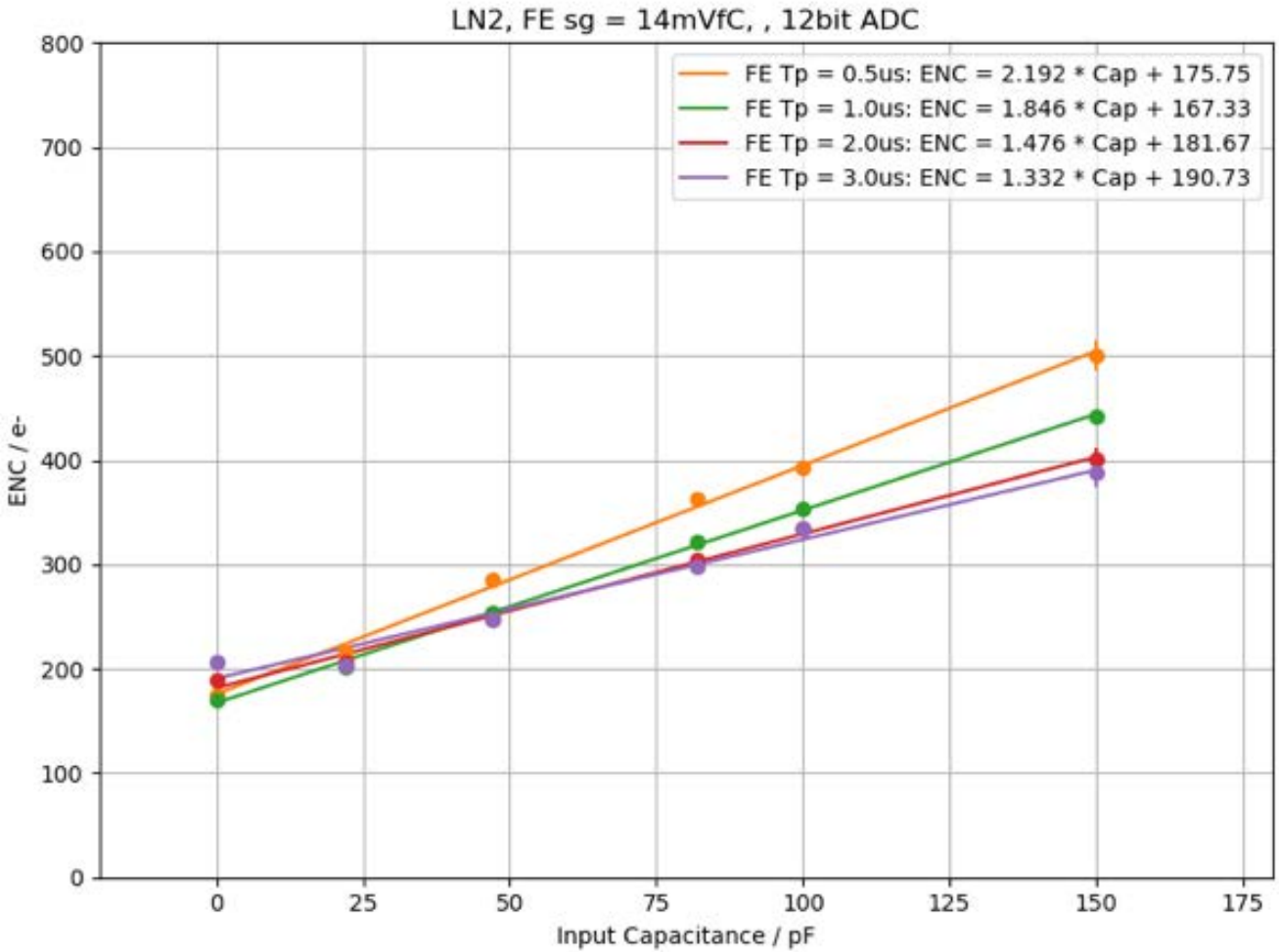


No significant differences between CMOS vs BGR

LArASIC+ColdADC Noise

Noise as function of input capacitance at LN_2

Showing good linear relationship between noise and capacitance



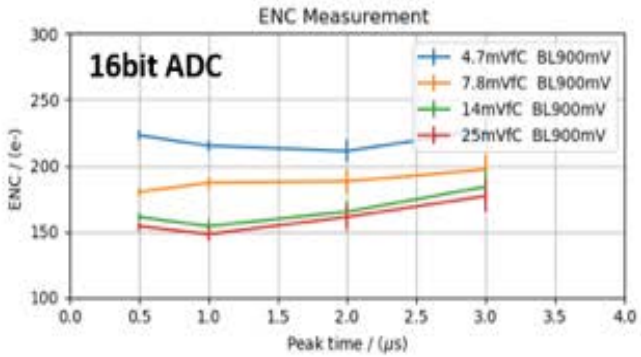
Note: due to test setup, the actual capacitance may be slightly lower than the points shown

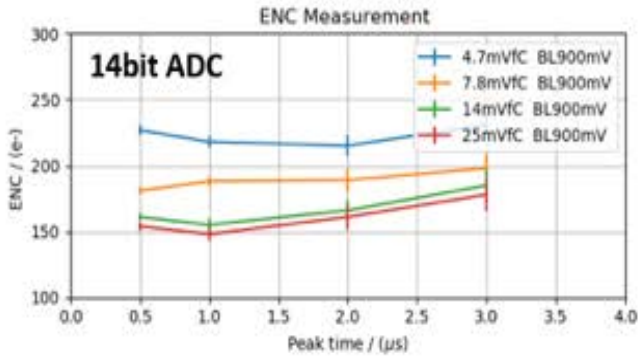
14-bit ColdADC

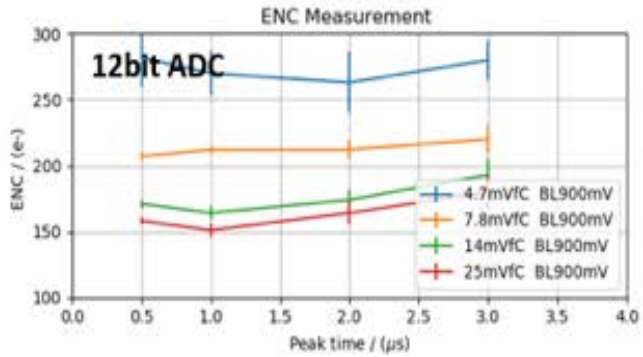
Default plan is to truncate 16-bit down to 12-bit

Given the superb noise performance, will consider outputting 14-bit

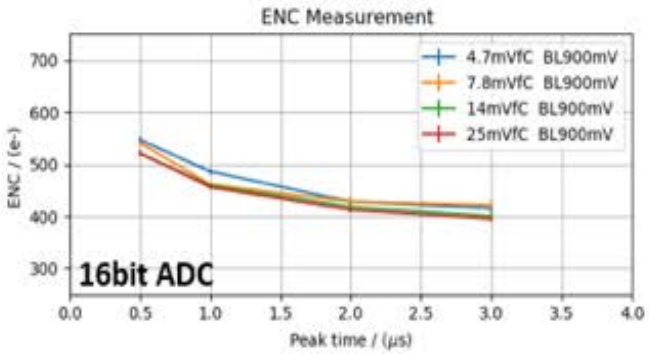
With Input Floating

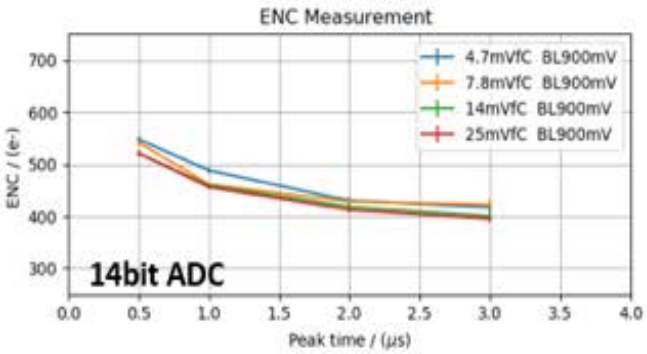


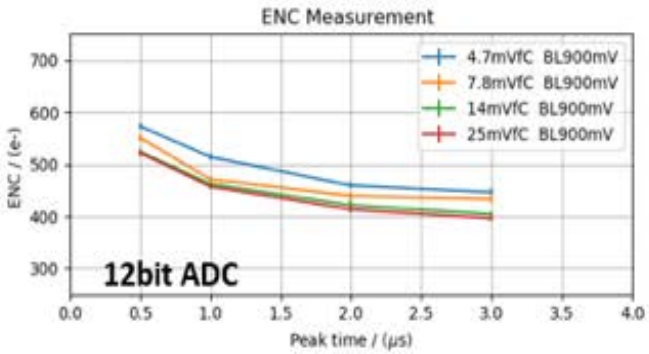




With 150 pF Mica Capacitors at Input

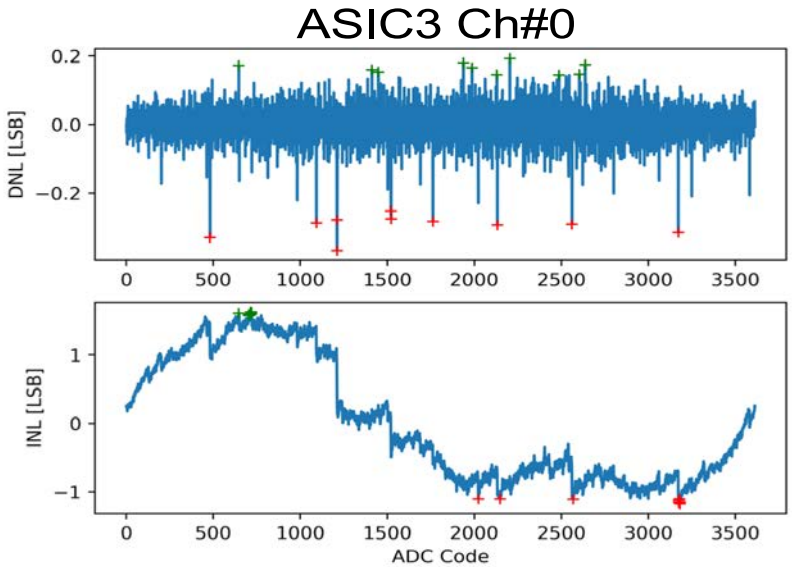


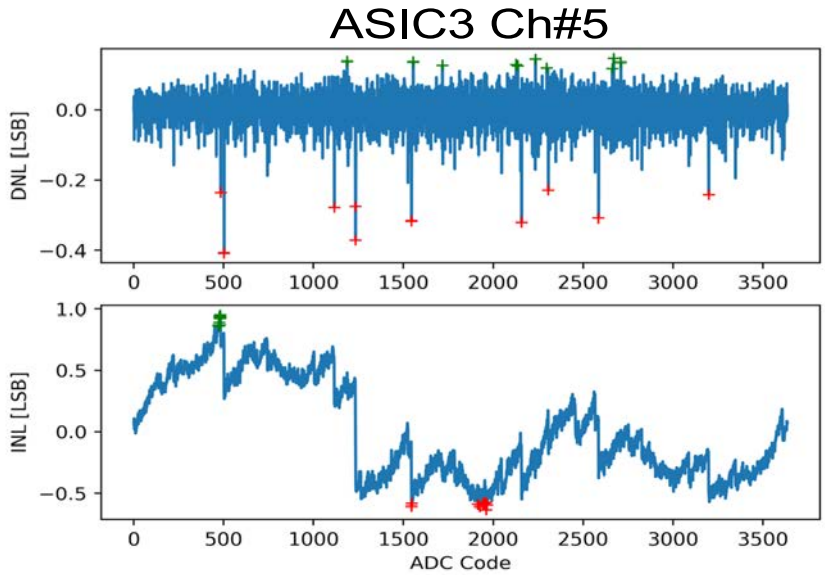


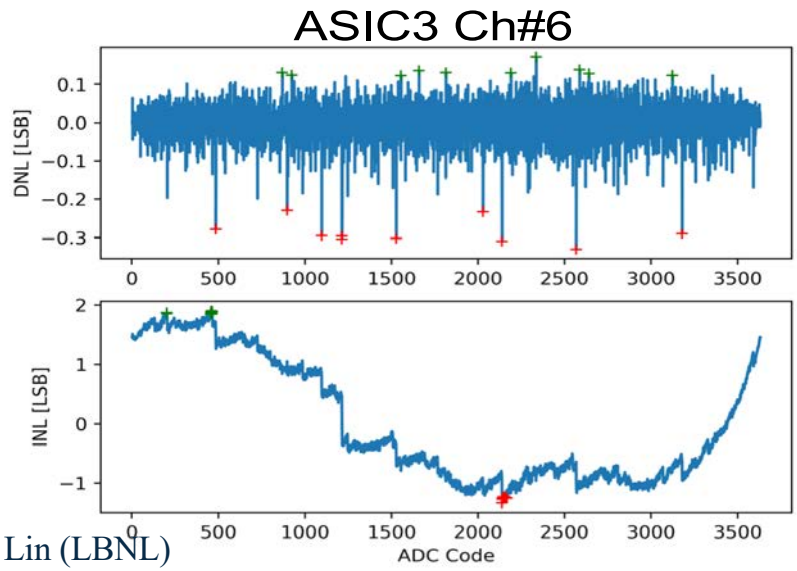


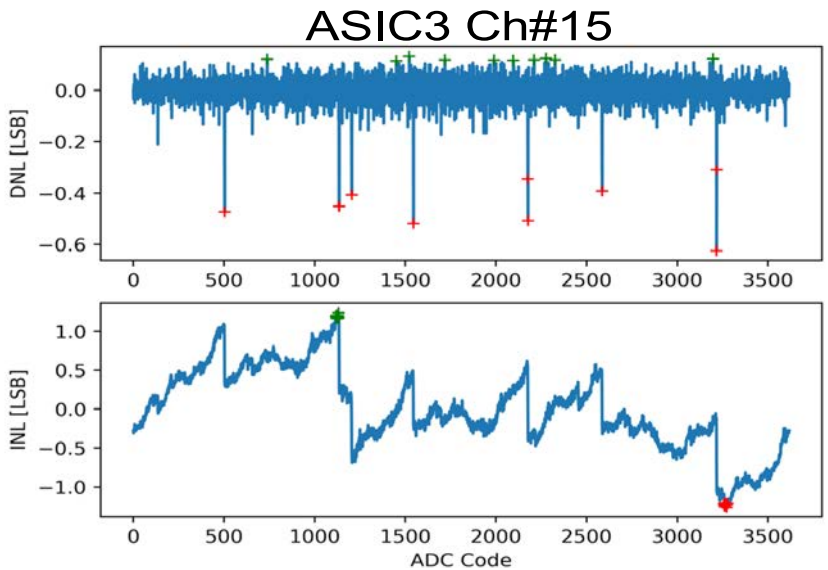
ColdADC Static Linearity

- Apply sine wave to input channel
- Extract DNL and INL from code density histograms





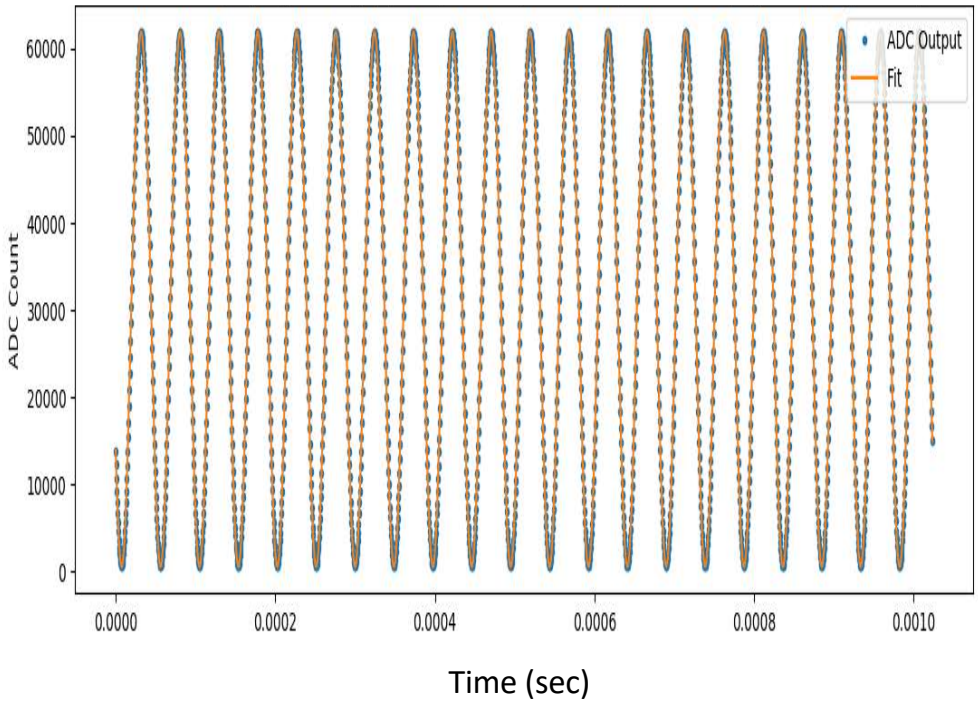


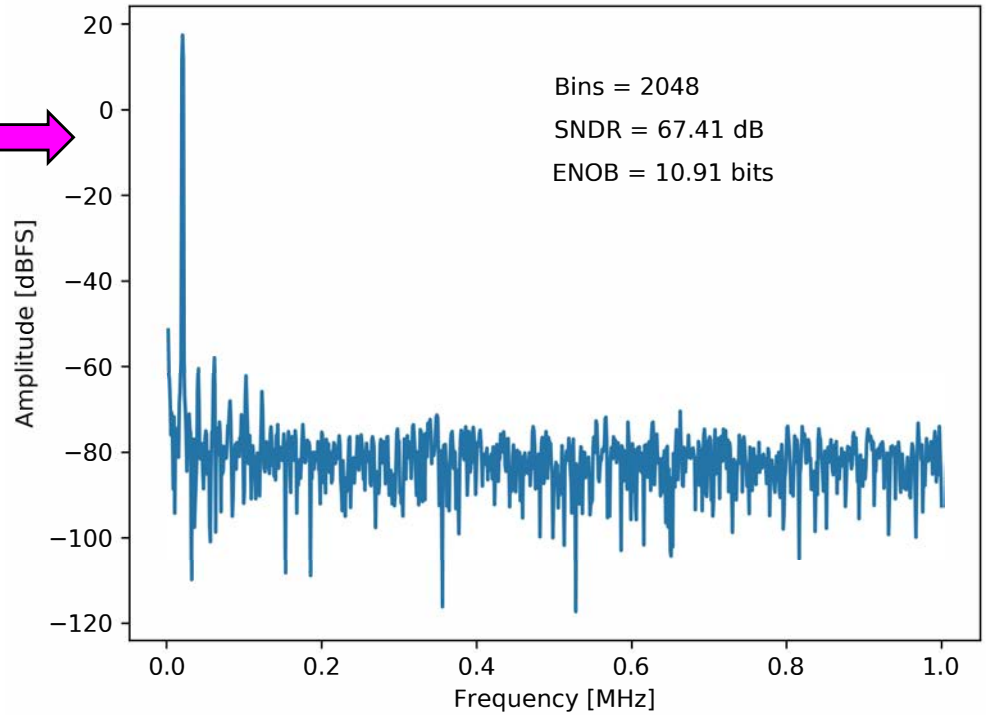


ColdADC Dynamic Linearity

FFT on coherently sampled sine wave

LN_2 Measurement



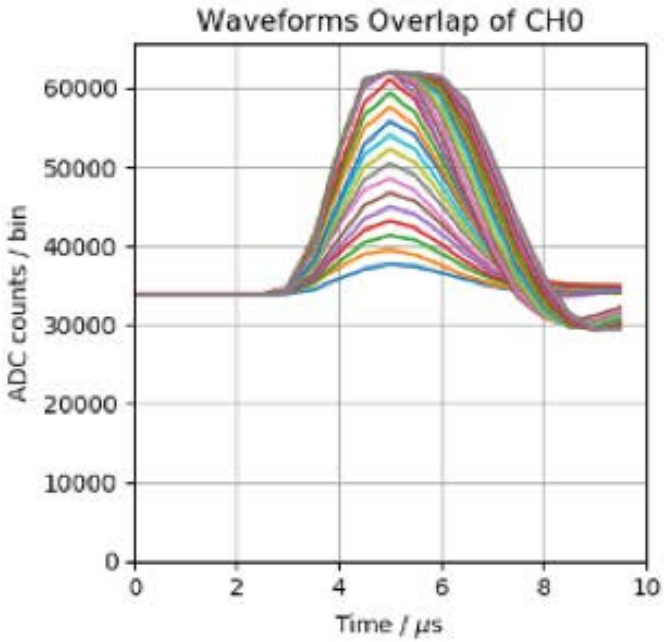


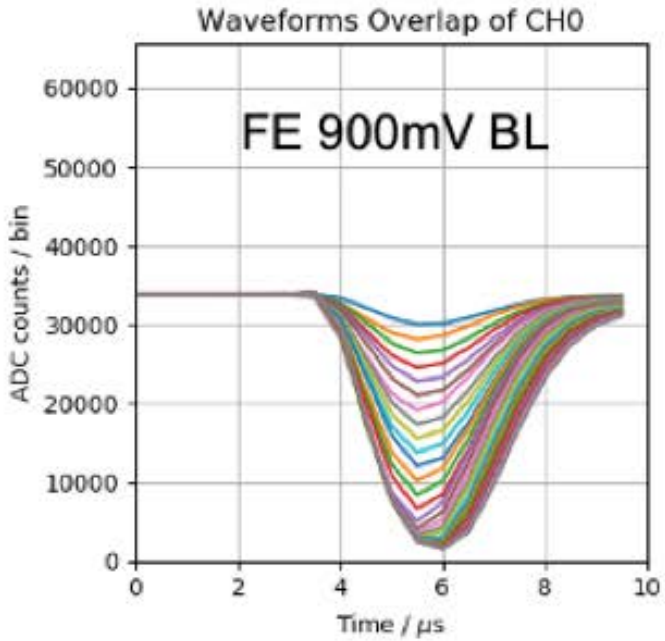
Measured ENOB ASIC (16 channels):

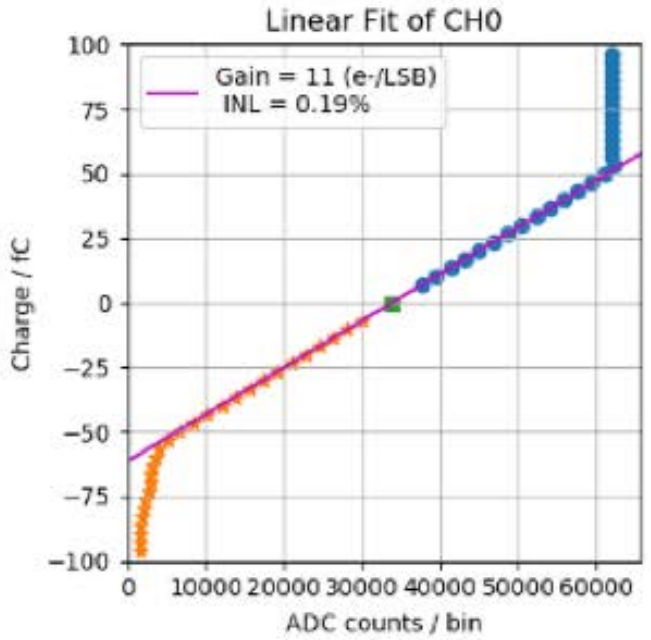
Channel#	Ch0	Ch1	Ch2	Ch3	Ch4	Ch5	Ch6	Ch7
ENOB	10.5	10.8	10.2	10.4	10.7	9.8	10.6	10.4
Channel#	Ch8	Ch9	Ch10	Ch11	Ch12	Ch13	Ch14	Ch15
ENOB	10.2	10.5	10.6	10.5	10.7	10.3	9.8	9.7

LArASIC Calibration Circuit

LArASIC has a 6-bit DAC to inject charge at input for calibration



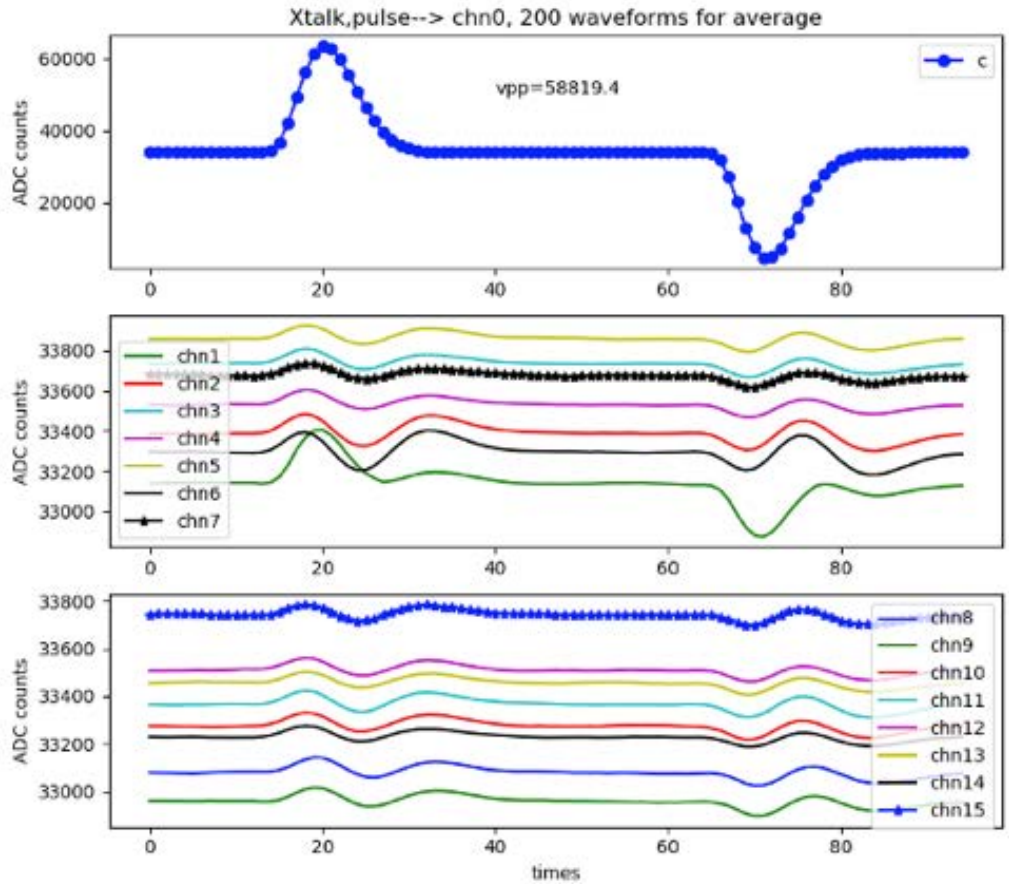




Observed non-linearity (from linear fit) of 0.19% is dominated by the 6-bit DAC. Non-linearity from LArASIC+ColdADC is expected to be well less than 0.1%

Channel Crosstalk

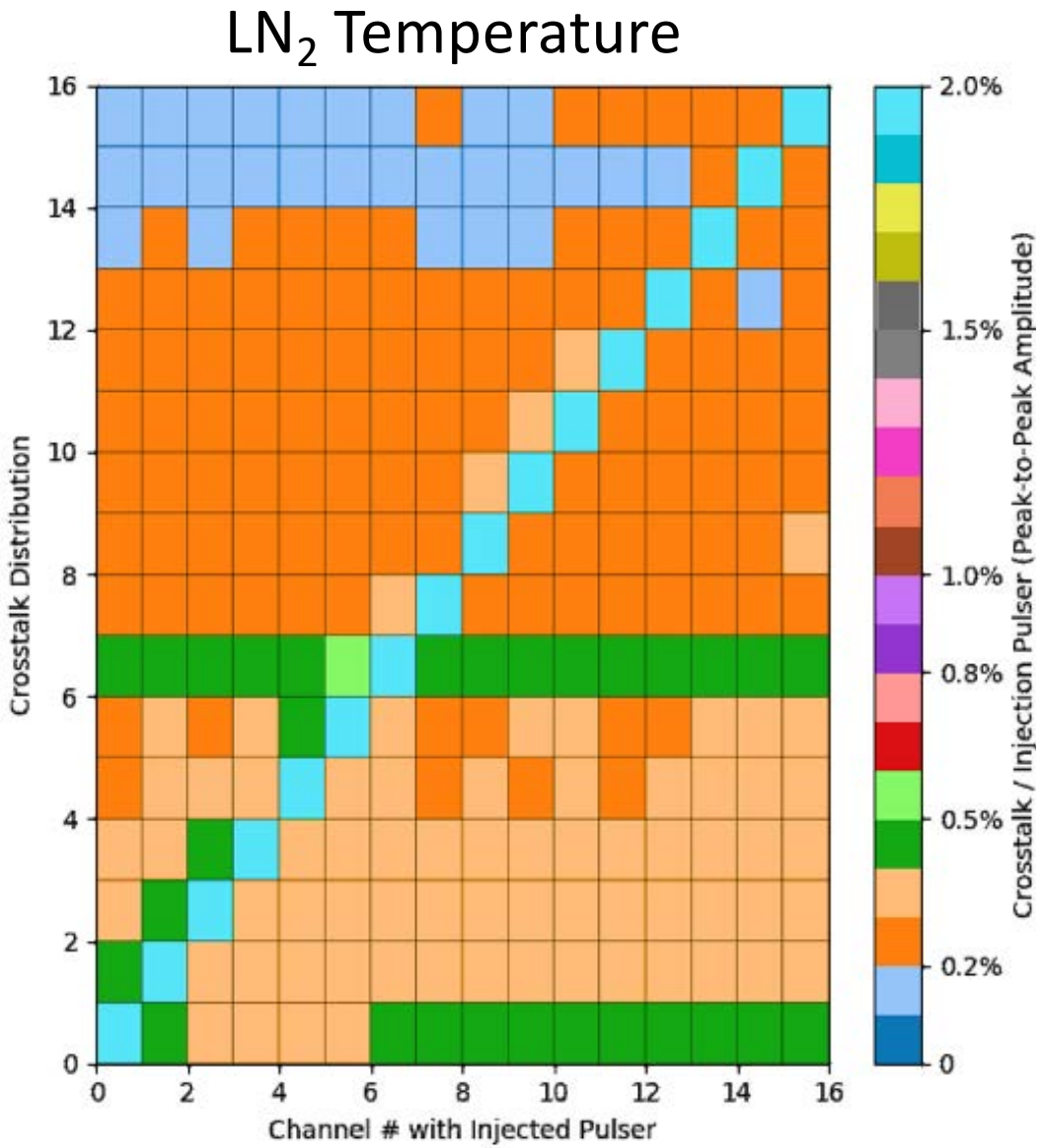
- Study channel crosstalk for LArASIC+ColdADC together
- Large input pulse on one channel and look at the response on the remaining 15 channels



Room Temperature

CHN	Amplitude /LSB	Crosstalk /%
0	58819	100
1	532	0.905
2	184	0.314
3	142	0.242
4	136	0.231
5	131	0.223
6	221	0.375
7	117	0.199
8	120	0.203
9	120	0.204
10	114	0.194
11	114	0.194
12	99	0.168
13	96	0.163
14	88	0.149
15	88	0.149

Channel Crosstalk



Results:

- Largest crosstalk on the adjacent channel within the ADC core
- About 1% at warm;
  < 0.5% at LN_2 temperature
- Studies suggest the source of the crosstalk is in SHA/MUX

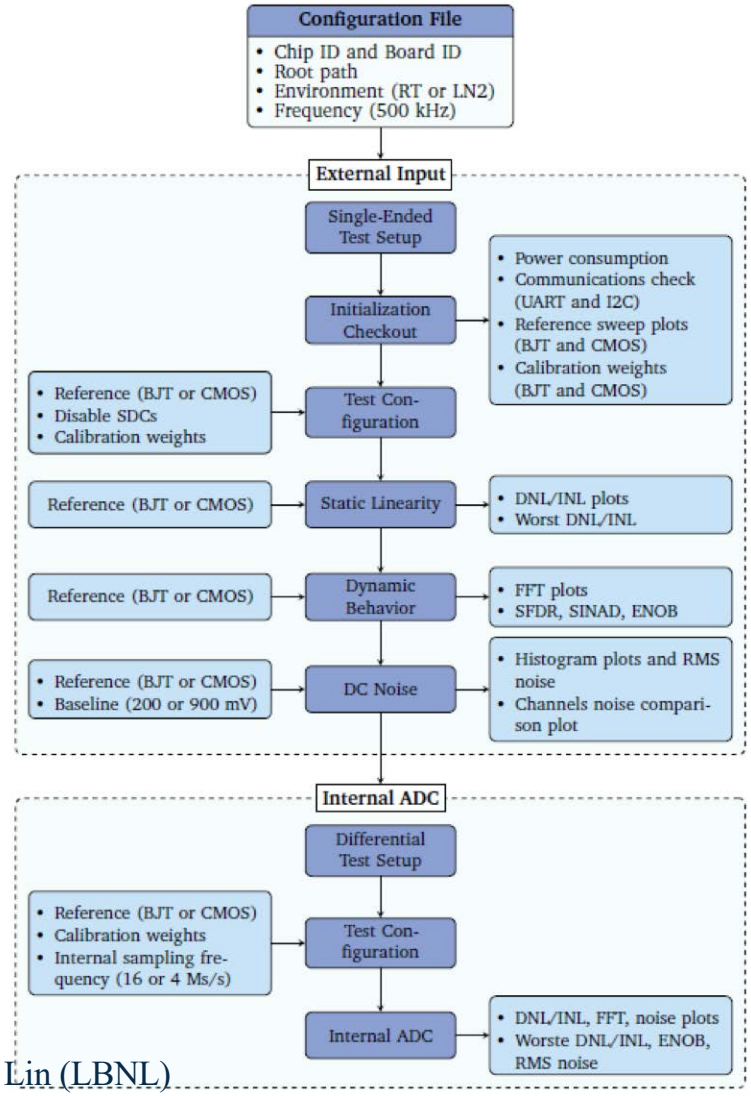
ColdADC Power Consumption

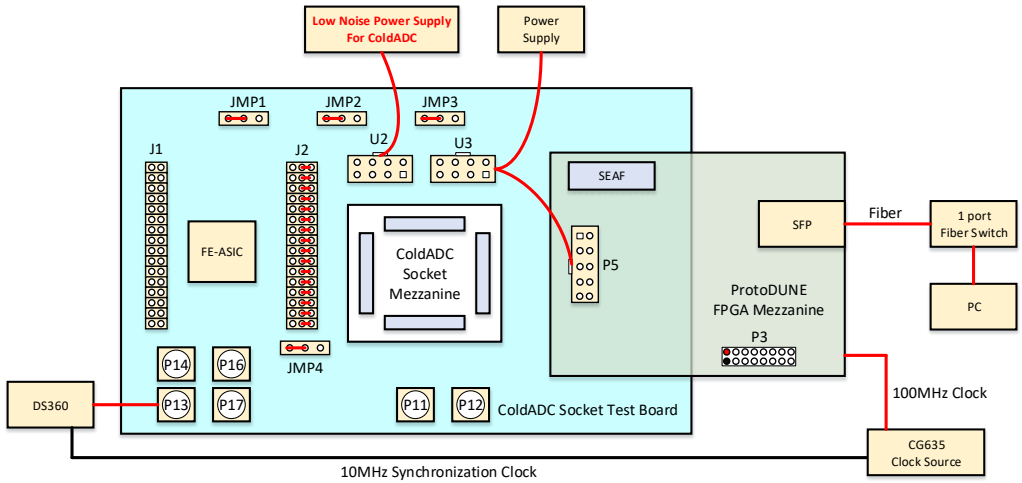
- Running ColdADC at higher than nominal voltages to address several issues (e.g. IR drop, missing level-shifter, etc.)
- Expect lower power consumption in the next revision of the ColdADC. Also similar performance between BGR and CMOS
- At our current nominal configuration, drawing ~425mW per chip (~26 mW/channel)

Temperature	RT	RT	RT	LN_2	LN_2	LN_2
Reference	BGR	BGR	CMOS	BGR	BGR	CMOS
SDC	enable	bypassed	bypassed	enable	bypassed	bypassed
VDDA2P5/VDDD2P5/ V	2.5	2.5	2.5	2.5	2.5	2.5
VDD1P2 / V	2.1	2.1	2.1	2.1	2.1	2.1
VDDIO / V	2.25	2.25	2.25	2.25	2.25	2.25
Total Power / mW	515	418	418	563	513	425
Power per Channel / mW	32.2	26.1	26.1	35.2	32.1	26.6

ColdADC Production Testing

- QC procedure developed and tested at BNL
- U. of Florida is setting up the production site to perform QC on the remaining ~90 packaged ColdADC chips

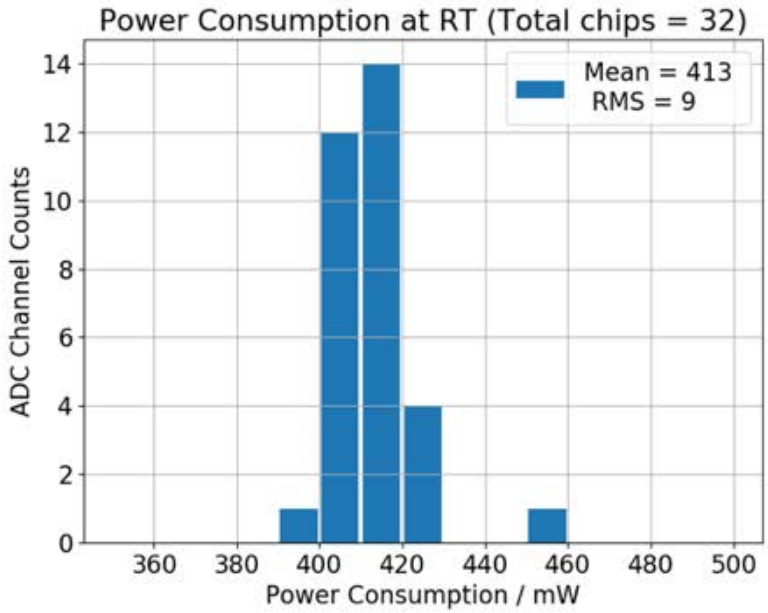




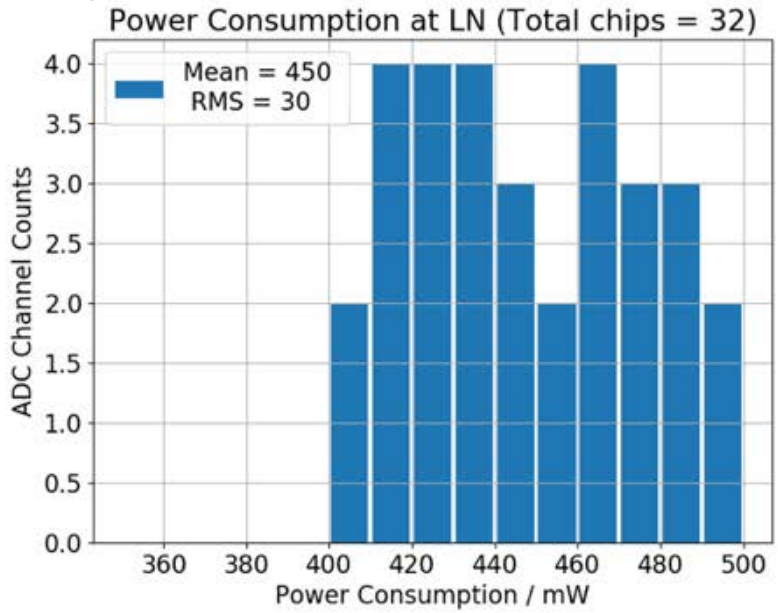
ColdADC Production Testing

- BNL performed QC on 33 packaged ColdADC
- One chip (#00096) drew high current. Has a “short” between VDDA2P5 and VSSA2P5. Sent out for post-mortem
- Also previously tested other chips. Out of 53 (51 packaged and 2 bare dies), only one failed. Yield is very good
- Showing results from the 32 QC’ed chips

Power Consumption



(a) At RT



(b) At LN2

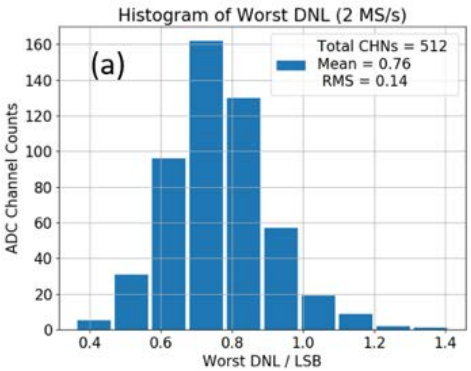
ColdADC Production Testing

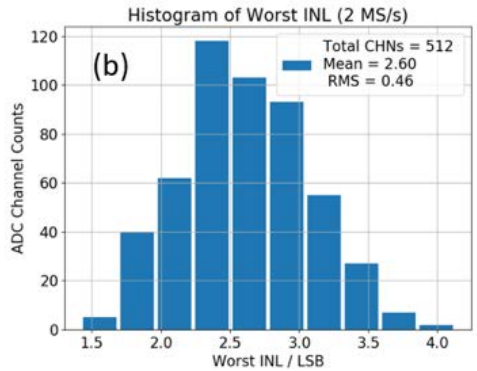
Linearity measurements are done with all 16 channels pulsed simultaneously

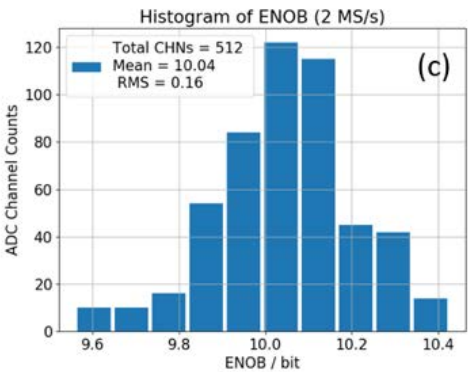
Due to crosstalk, slightly worse linearity values than single channel measurements

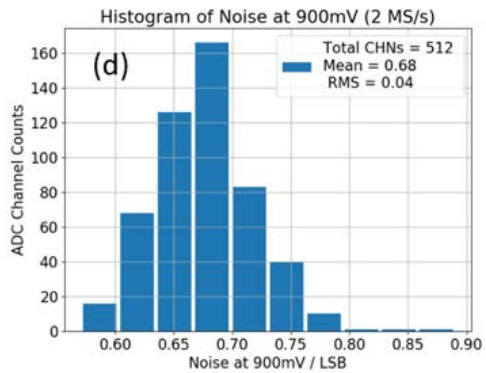
Linearity (Sampling Rate = 2 MHz)

RT

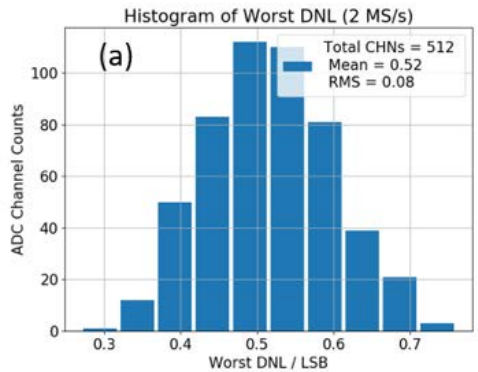


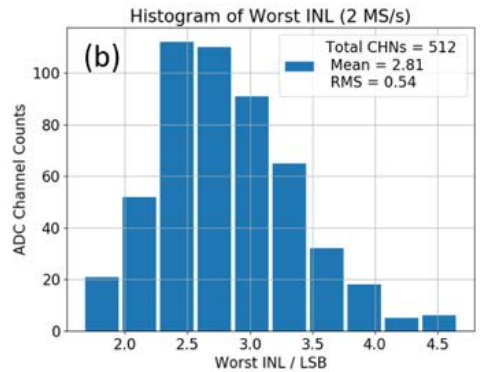


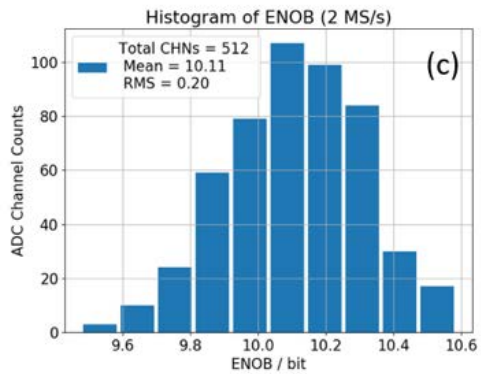


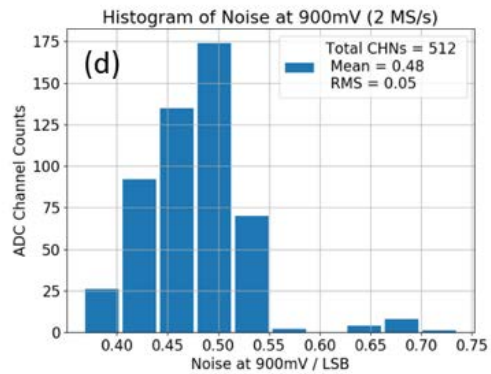


LN_2







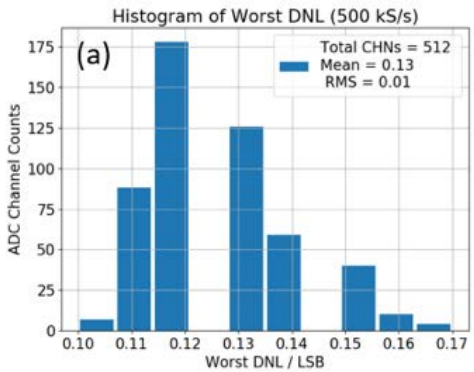


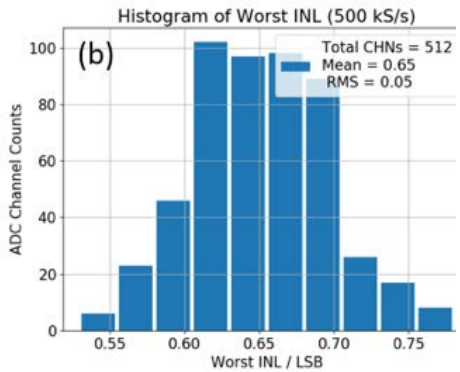
ColdADC Production Testing

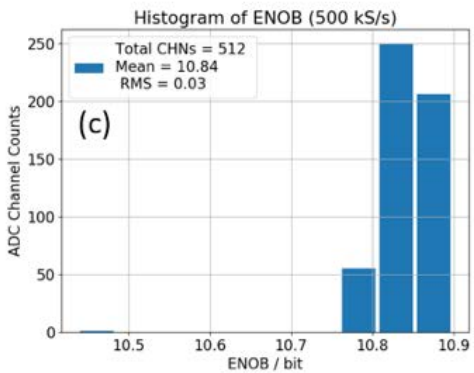
Also characterize performance with slower clock speed to estimate the performance with minimal crosstalk and kickback

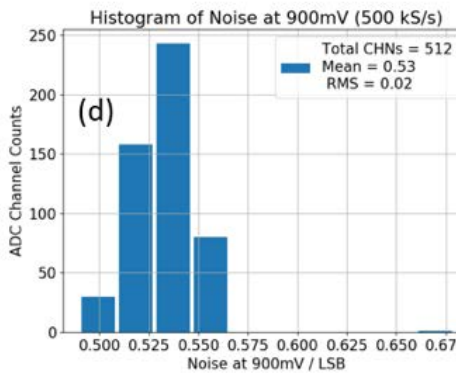
Linearity (Sampling Rate = 0.5 MHz)

RT

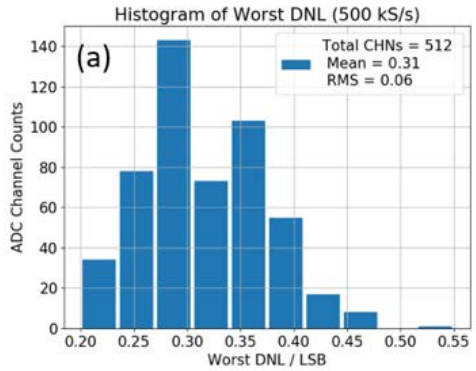


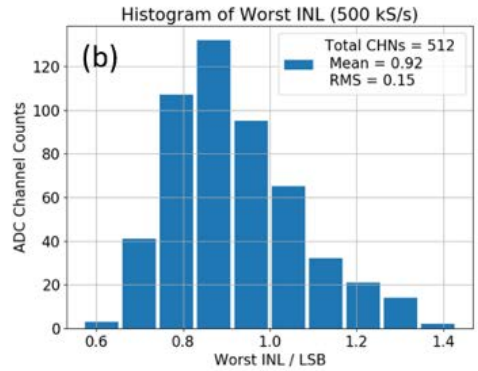


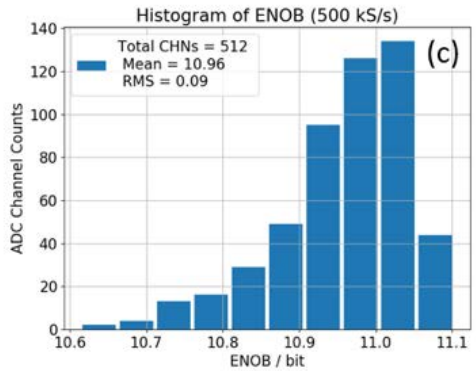


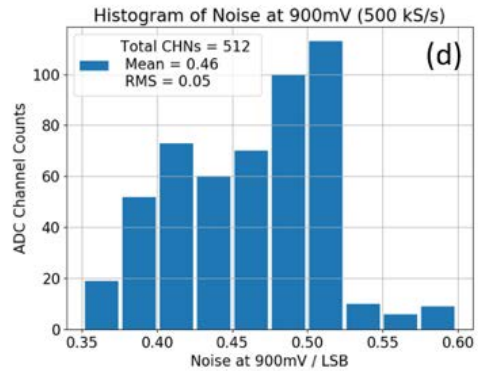


LN_2





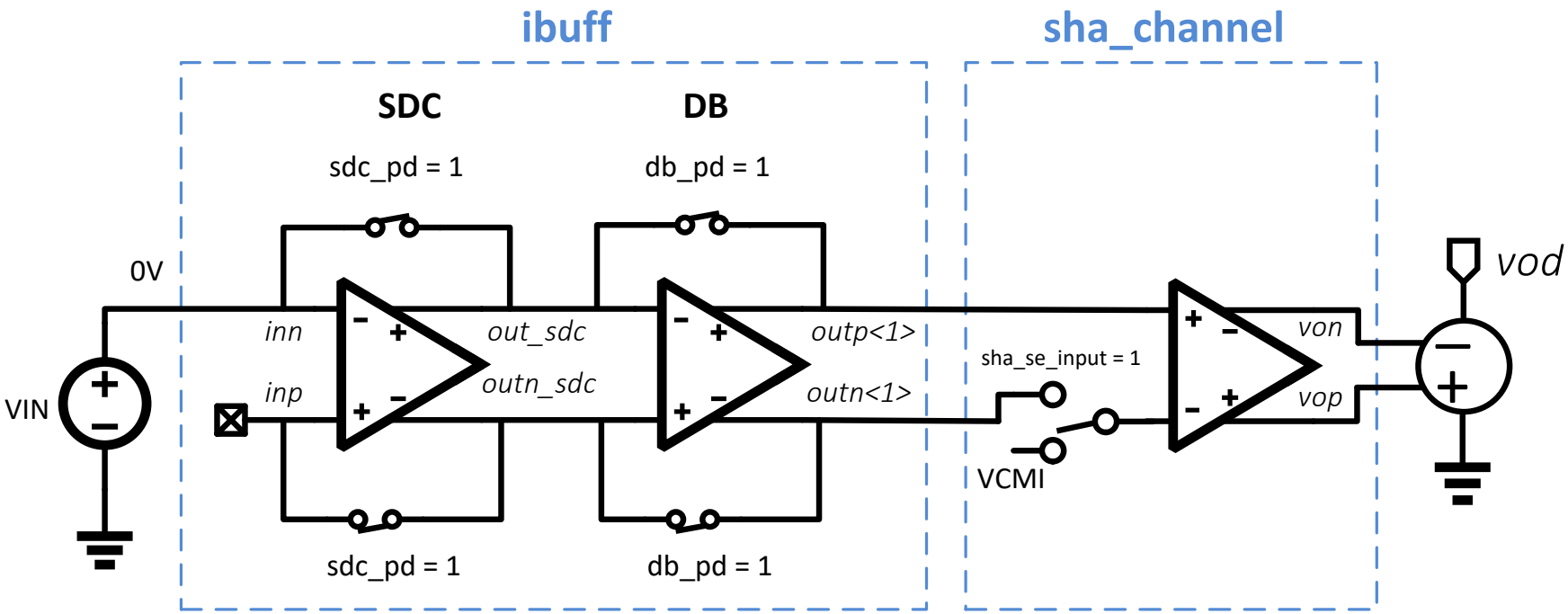


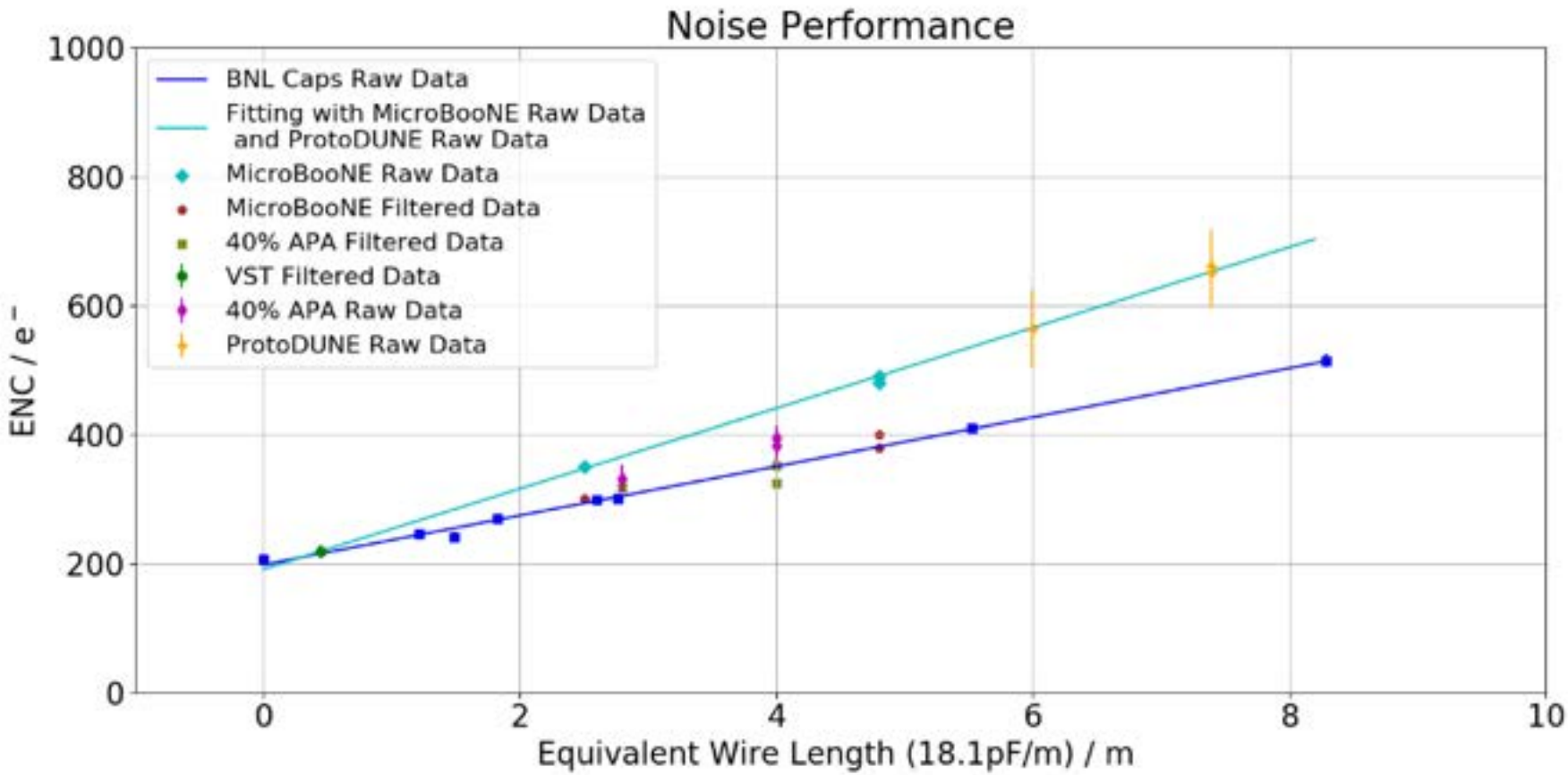


Summary

- First prototype of ColdADC is performing well. Essentially meeting DUNE specs
- Noise performance is excellent. Reducing quantization noise by going to 14-bit can further improve the overall system noise
- Will consider outputting 14-bit. COLDATA provides for 14-bit as well as 12-bit data (as does the Warm Interface Board output format)
- A number of issues were identified. With the redundancies and programmability of the ColdADC, able to configure the chip for good performance
- Power consumption is acceptable even at elevated operating voltages. Power consumption will go down in the next version of ColdADC
- Production QC Testing procedure has been exercised. Yield based on ~50 chips is high (>98%). Production Testing Site will QC the remaining packaged chips soon

Input Buffer





LArASIC gain = 14mV/fC; 2 μs shaping time

SDC Linearity

- SDC buffer may improve marginally the ADC DNL performance in LN_2 . However, it introduces large variation in INL
- Given that LArASIC output is capable of driving signal directly to ColdADC SHA, SDC is bypassed when characterizing the ADC performance