A Brief History of Cold Front-End ASIC Development for LArTPC

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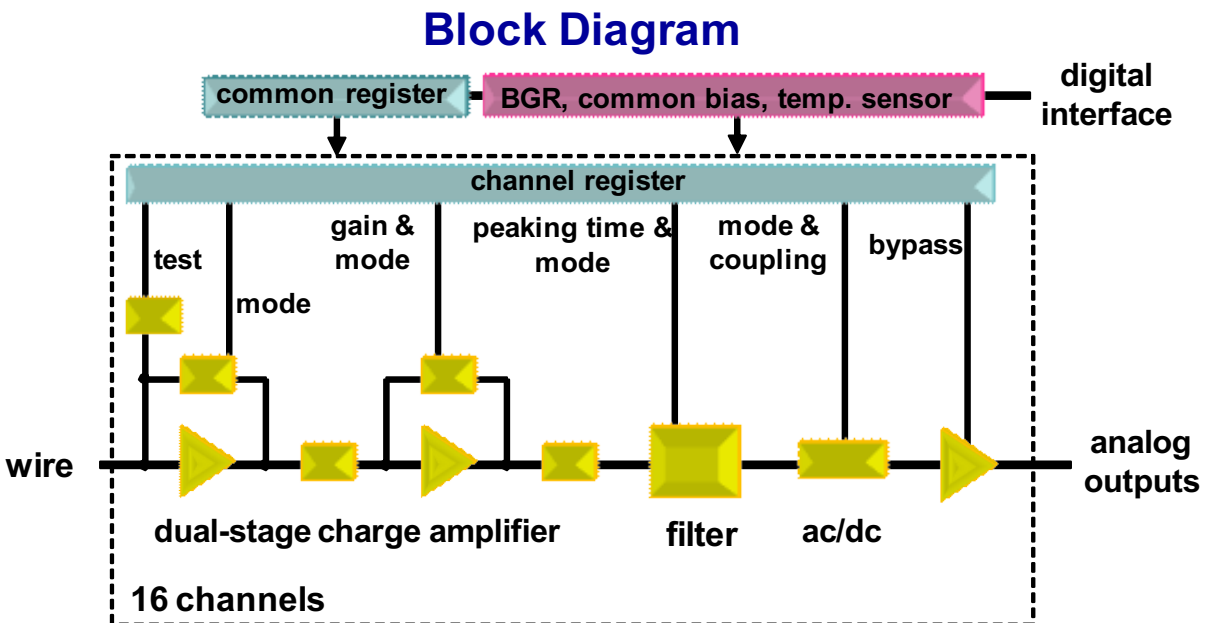
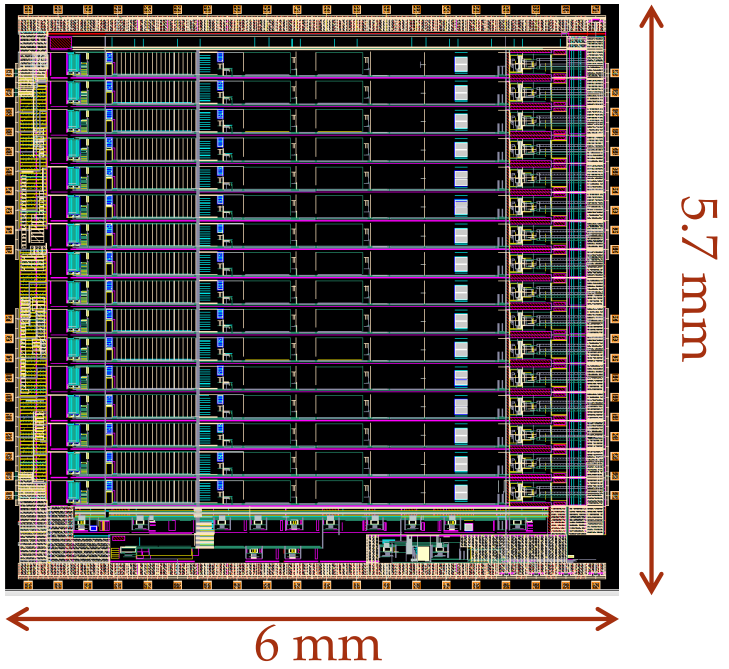
Outline

- Introduction
- Brief History of Cold FE ASIC Development
- Performance of FE ASIC in MicroBooNE and ProtoDUNE
- Summary

Introduction – Front-End ASIC





- 16 channels, programmable
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 900 mV)
- selectable dc/ac coupling (100μs)
- built in pulse generator with 6-bit DAC
- built in analog monitoring output
- programmable bias current: 100pA, 500pA, 1nA, 5nA
- rail-to-rail analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 144 configuration registers with SPI interface
- ~ 5.5 mW/channel (input MOSFET 3.9 mW)
- ~ 16,000 MOSFETs
- designed for 77K-300K operation
- designed for long lifetime
- tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES

A Brief History of Cold FE ASIC Development

Version	Submission	Results
V1	02/2010	Functionality in LN2 achieved
V2	12/2010	Optimization of input MOSFET and resistance of input line
V3	07/2011	AC coupling and improvement of DC PSR
V4	03/2012	Improvement of uniformity of calibration response in LN2
V4*	06/2012	Improvement of cold yield, instrumented ***MicroBooNE (8,256 channels)***
P1	02/2016	Internal pulse generator, bias current options, BGR start-up
P2	08/2016	Pole-zero cancellation, external resistor and analog monitoring, instrumented ***ProtoDUNE-SP (15,360 channels)***
P3	03/2018	Non-uniform baseline, default gain configuration

MicroBooNE Experiment

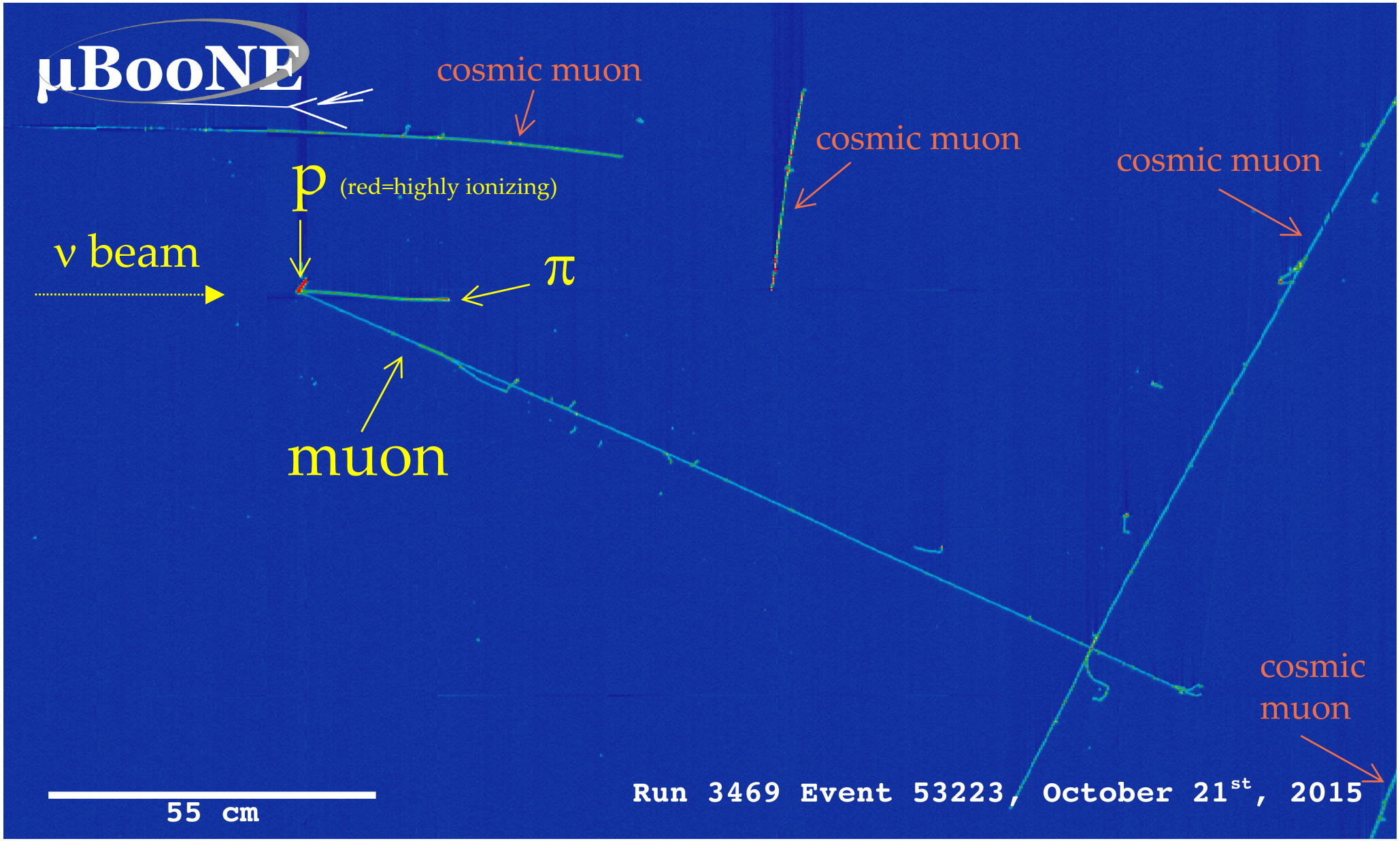
- 170 ton LAr TPC in the Fermilab Booster Neutrino Beamline

- MicroBooNE is also an important first step in the SBN program

- physics goals:
  - *address MiniBooNE low energy excess*
  - *make 1st low energy neutrino cross section measurements on Ar*

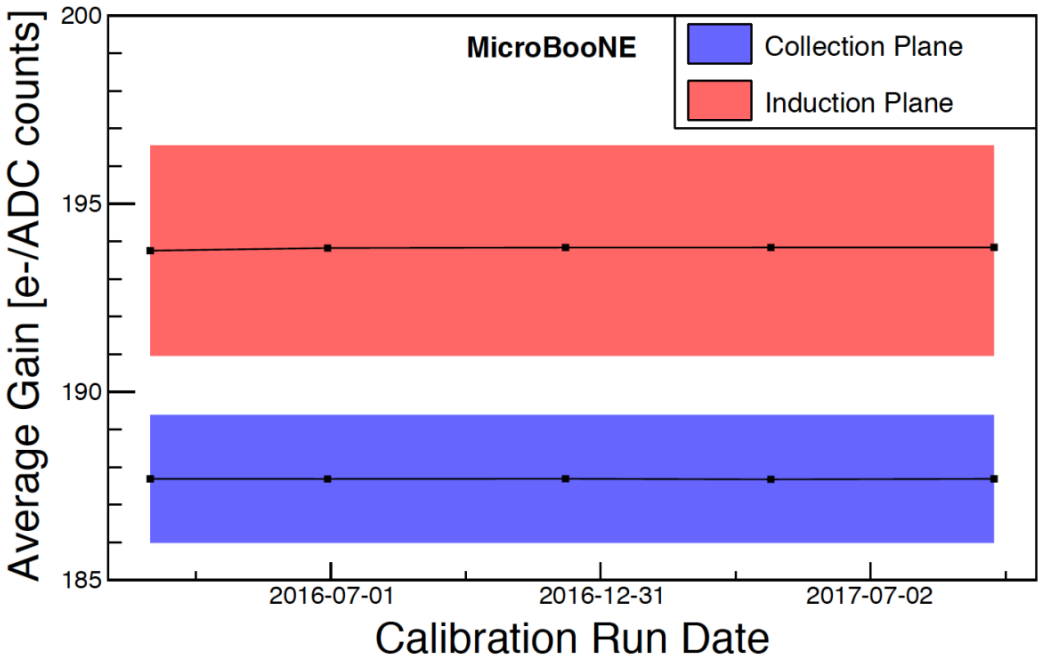
- technical advances:
  - *argon fill without evacuation* (*1st demonstrated in LAPD*)
  - ***cold front-end electronics***
  - *long drift (2.5m)*
  - *near surface operation*
  - *automated reconstruction*

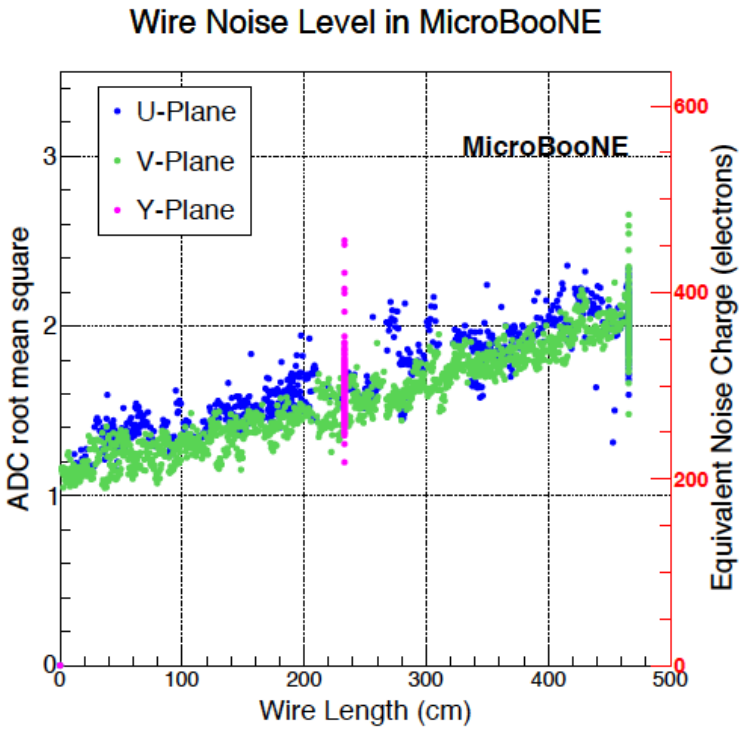
Start of Operations → First Neutrinos: October 15, 2015



more images here: https://microboone.fnal.gov/first-neutrino-event-candidates-in-microboone-november-2-2015/

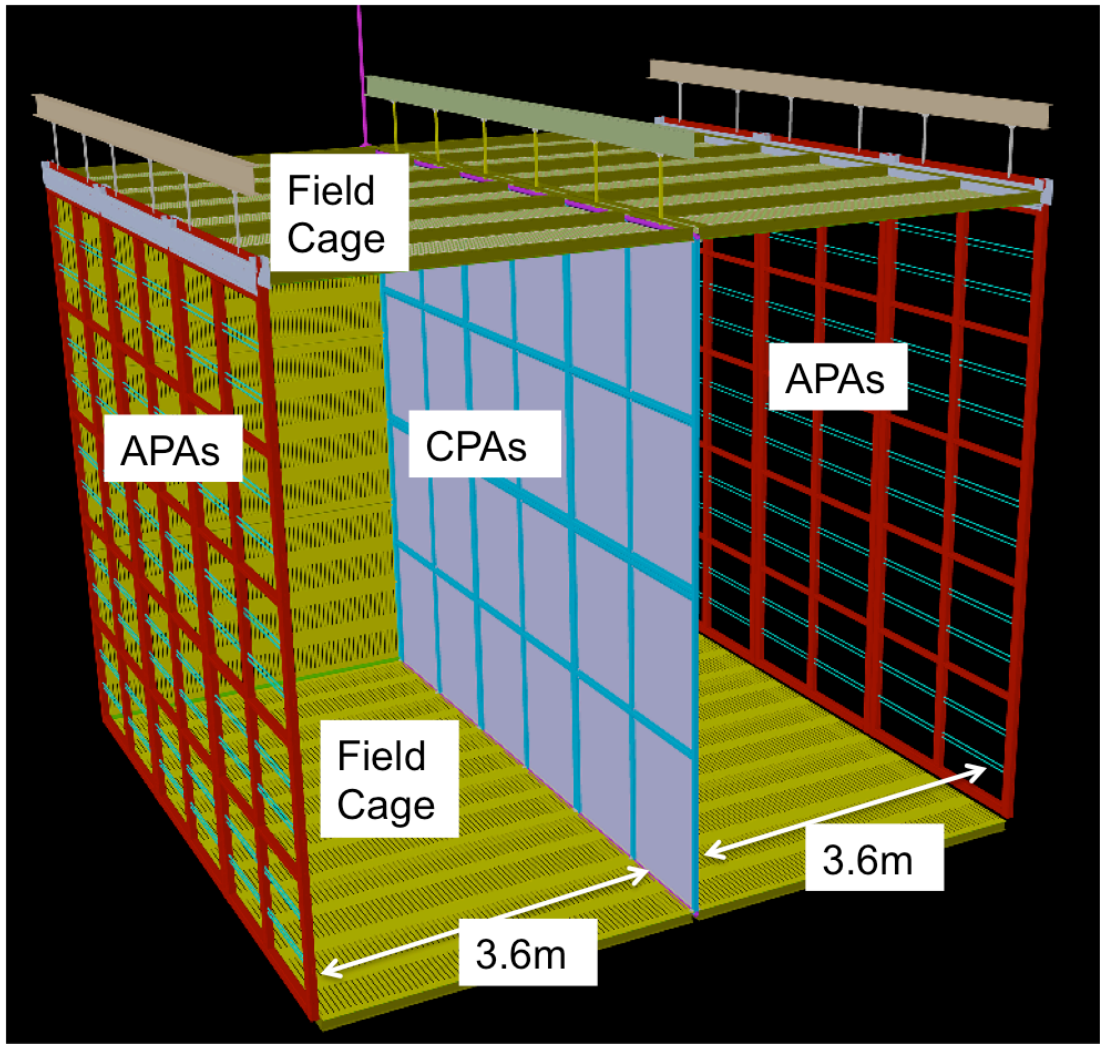
Excellent Stability and Performance of MicroBooNE TPC





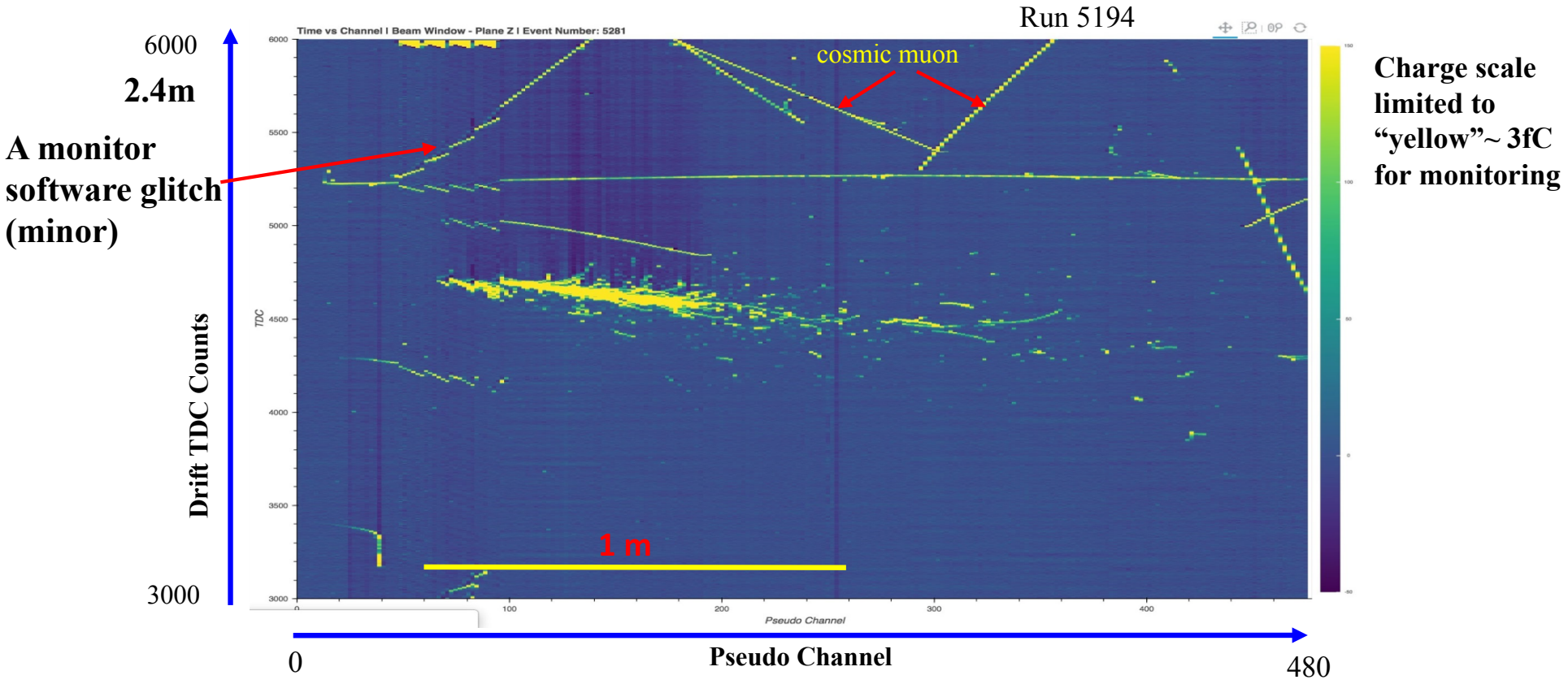
- MicroBooNE is the first experiment instrumented with cold CMOS ASICs, total ***8,256*** channels
  - S/N is improved by more than factor of 3 compared to previous large scale LArTPC experiment (e.g. ICARUS)
- Electronic calibration
  - Cold electronics gain stable over two year period, ***variation ~0.2%***
- Excellent noise performance
  - ENC after noise filtering is < **400 e^-** for 85% of channels, in agreement with bench tests of FE ASIC

ProtoDUNE-SP



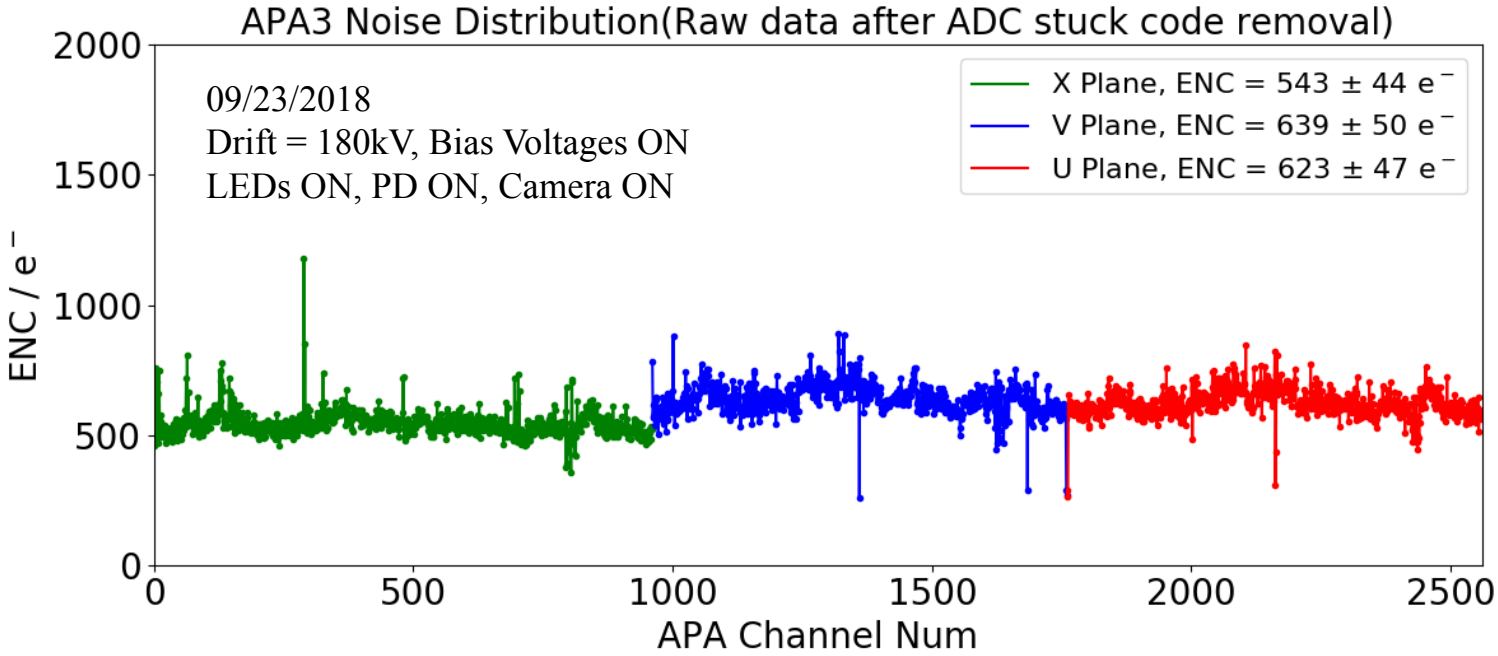
- Single-phase TPC prototype
  - Sit in H4 beam line in EHN1 @ CERN
  - Consisting of 6 full-size APA's plus CPA's → 2 x 3.6m drift regions
  - Total 15,360 TPC channels
  - Photon detectors with different fabrication methods
  - Successful operation in 2018 & 2019
- A key test platform for DUNE Far Detector:
  - Components
  - Construction methods
  - Installation procedures
  - Commissioning
  - Detector response to particles

An Example of EM Shower in ProtoDUNE



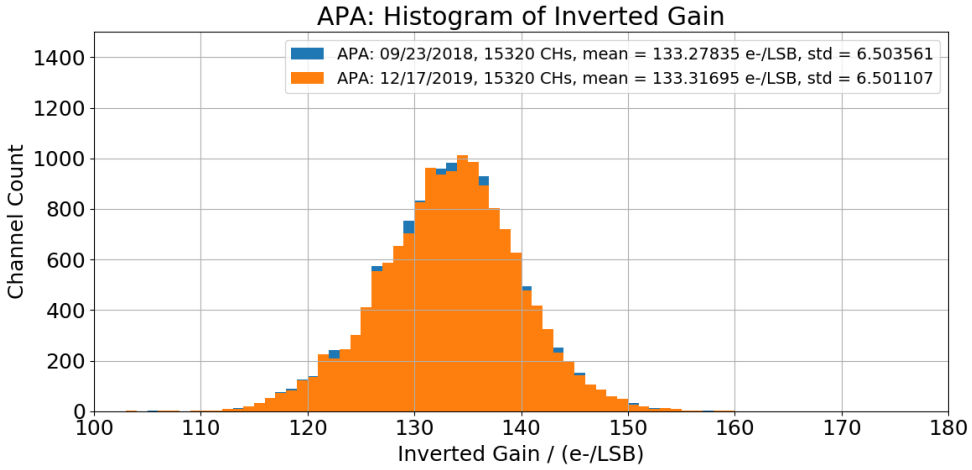
From Online Monitoring (Raw Data)

ProtoDUNE ENC Performance



- With drift 180kV and nominal bias voltages
  - **99.74% (15,320 of 15,360)** of TPC channels are active regardless of noise performance
  - Only 6 inactive FE channels, others can be attributed to TPC etc.
- Noise performance with drift and bias on
  - ENC of collection (X) plane (5,473 of 5,760 channels): **565 ± 60 e-**
  - ENC of induction (V) plane (4,347 of 4,800 channels): **662 ± 56 e-**
  - ENC of induction (U) plane (4,439 of 4,800 channels): **651 ± 54 e-**

Excellent Stability and Performance of ProtoDUNE TPC



Plane	Peak signal-to-noise ratio			
	Raw Data		After Noise Filtering	
	MPV	Average	MPV	Average
Collection	30.9	38.3	40.3	48.7
U	12.1	15.6	15.1	18.2
V	14.9	18.7	18.6	21.2

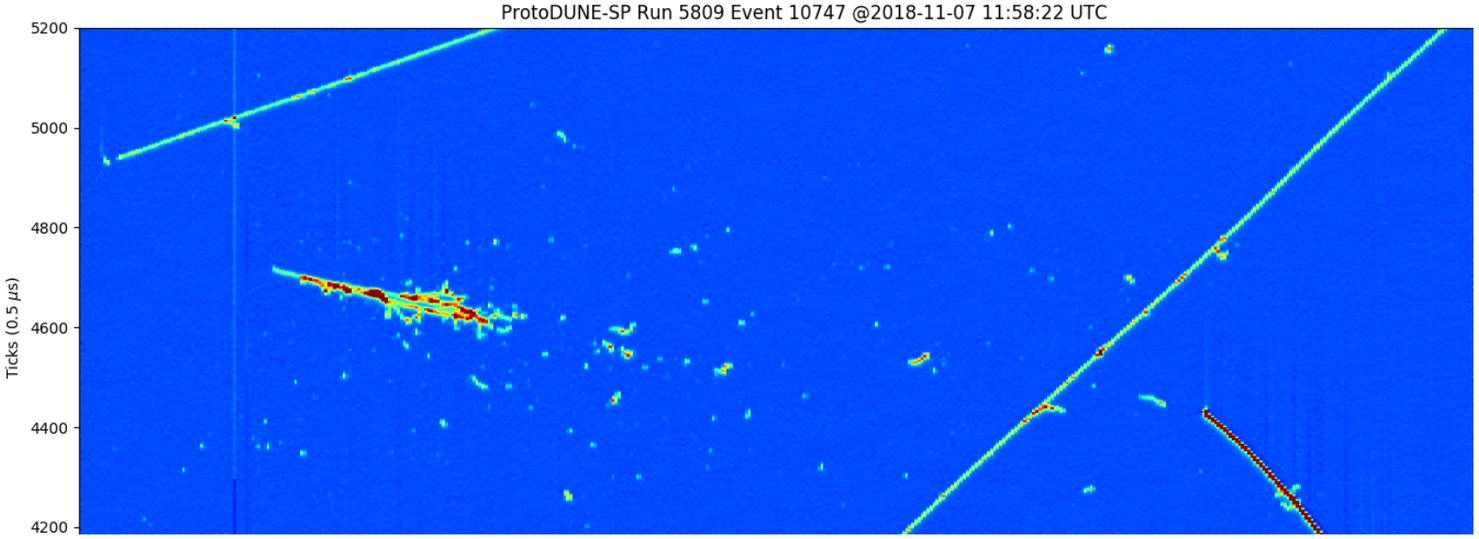
- Gain is stable over 15 months of operation
  - Variation < 0.05%
- Excellent Signal to Noise Ratio of the full system
  - Signal: detected Charge (*hit Peak-amplitude)* in individual channel waveform (from U,V,C wire-plane) from mip tracks corrected by angle of incidence
  - Noise: σ of baseline fluctuation in corresponding channel waveform

Summary

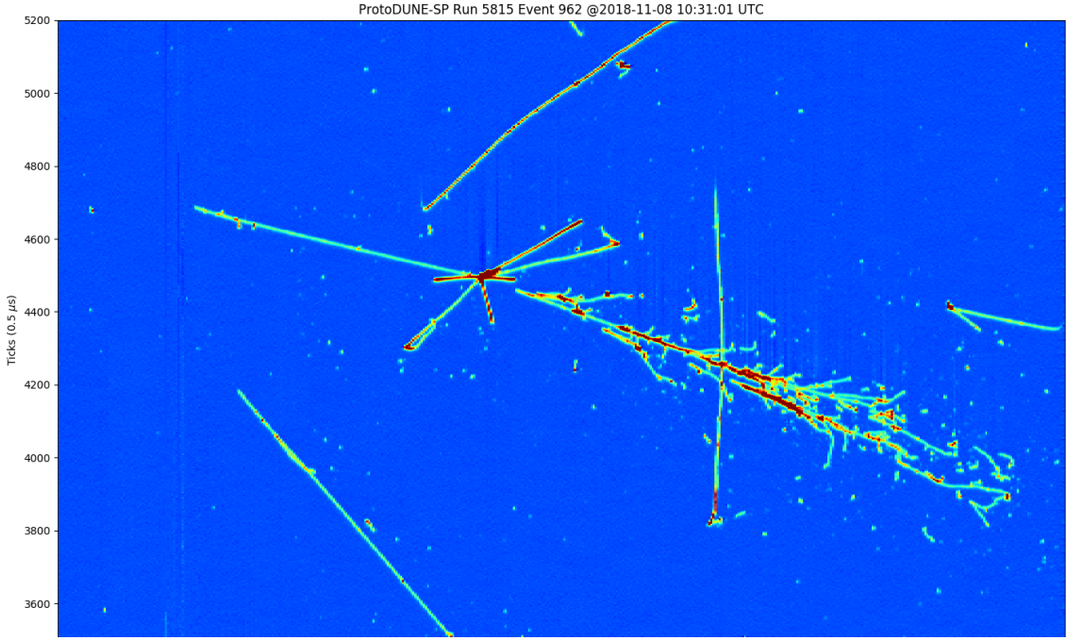
- R&D of CMOS cold electronics started in 2008
  - First analog front-end ASIC was designed in 2010
- FE ASICs have been used to instrument MicroBooNE (V4*) and ProtoDUNE (P2) LArTPCs ***successfully***
- Cold FE ASIC is continuing development towards a robust design adaptable to future design rule and process technology changes
  - P3 FE ASIC has been fabricated and evaluated in the lab
  - Development of P4 FE ASIC is ongoing, with plan to address the ledge effect (see Shanshan's ASIC talk) and add SE-DIFF converter

Backup Slides

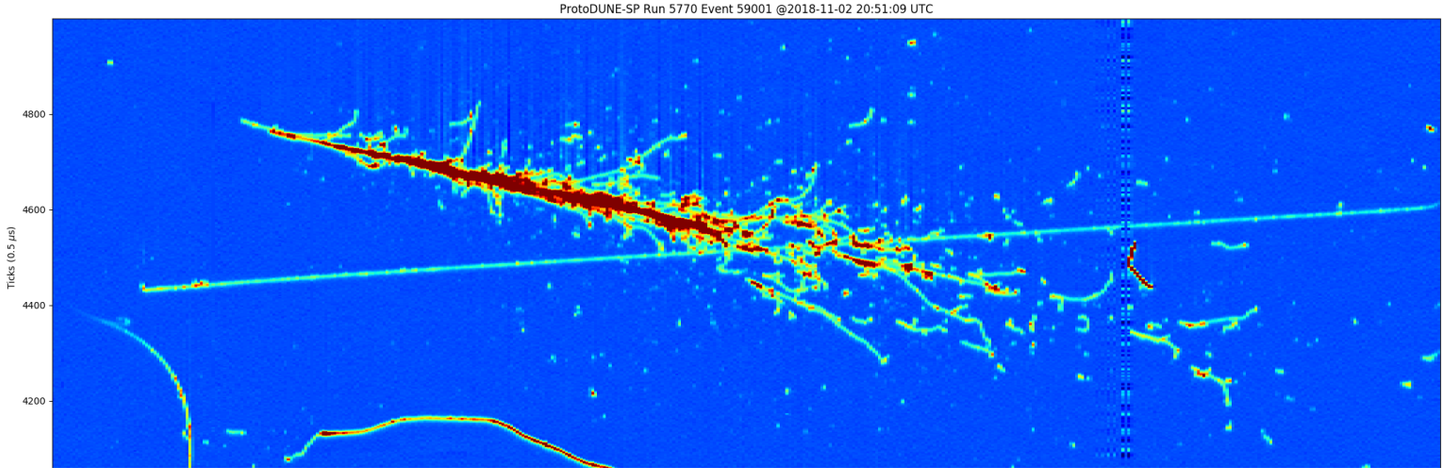
ProtoDUNE-SP Run 5809 Event 10747 @2018-11-07 11:58:22 UTC



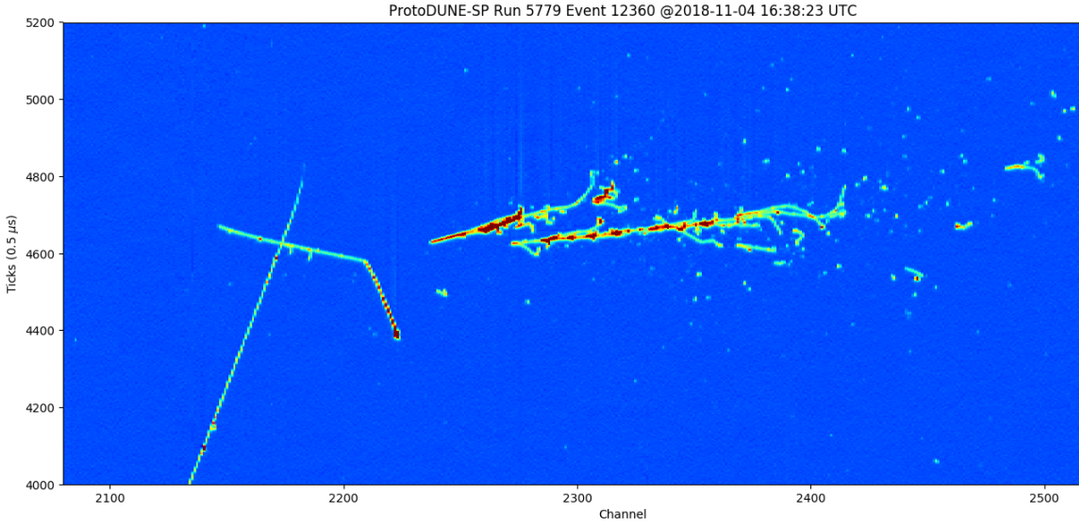
ProtoDUNE-SP Run 5815 Event 962 @2018-11-08 10:31:01 UTC



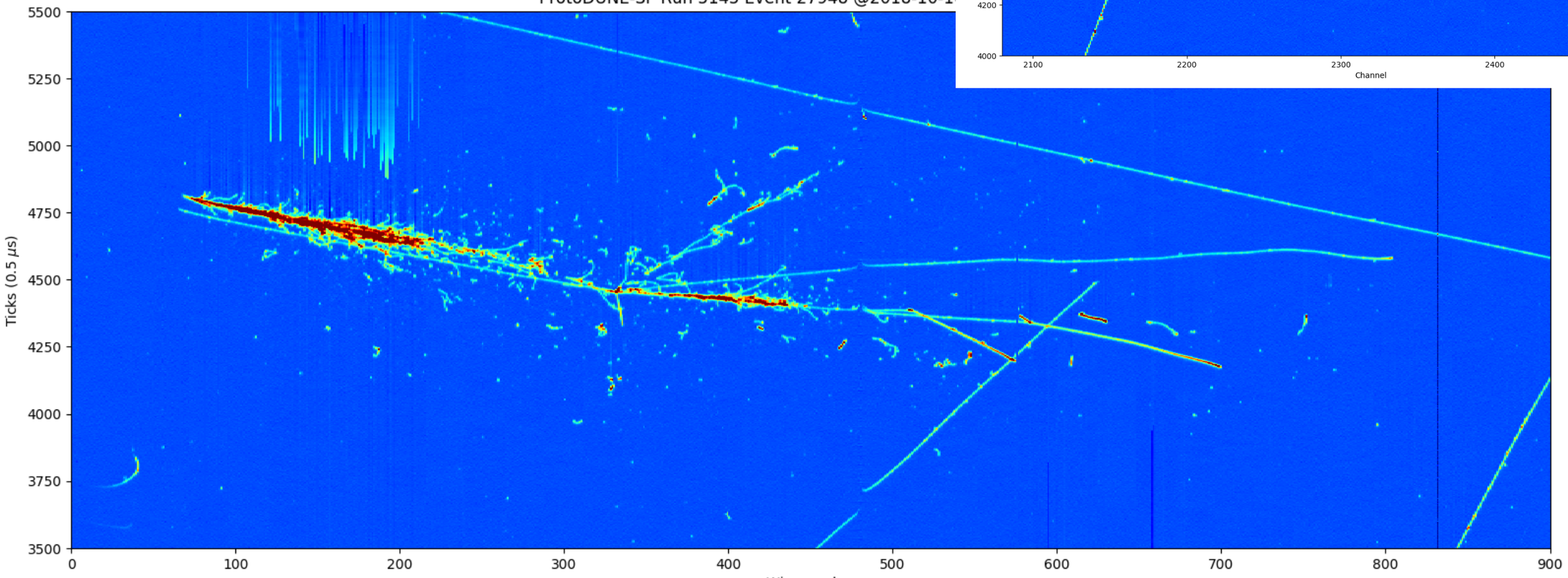
ProtoDUNE-SP Run 5770 Event 59001 @2018-11-02 20:51:09 UTC



ProtoDUNE-SP Run 5779 Event 12360 @2018-11-04 16:38:23 UTC



ProtoDUNE-SP Run 5145 Event 27948 @2018-10-1



ProtoDUNE-SP Run 5770 Event 50648 @2018-11-02 20:32:06 UTC

Ticks (0.5 μs)

Wire number

Charge (ke)

ProtoDUNE-SP Run 5772 Event 15132 @2018-11-03 10:09:15 UTC