BROOKHAVEN NATIONAL LABORATORY

DUNE DEEP UNDERGROUND NEUTRINO EXPERIMENT

# LArASIC - FE ASIC for DUNE LAr TPC

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U.S. DEPARTMENT OF ENERGY | Office of Science

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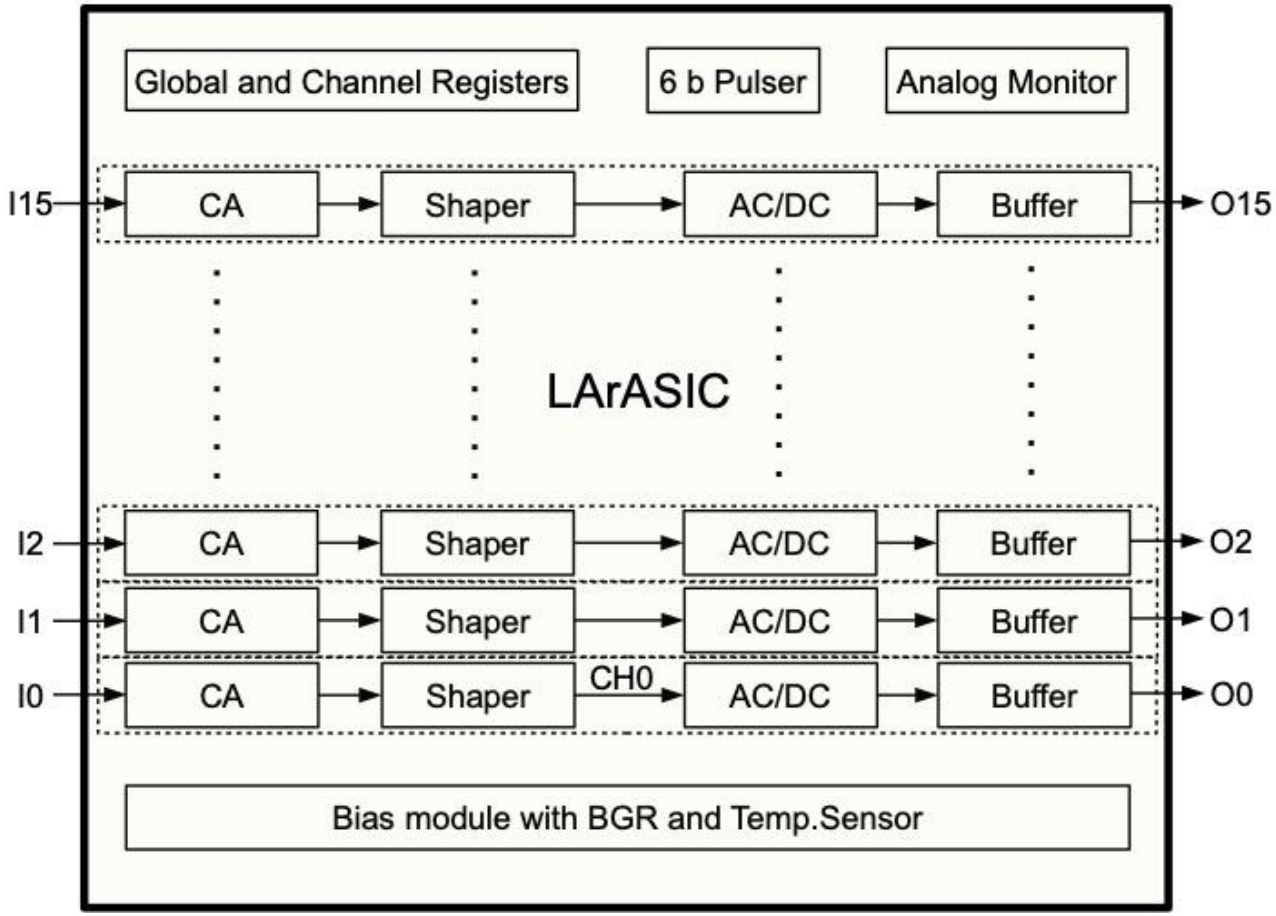
# Outline

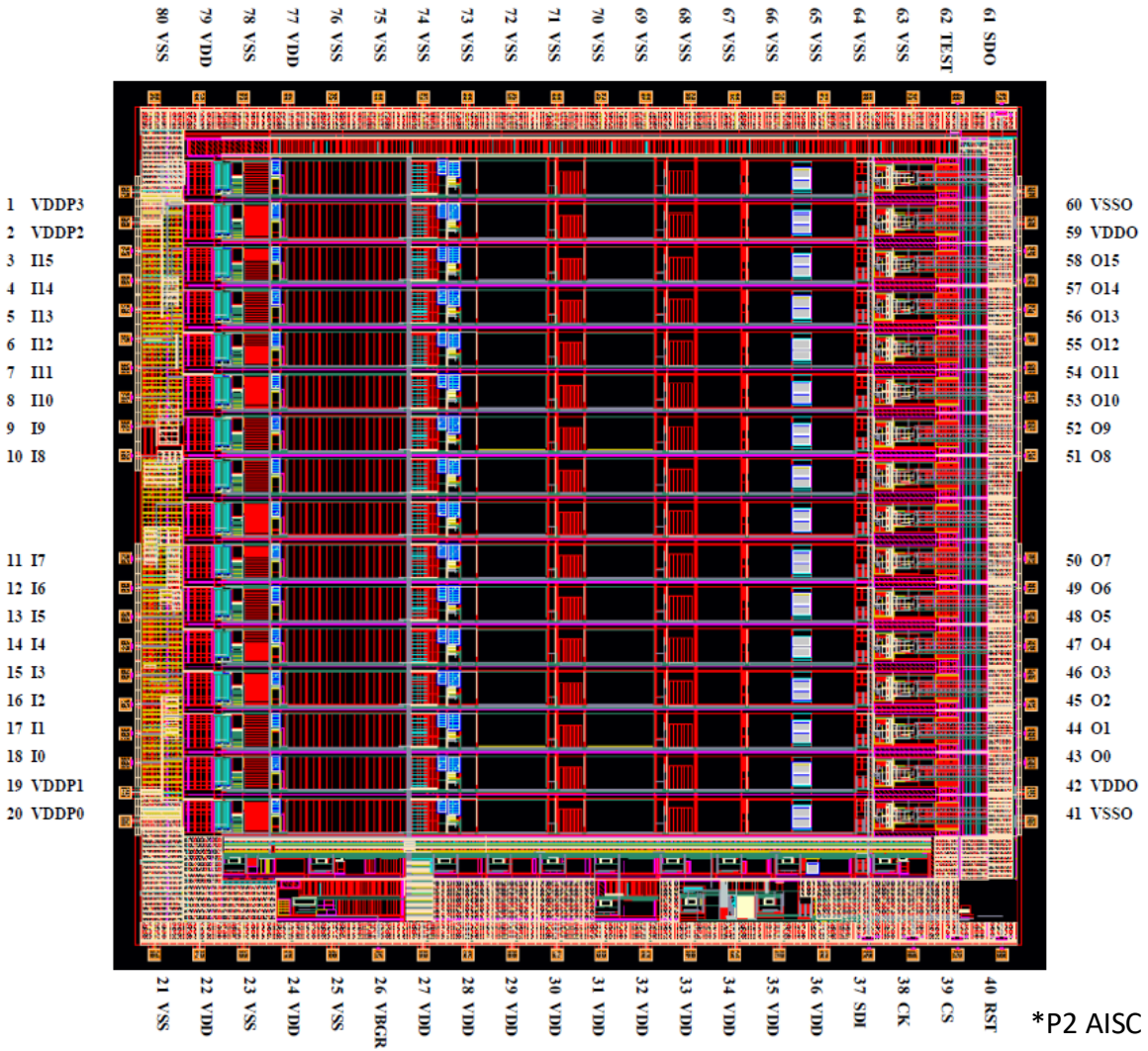
- LArASIC Introduction
- Changes Between Recent LArASIC Versions
- LArASIC P3 Simulations and Identified Issues
- LArASIC P4 Development
- LArASIC P4 Simulations
- Summary and Future Work

# LArASIC – Simplified block diagram & functionality




- 16 channels
- Two-stage charge amplifier, high-order filter (5$^{th}$)
- Adjustable Reset Quiescent Current (RQI/leakage) settings (100 pA, 500 pA, 1nA, 5 nA)
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (Max. charge 55, 100, 180, 300 fC)
- Adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 µs)
- Selectable collection/non-collection mode
  (baseline 200, 900 mV)
- Selectable DC/AC coupling (100µs HPF time-const.)
- Rail-to-rail analog signal processing with single-ended buffer
- Bandgap referenced (BGR) biasing circuits
- Temperature sensor (~ 3mV/°C)
- Integrated 6-bit pulse generator
- 144 configuration registers, SPI interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- ~ 16,000 MOSFETs
- Designed for room (300K) and cryogenic (77K) operation
- Technology CMOS 0.18 µm, 1.8 V, 6M, MIM, SBRES

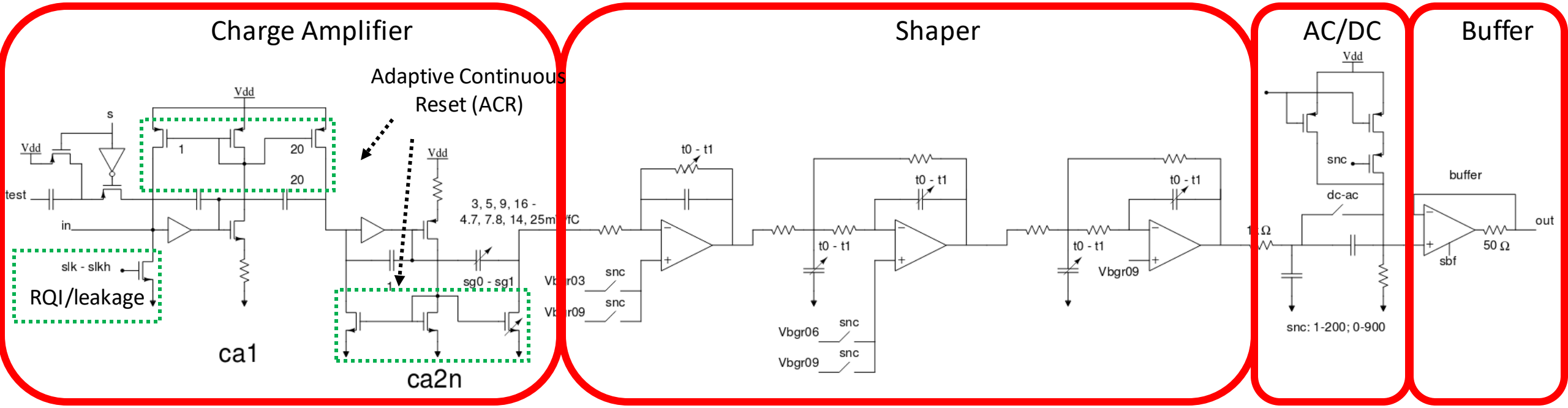
# Previous FE ASIC layout




*P2 AISC

Successful deployment with excellent performance at MicroBooNE and ProtoDUNE

# LArASIC Channel – Simplified block diagram



# Changes between recent versions of the FE ASIC

## P1 (V6)

- 6-bit pulse generator added
- SLKH, i.e., high (10x) Reset-loop Quiescent Current (RQI) added to compensate for saturation effects (aka “Chirping”)
- BGR fix didn’t work → 7% chips don’t start in cold
- RQI subtraction added in CA2 to correct for BL DC for 5nA RQI → CA2 Adaptive Continuous Reset (ACR) non-functional → needs 1GOhm at input
- Transistor sizing similar to V5
- Imperfect PZ cancellation → return to baseline issues

## P2 (V7)

- PA-SH changed to correct return to baseline issue
- Removed RQI subtraction in CA2
- Changed W and L in the ACR of CA1 and CA2
  - {W,L} in ACR CA2, P2 = {8*W, 8*L} ACR CA2, P1
- Inter-channel BL variation (geometric dependence) for 200 mV BL option observed due to packaging stress
- Ledge observed only in cold during shower event (after P3 tape-out)
- BGR issue of 7% chips in cold still present

## P3 (V8)

- Geometric dependence for 200 mV baseline mitigated by replacing current biasing with voltage in shaper 1$^{st}$ and 2$^{nd}$ stages → changes CA2 bias vol.
- Ledge behavior still present in cold
- BGR issue of 7% chips in cold still present

# Outline of Identified problems and simulation methodology

- Identified problems
  - Bandgap Voltage Reference (BGR) fails in 7% of the chips
  - Ledge effect during shower event

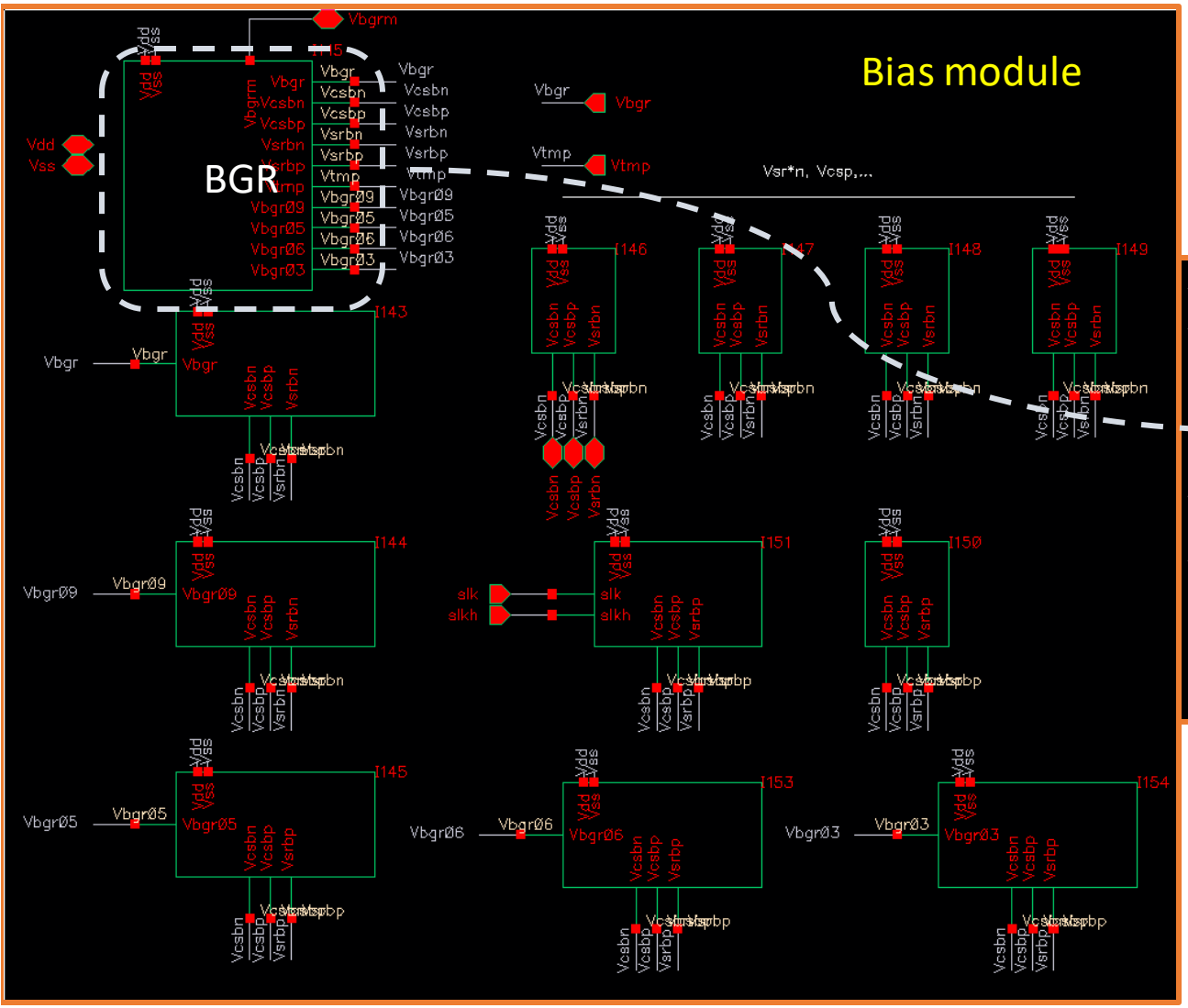
  } Only in Cold operation

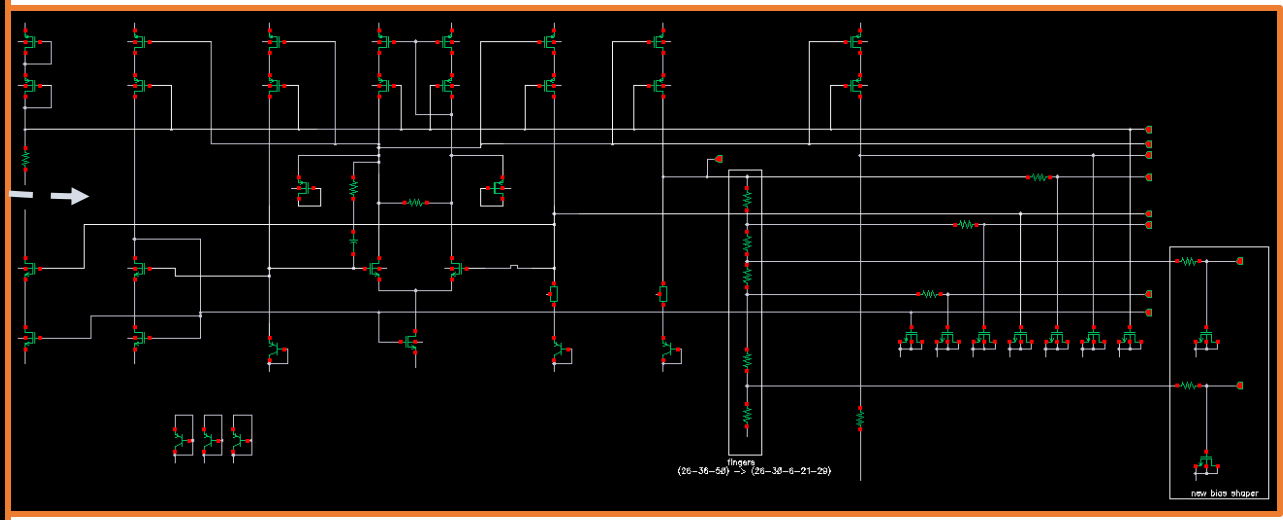
- Simulation procedure
  - Model files from foundry used
    - "cmno18_asp_v1d2.scs" in BSIM4 (V4.5)
    - Extrapolated for LN and LAr temperatures, outside of guaranteed range
    - Mismatch models only for MOSFETs
  - Perform different analysis needed such as DC, AC, stability (STB), noise , transient (with or/and without noise) in nominal, process corners (SS, FF, SF and FS) and Monte Carlo with process variation (PV) and mismatch (MM)
  - Schematic level simulations have been shown later

# BGR Problem in P3

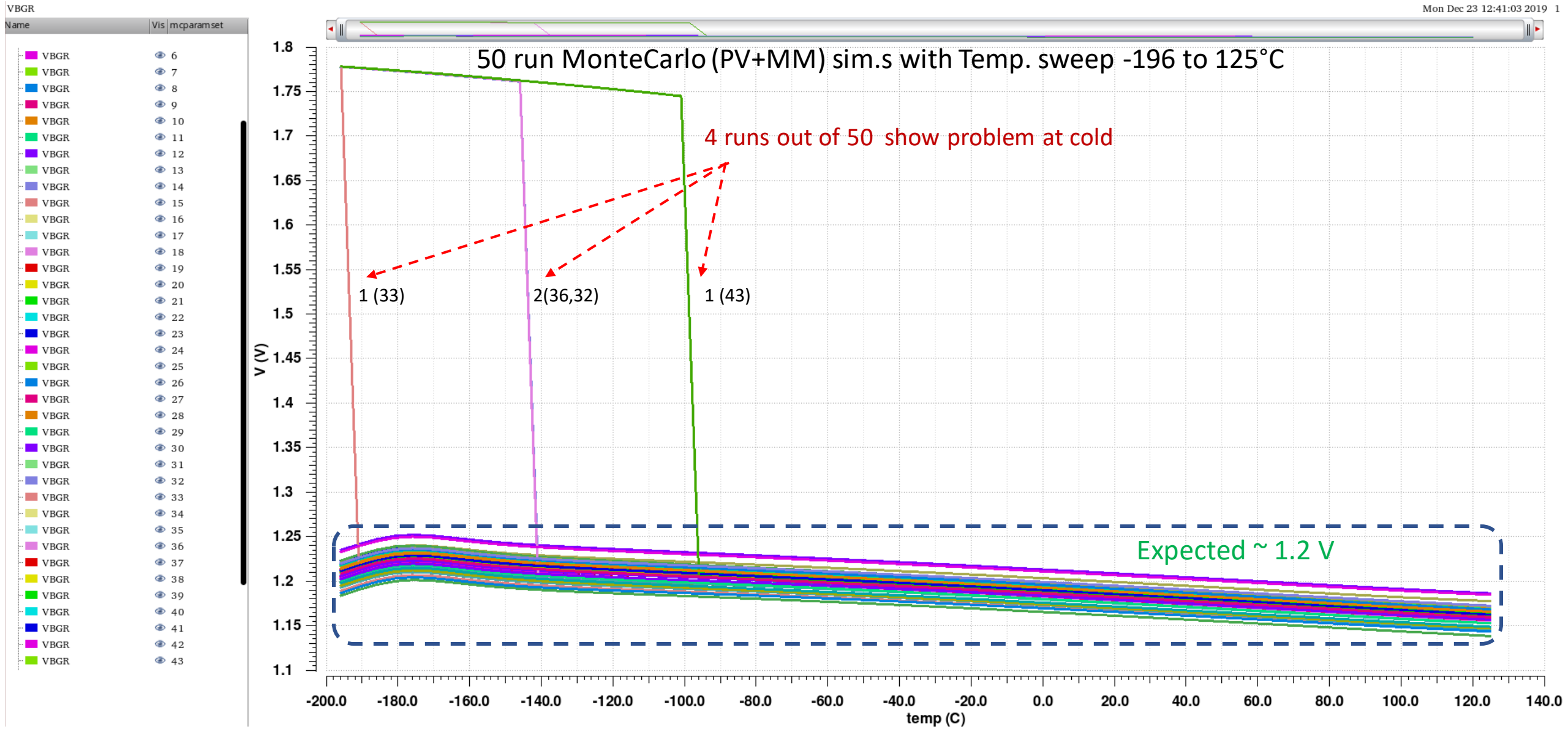
# Bias module based on Bandgap Voltage Reference (BGR)

- Still 7% of the P3 chips doesn't start only in cold → They are currently screened-off

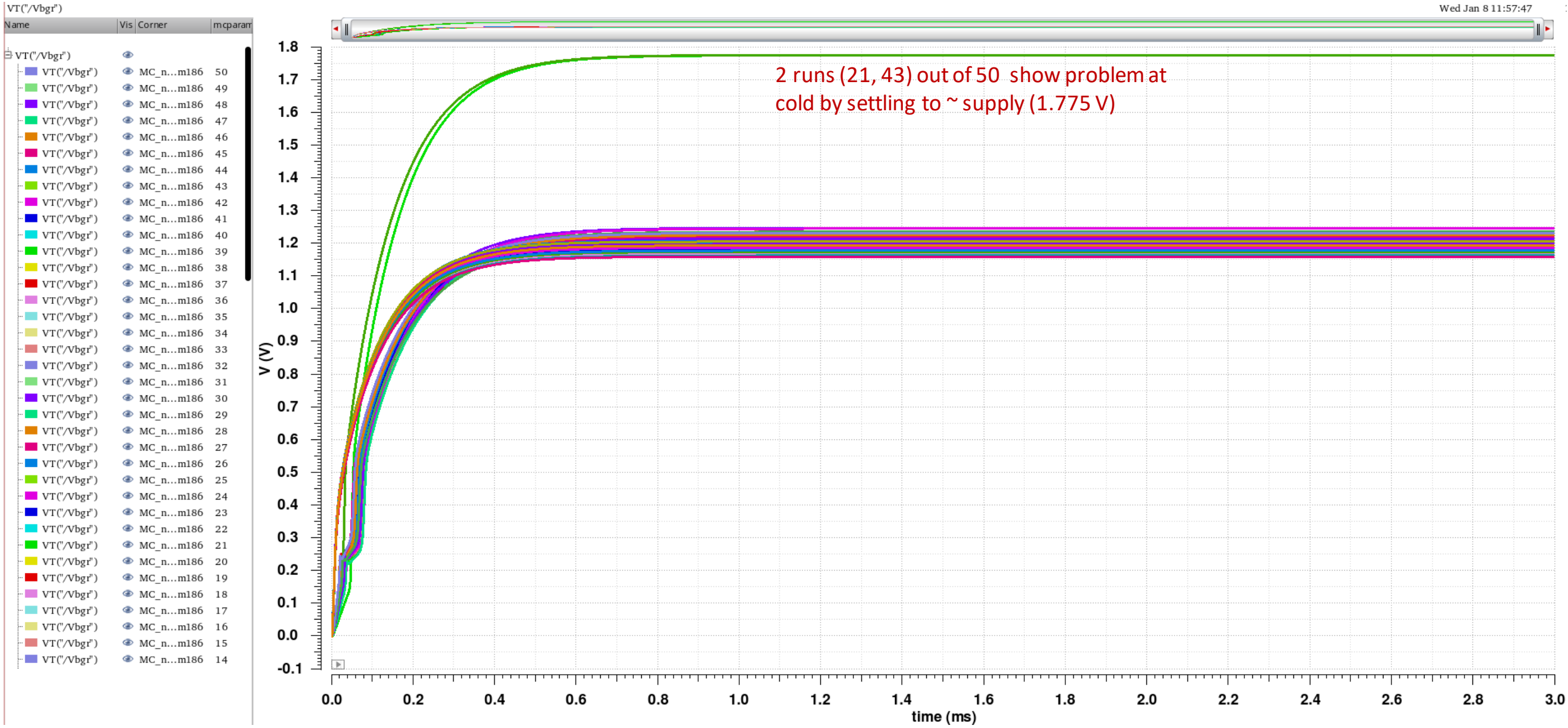


# P3 BGR simulations



# Start-up sim.s of P3 BGR




1µs supply ramping; 50 run MC (PV+MM) at LAr and RT

# Ledge Effect in P3

# Ledge effect in LArASIC P3

- Only during cold operation and mostly with shower charge (e.g. > 100 fC for 14 mV/fC setting) for 200 mV baseline setting, LArASIC P2 and P3 outputs of some of the channels saturate and produce ledge characteristic after a delay

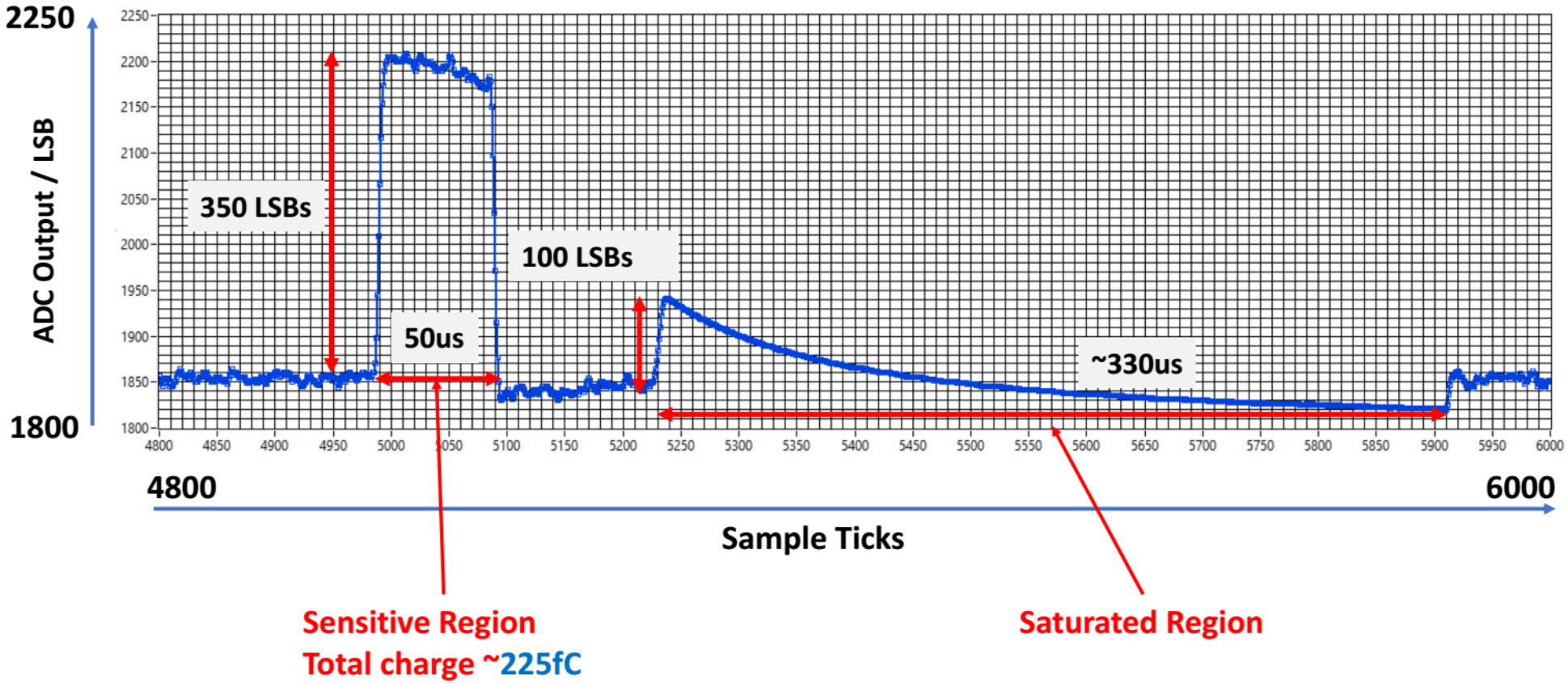
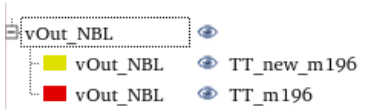


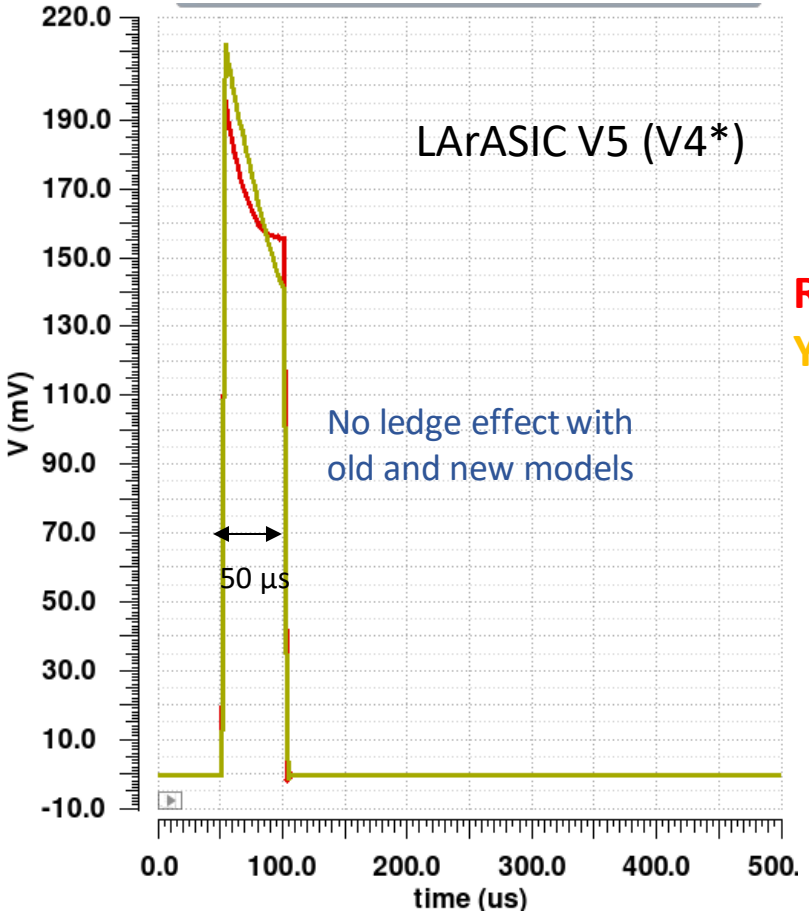

Image from: Study of the “Ledge” effect in protoDUNE readout, Hucheng Chen, et al.

# Simulation of shower event at LN : 500 fC input for 50 µs

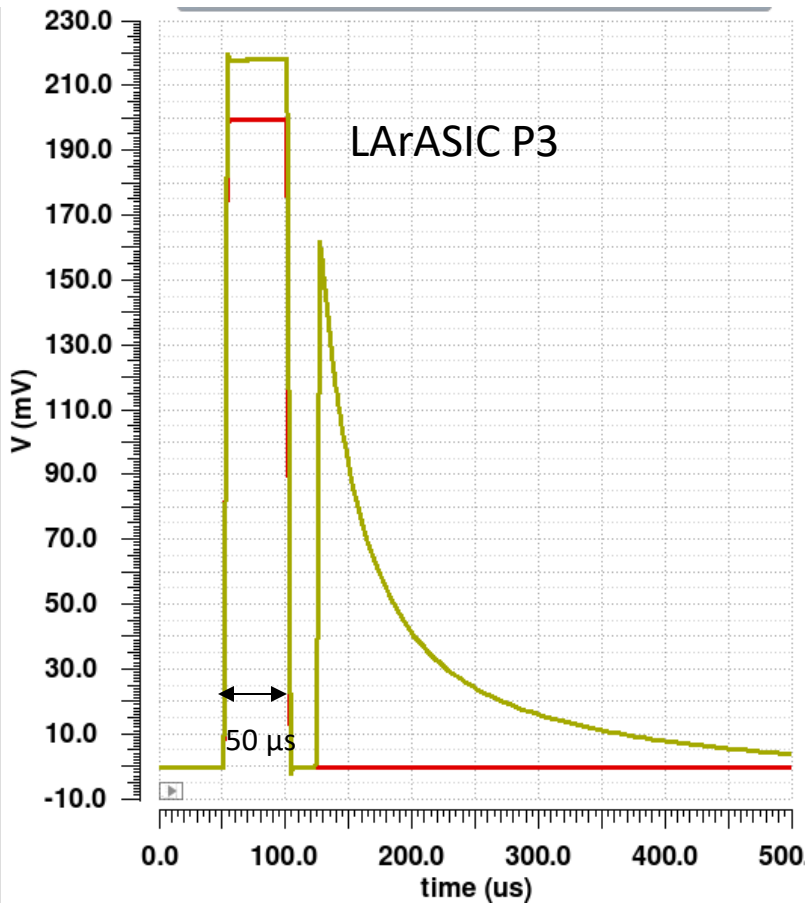
Ledge effect only observed with new models (BSIM4) and not with old (BSIM3)




tPeak = 1 µs
Leakage = 500 pA
BL = 200 mV
Gain = 14 mv/fC
Cdet = 150 pF




**Red: old model**
**Yellow: new model**

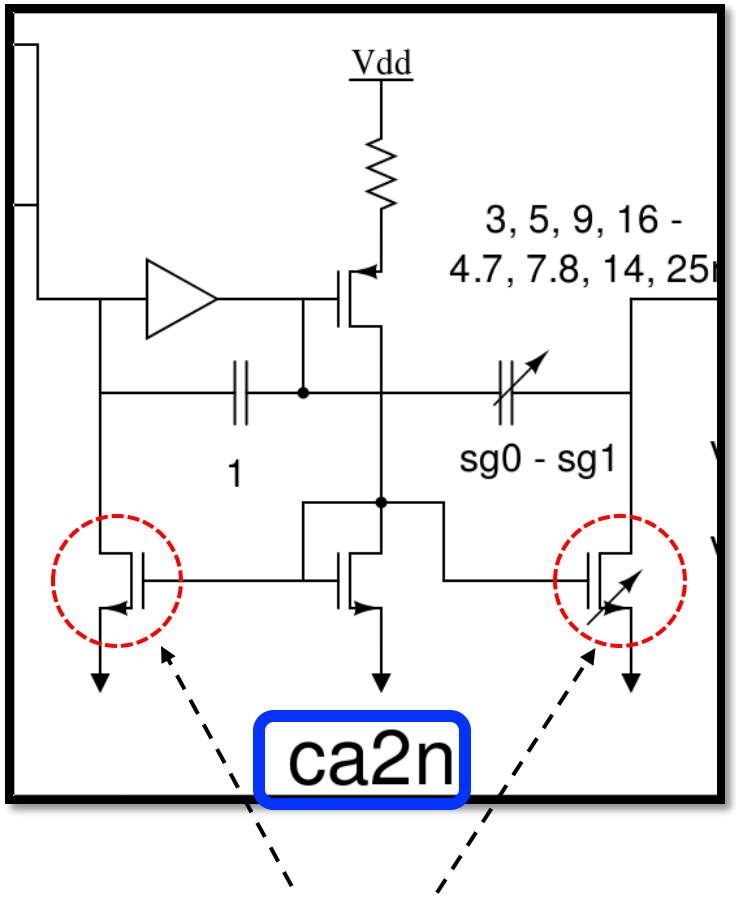

TT_m196 → rf018.scs is BSIM3 (V3.24) ~17k lines
TT_new_m196 → cmno18_asp_v1d2.scs is BSIM4 (V4.5) ~38k lines

} 180 nm TSMC tech. model files

# Origin of ledge effect

- Adaptive Continuous Reset(ACR) network in the ca2n resized from V5(V4*)/V6(P1) moving to V7(P2)/V8(P3) to improve pole-zero cancellation (baseline restoration)
- Width and Length of the transistors in ACR increased by 8 times in P3 compared to V5, increased gate cap. by ~64 times, making the loop unstable, causing ledge

Ledge effect origin fully understood

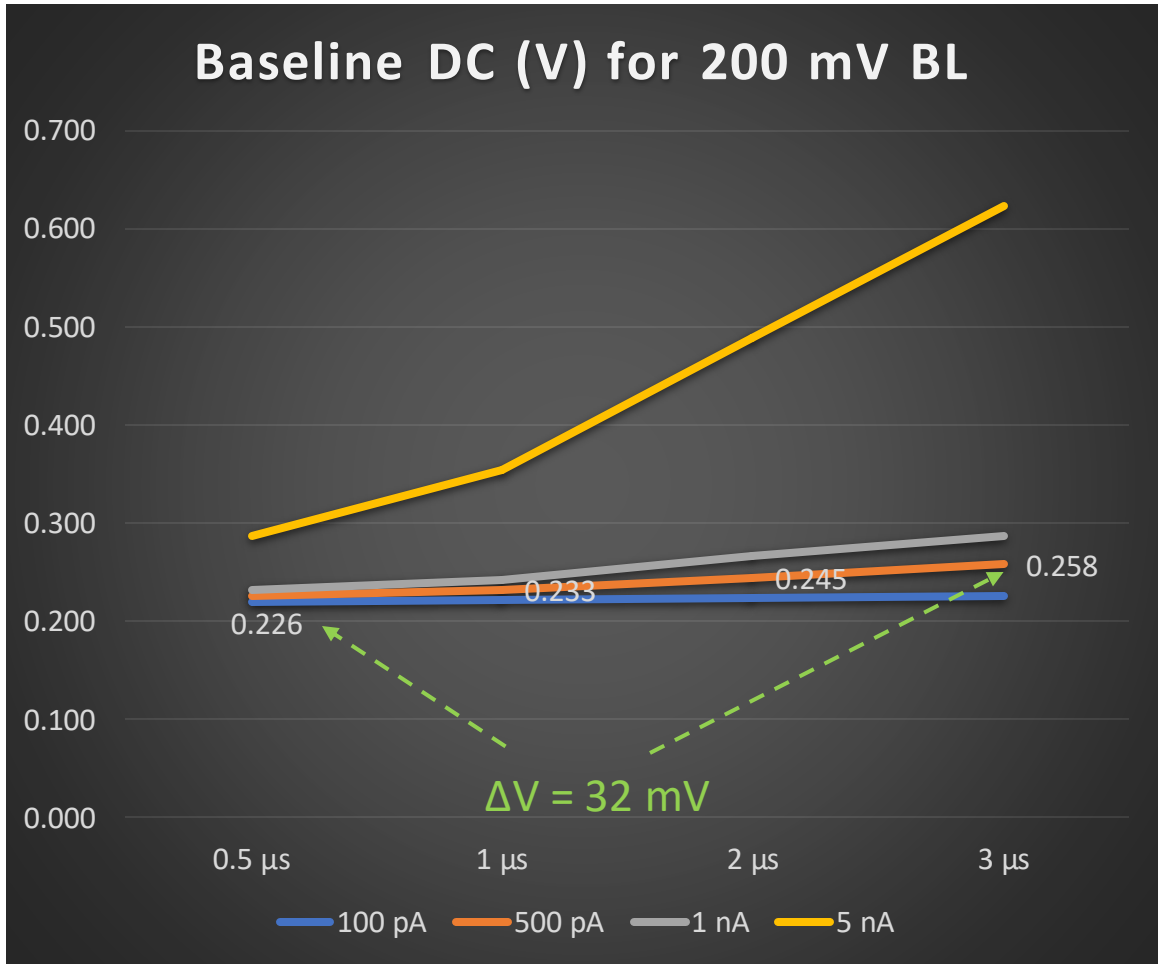


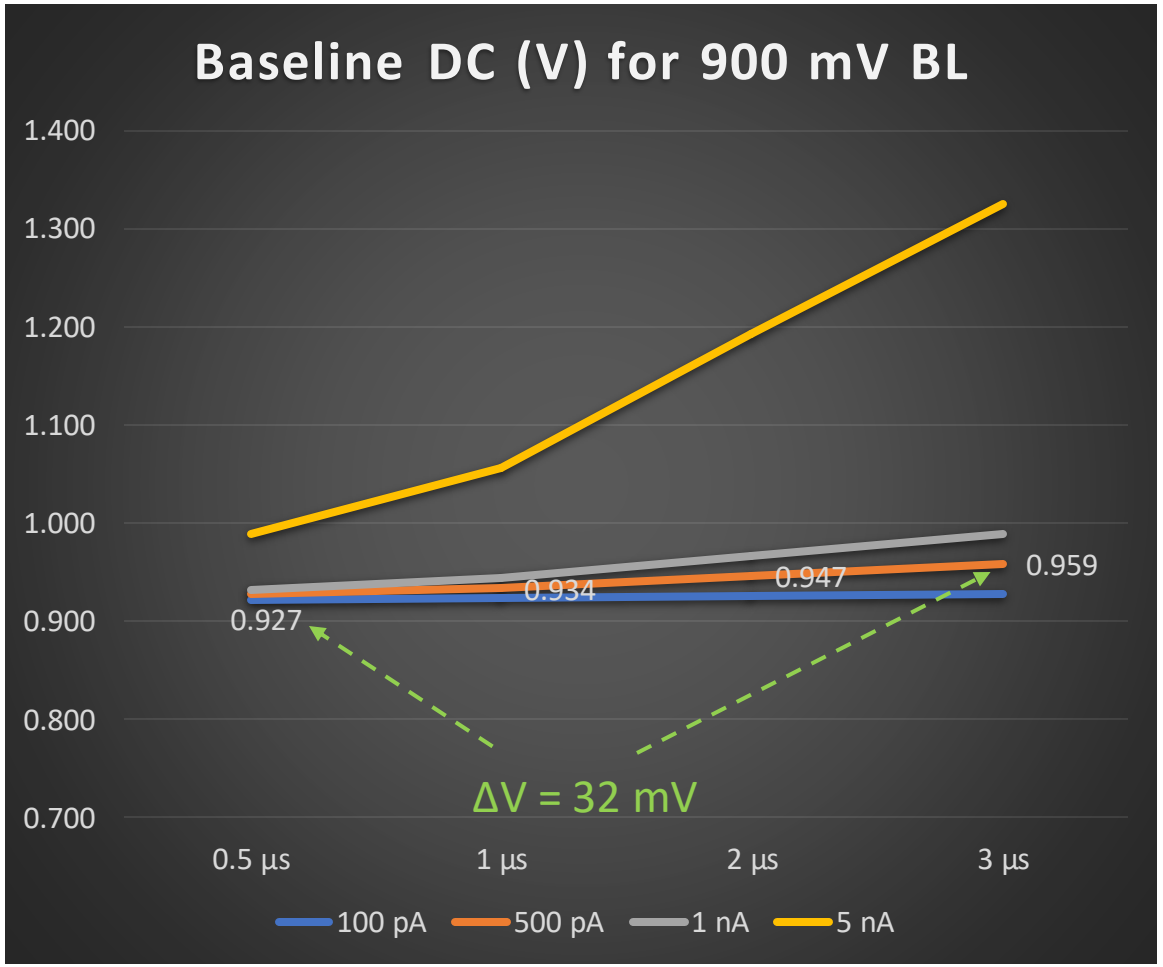

Both W and L increased by 8 times

# Other Performance Metrics of P3

# Simulations of P3 channel baseline DC shift for different settings

* Setting: BL = 200/900 mV, Gain = 14 mV/fC, Cdet = 150 pF



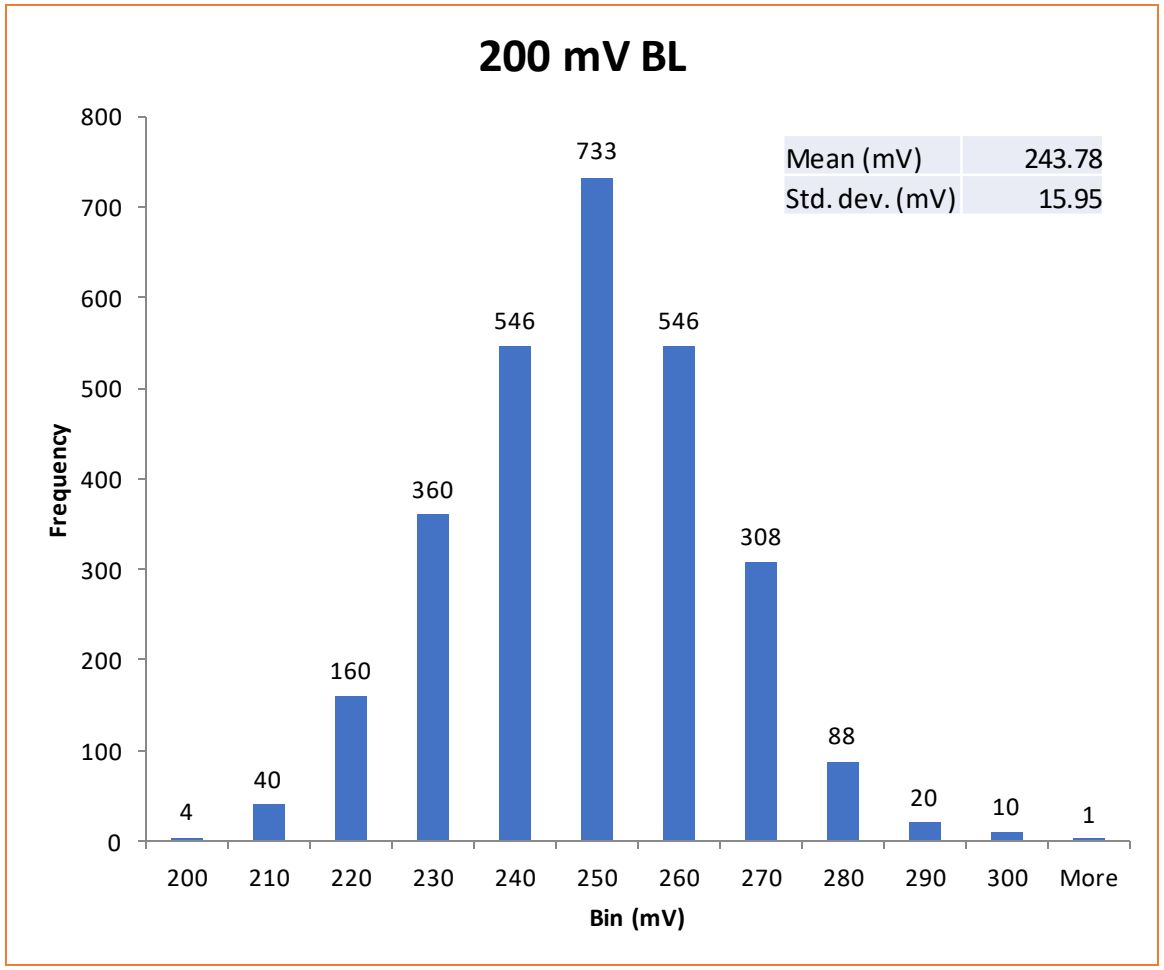



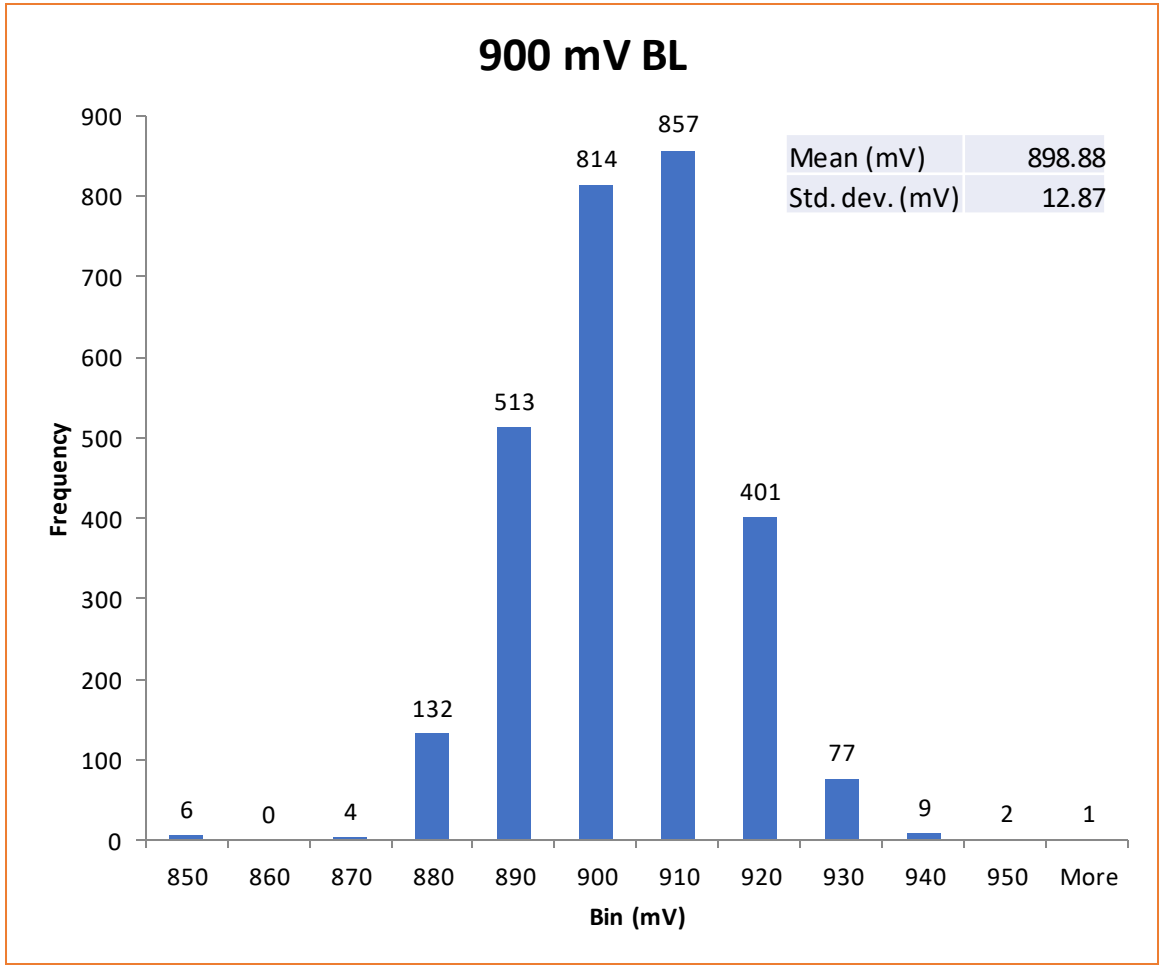

RQI (leakage) setting of 500 pA mostly used and 5 nA is not needed

Baseline shift reduces signal swings

# P3 ASIC baseline DC variation in LN – Measurement of 171 chips, 2736 channels

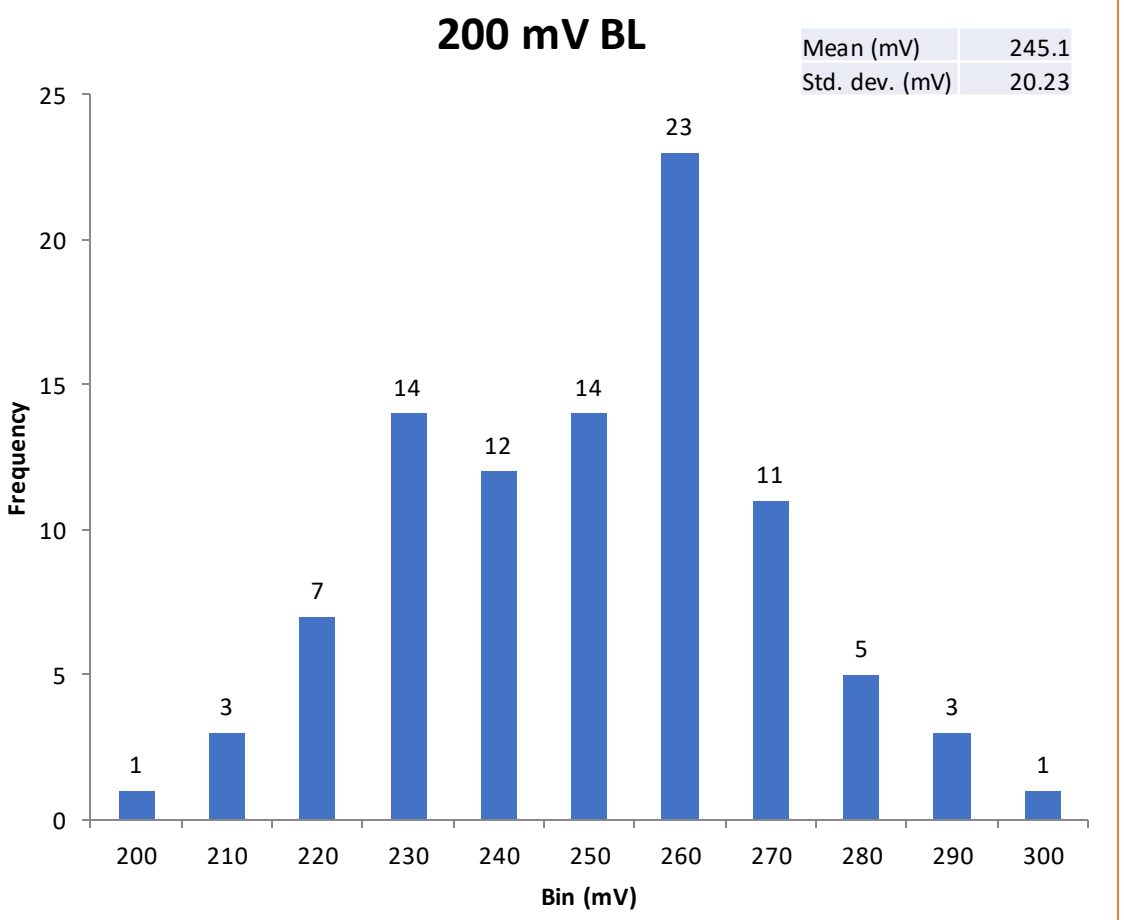
Setting: BL = 200/900 mV, Gain = 14 mV/fC, Tp = 2 us, DC, Buffer on, 500pA.
1.6% had unresponsive channels and 4.79% did not respond after a power cycle in LN

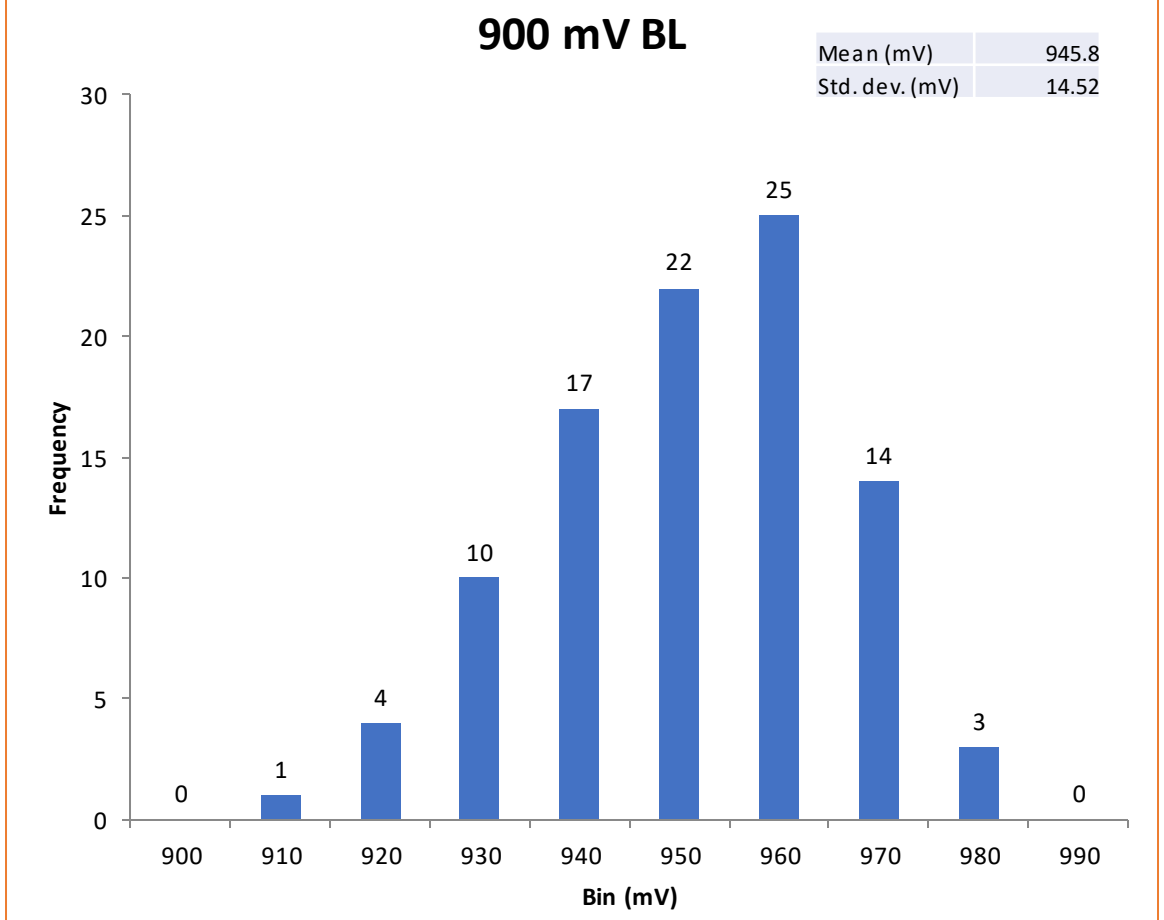


# P3 FE ASIC baseline DC variation in LN – MC simulations

100 run MC simulations (PV+MM) at schematic level
Setting: BL = 200/900 mV, Gain = 14 mV/fC, Tp = 2 us, DC coupling, Buffer not used, 500pA, Cdet = 150 pF
Bandgap reference voltage problem (1.78 V instead of 1.2 V) in 6% (200 mV BL) and 4% (900 mV BL) simulation runs

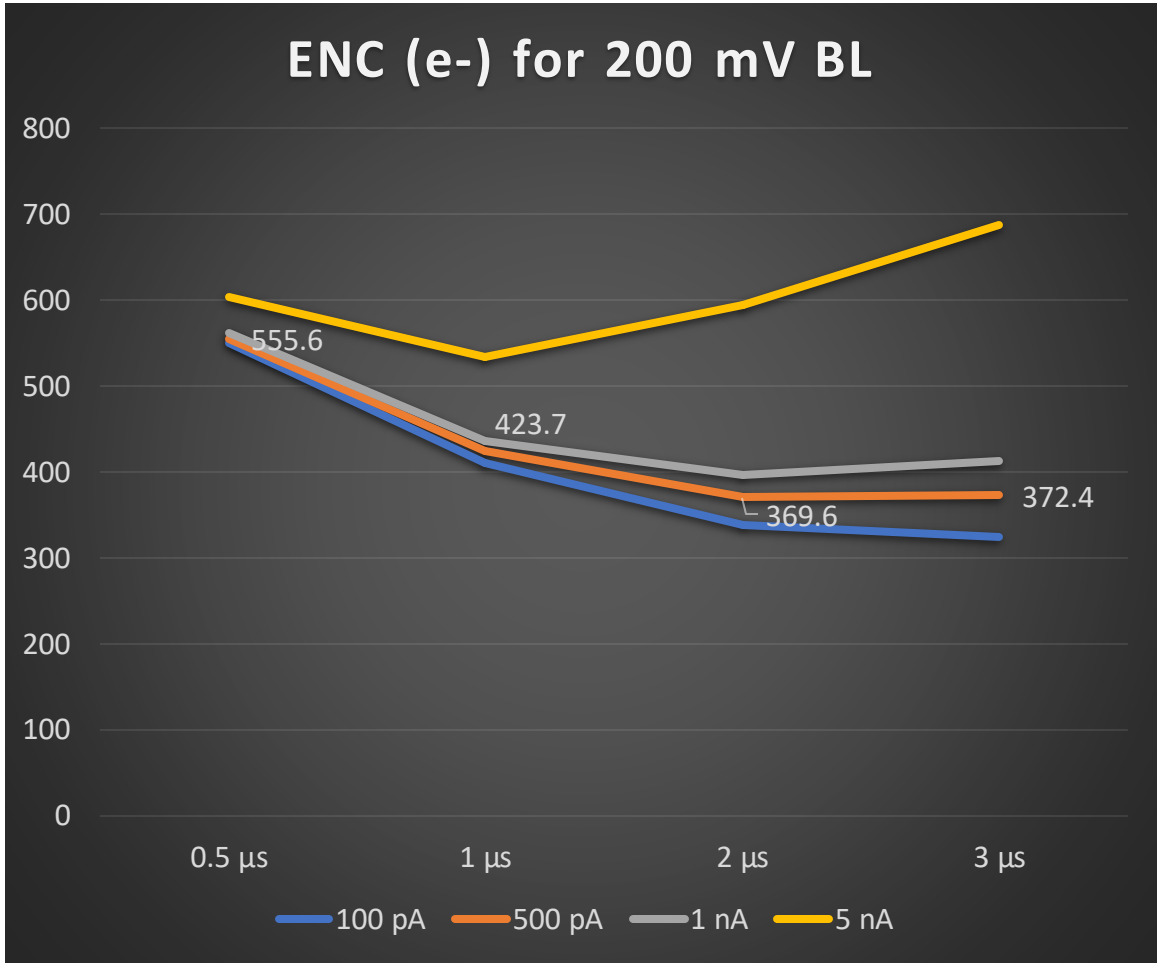


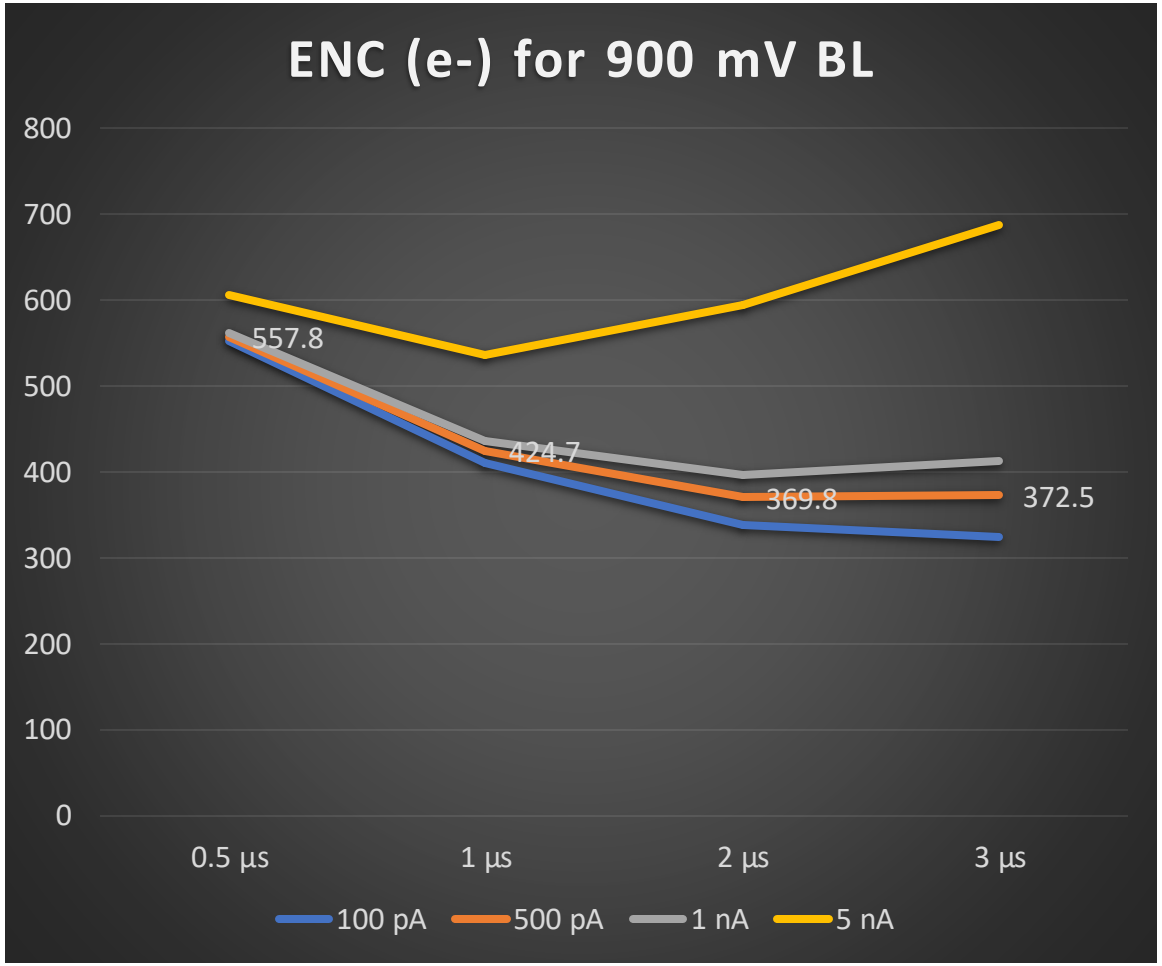




Close to measurements

# Simulations of P3 channel ENC

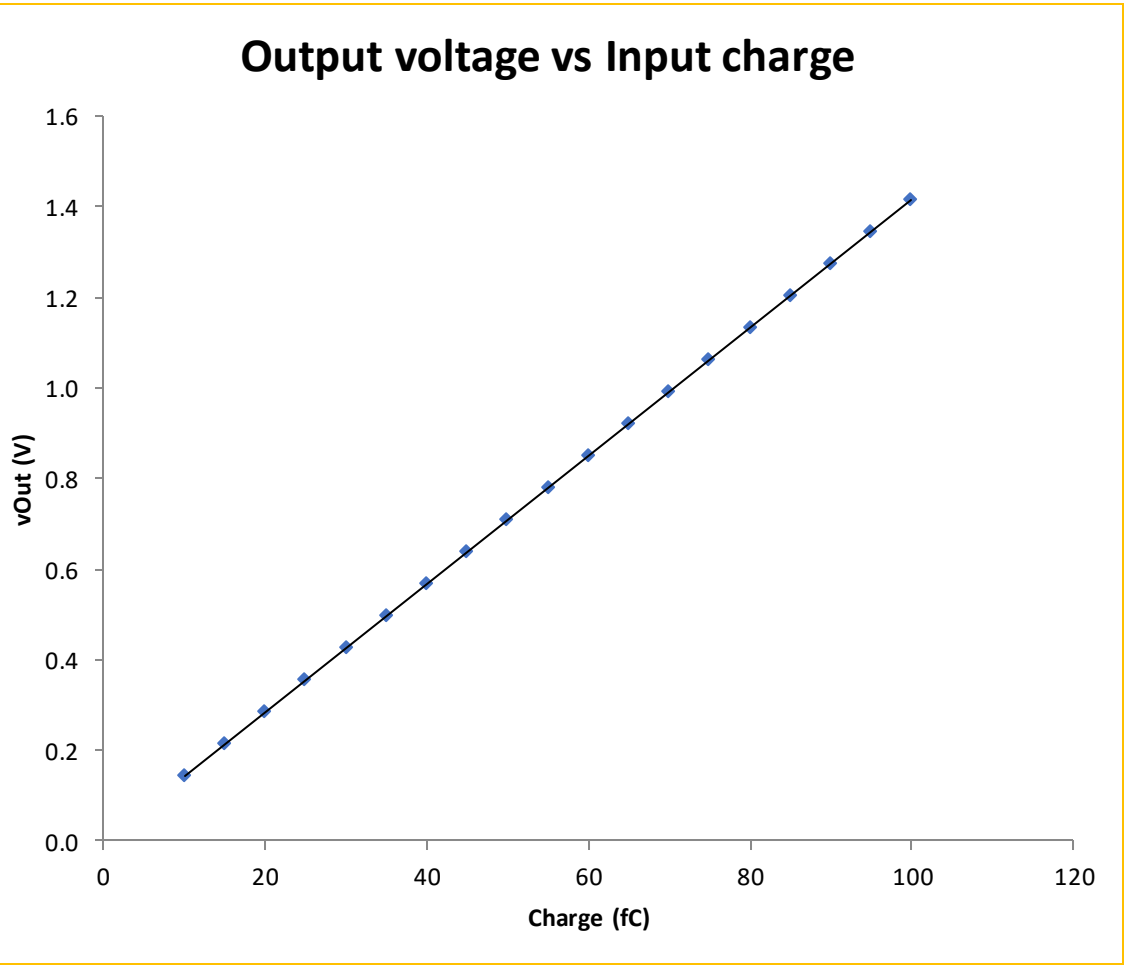
Setting: BL = 200/900 mV, Gain = 14 mV/fC, Cdet = 150 pF

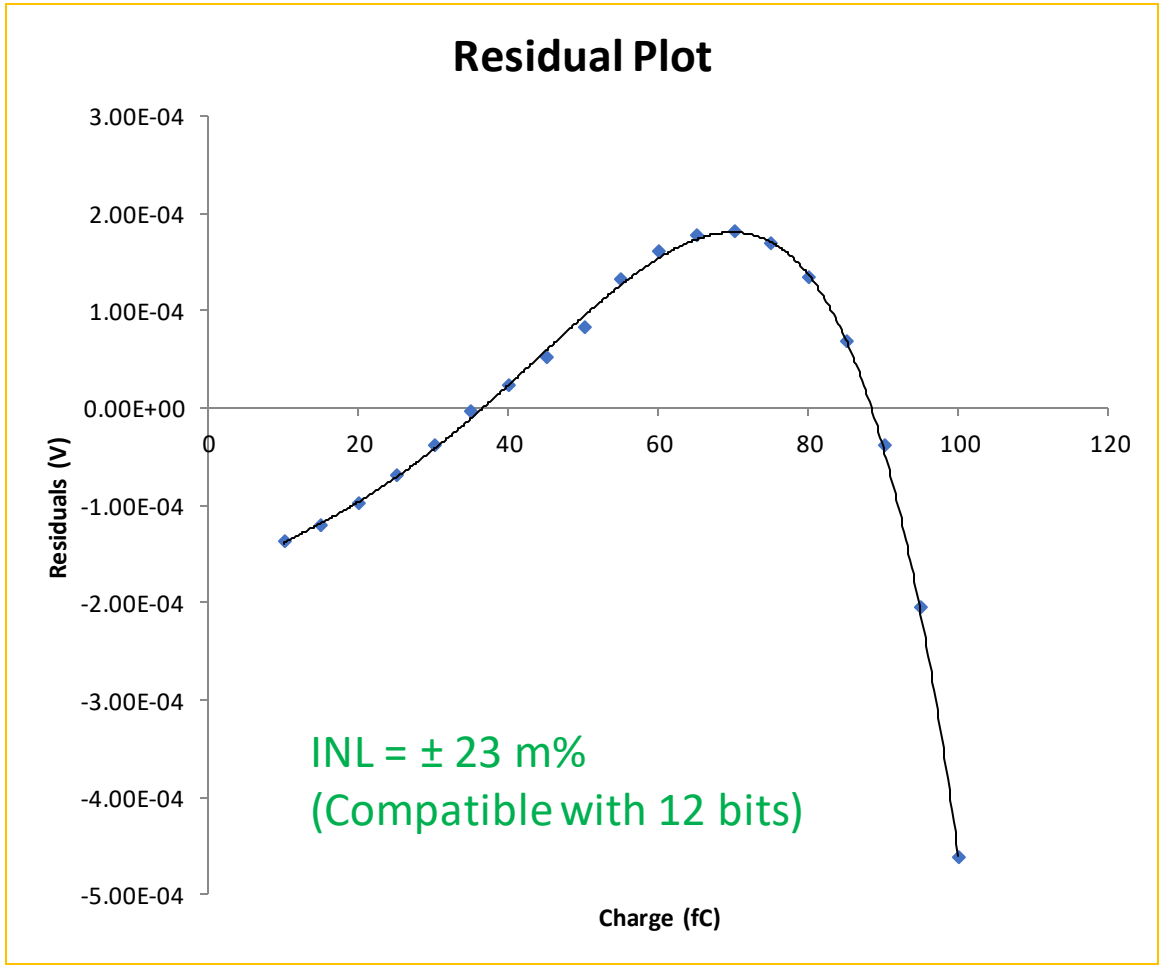


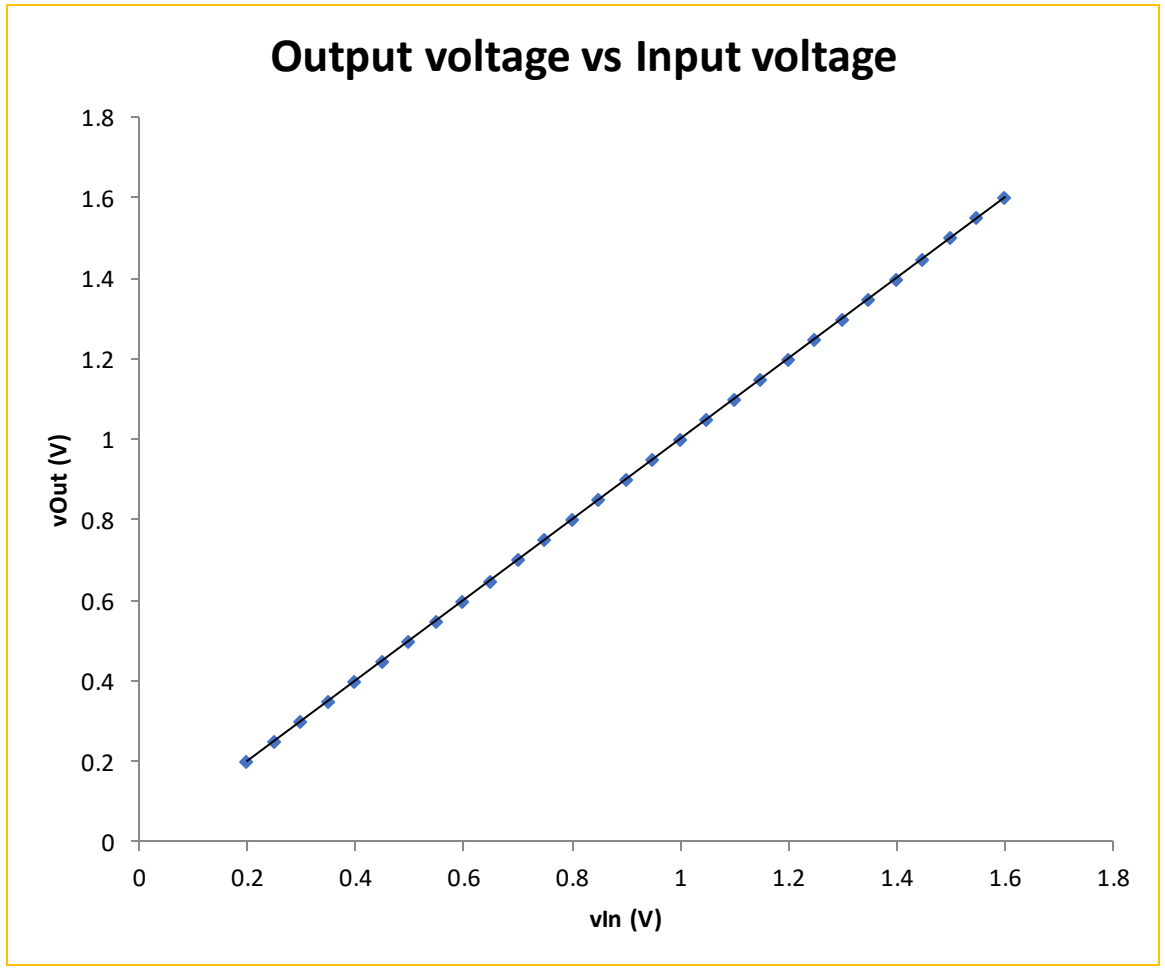
# P3 Simulation results – Linearity

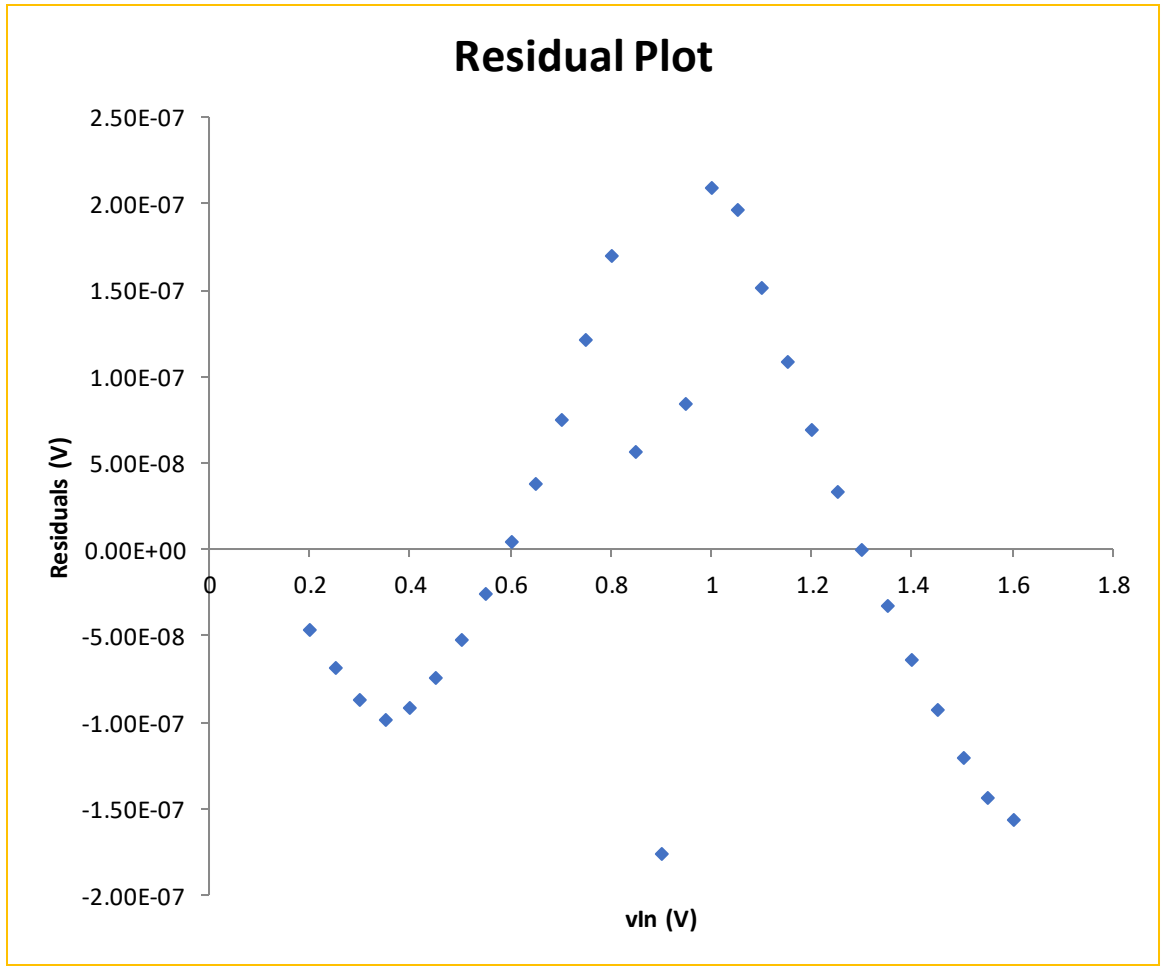
Setting: BL = 200 mV, Gain = 14 mV/fC, Tp = 2 us, 500pA, Cdet = 150 pF



# Single-ended output buffer linearity




INL = ± 14 µ% (Typical)

# LArASIC P4 Development

- Towards a robust design

# Required Improvements for New FE ASIC (P4)

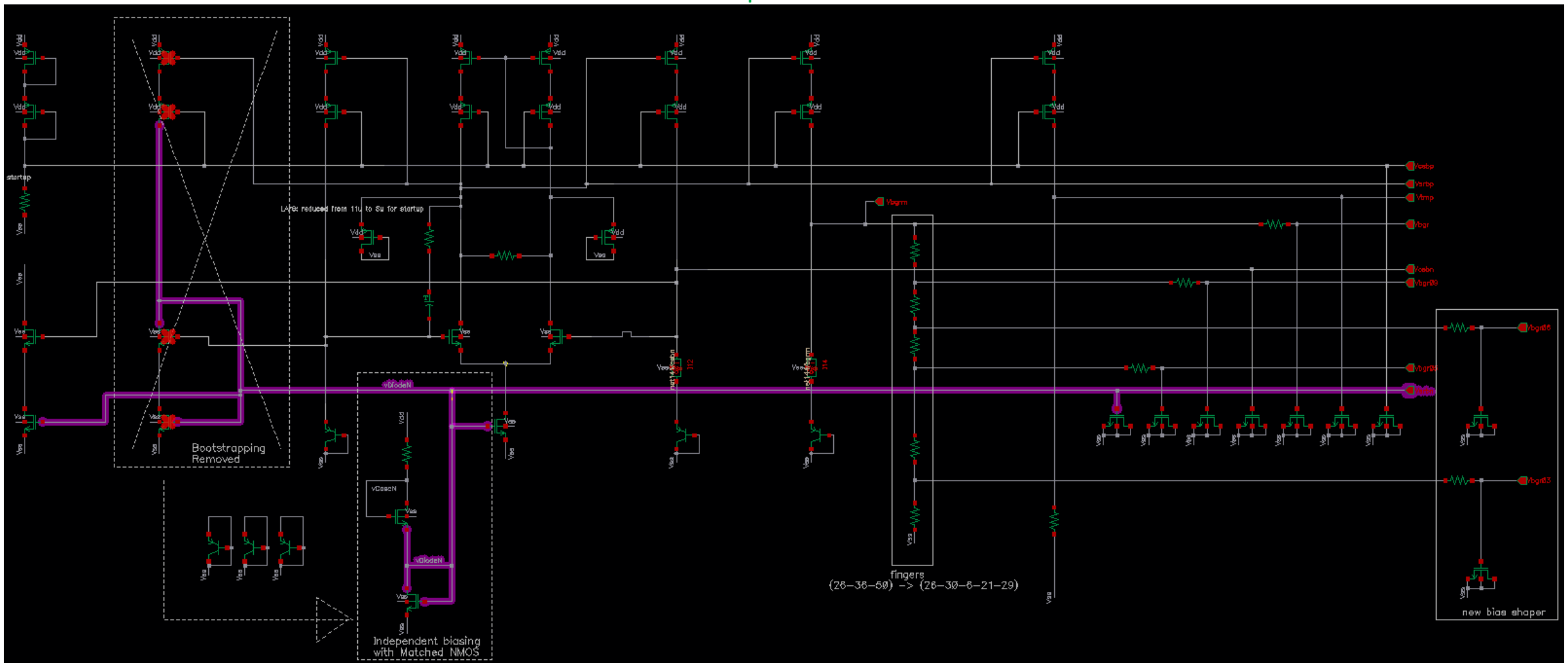
- Required
  - Address bandgap voltage reference failures happening in ~7% of the chips at cold
  - Ledge effect mitigation during shower events up to 500 fC input charge
  - Implement single ended to differential buffer matching with ADC spec.s
- Additional
  - Decreasing baseline shift for different settings

# BGR Problem Mitigation in P4

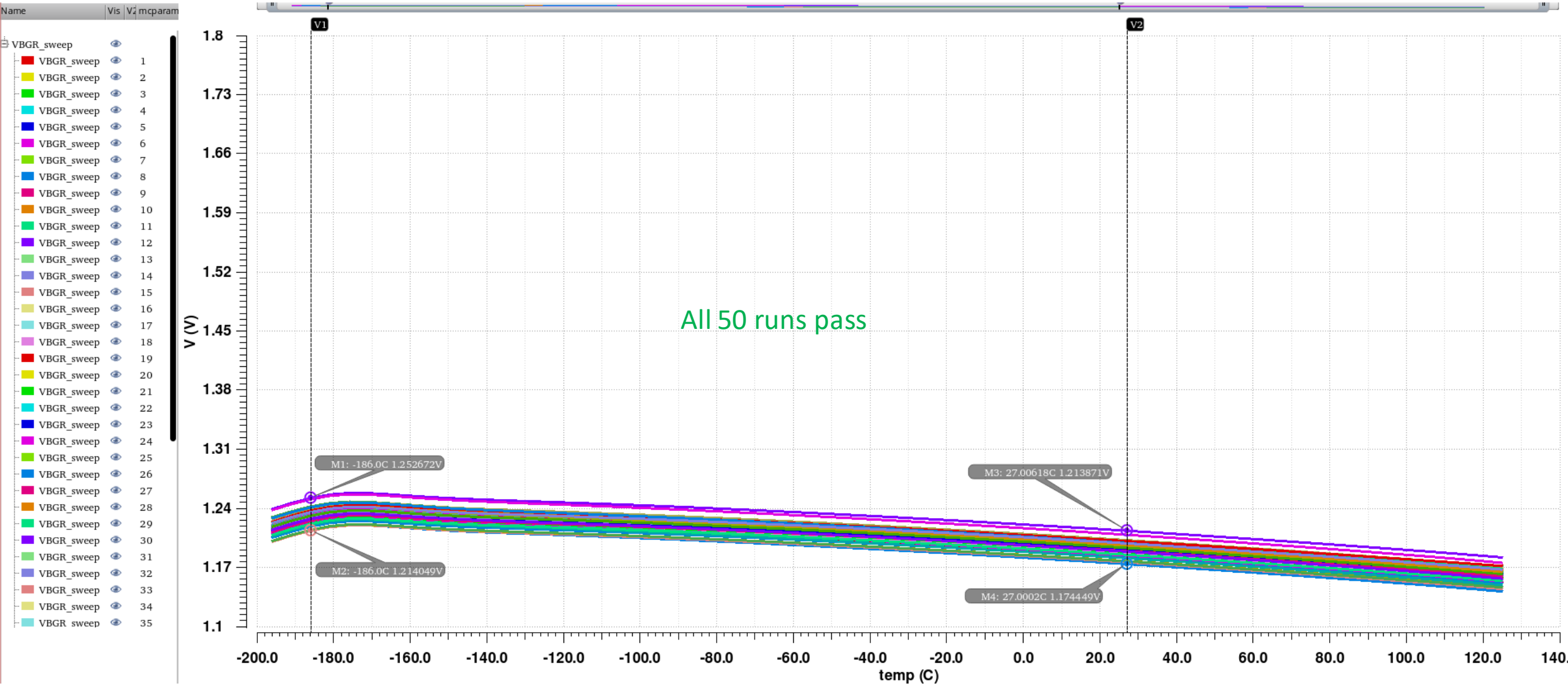
# Mitigation of Bandgap Reference problem with schematic modifications for P4

In all the previous versions of BGR, bias of BGR was derived from BGR → Problem

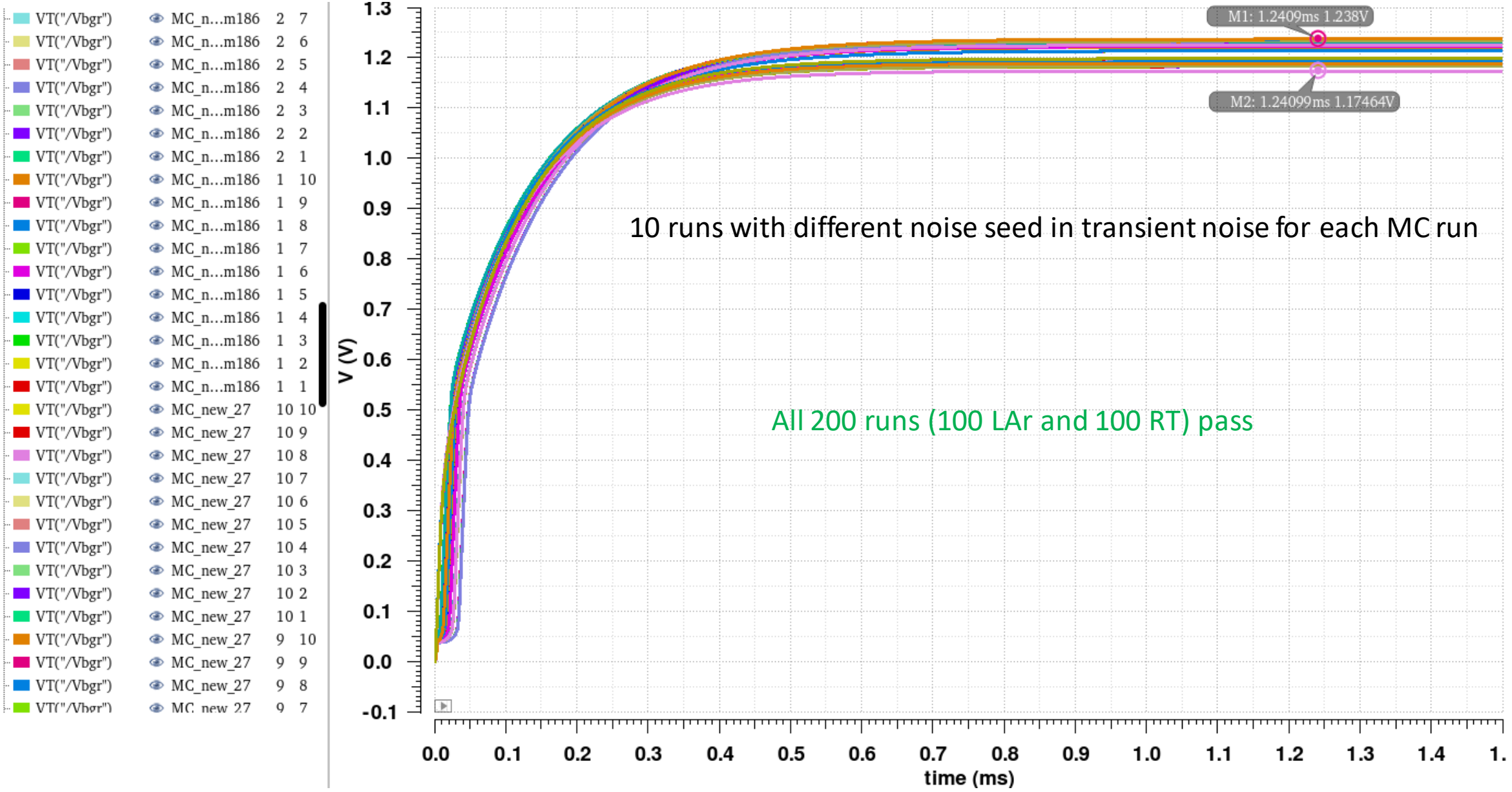
We decoupled it



# 50 run MC (PV+MM) sim.s with Temp. sweep -196 to 125°C of proposed BGR



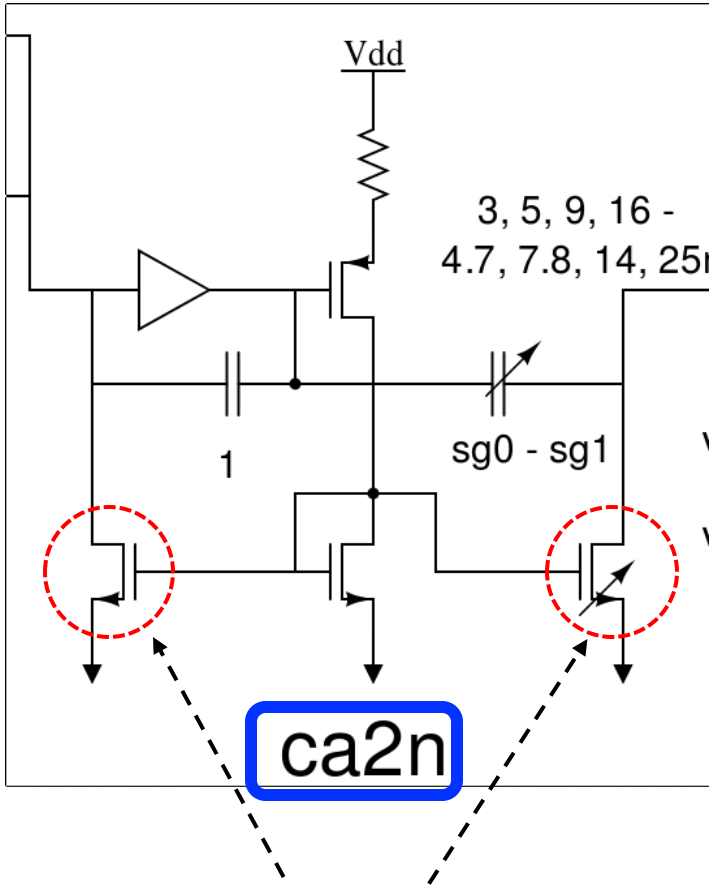
# Start-up sim.s of proposed BGR with 1µs supply ramping; 10 run MC (PV+MM) at LAr and RT



# Ledge Effect Mitigation in P4

# Proposed mitigation of Ledge Effect

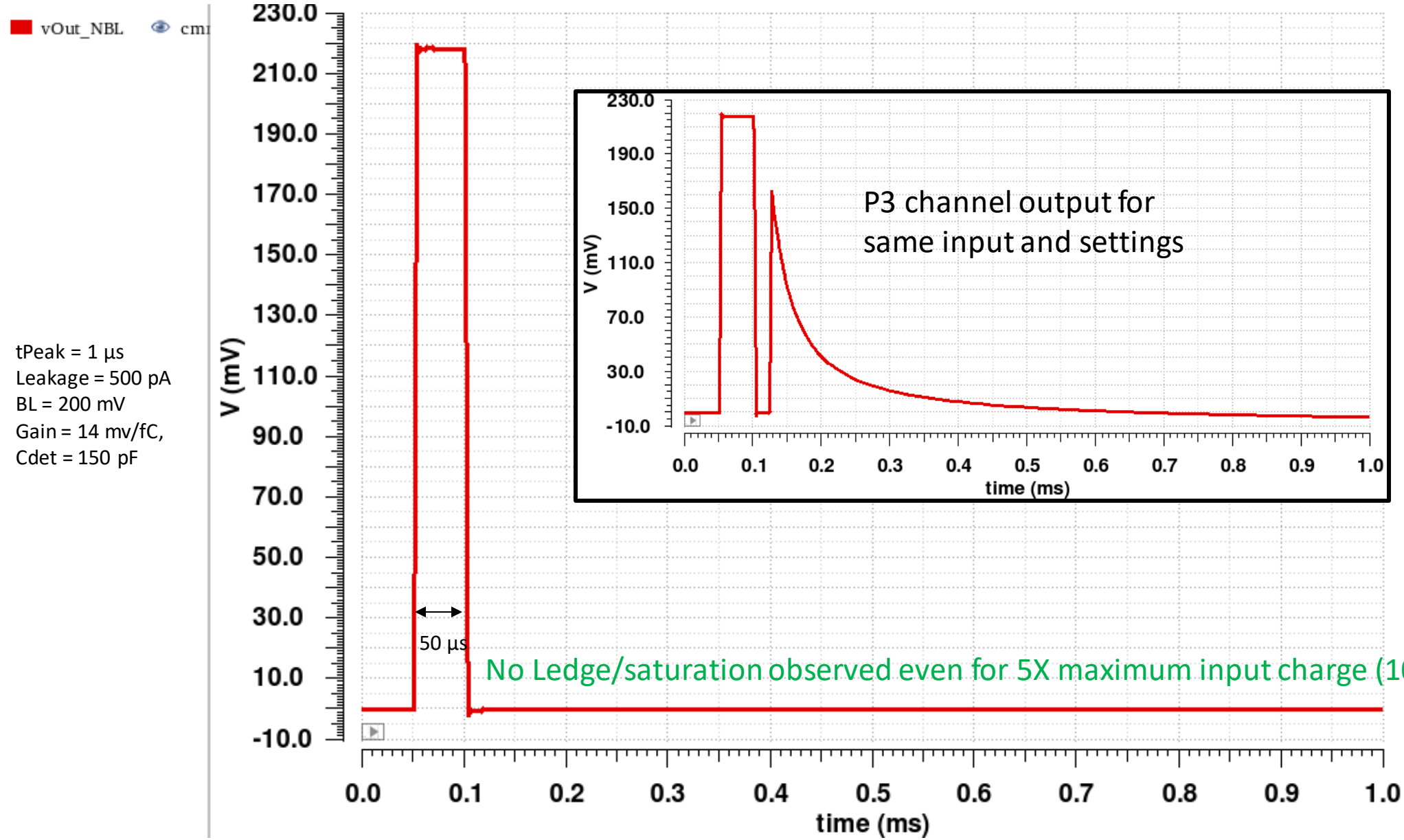
- After multiple simulations the optimal resizing factor was chosen to be 3x instead of 8x
  - Capacitance increases by factor 9, not 64
  - Mitigates ledge effect
  - Pole-zero cancellation similar to P3




Both W and L increased by 3 times instead of 8

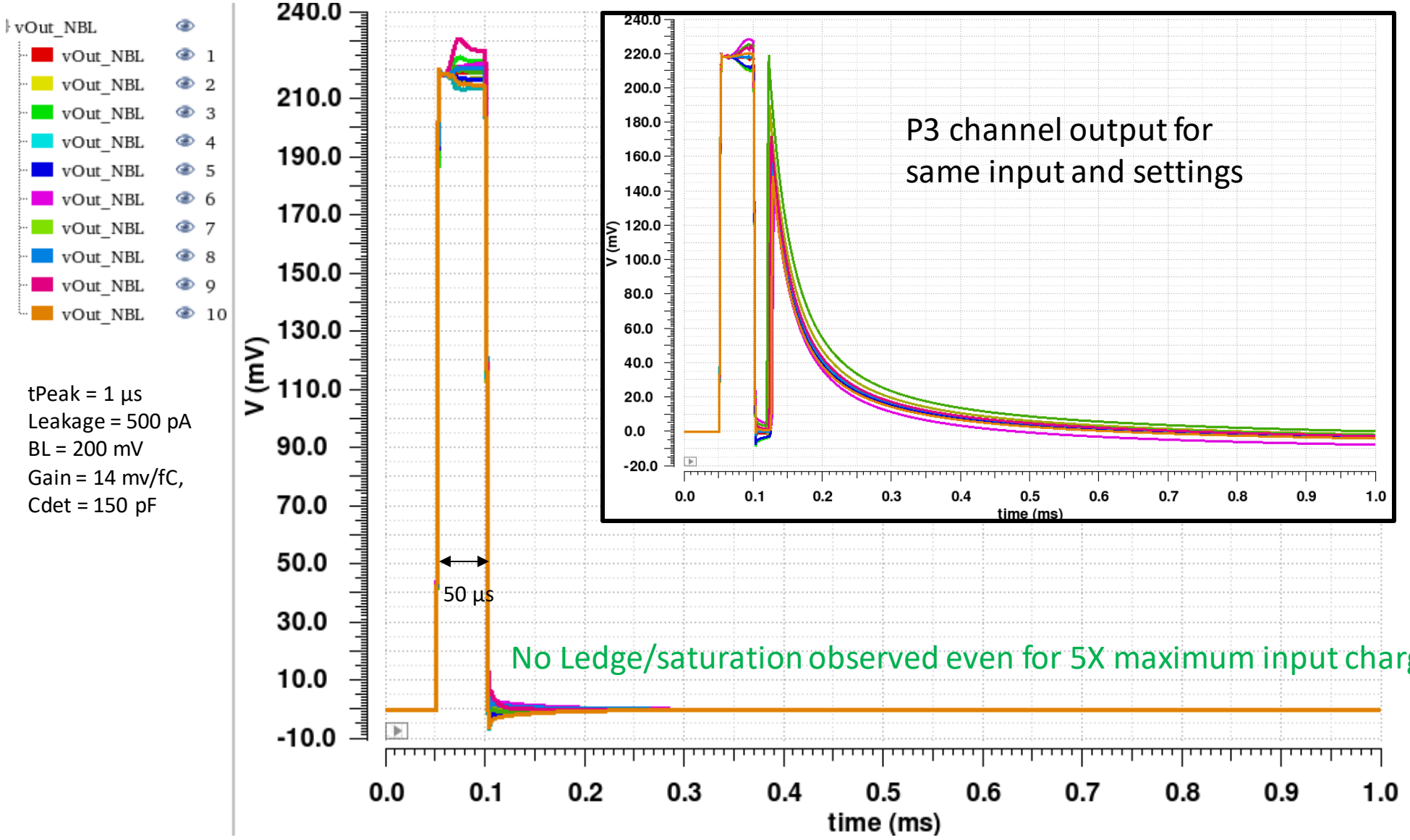
# Simulations of shower event at LN for P4 : 500 fC input for 50 µs

tPeak = 1 µs
Leakage = 500 pA
BL = 200 mV
Gain = 14 mv/fC,
Cdet = 150 pF



# Monte-Carlo simulation of shower event at LN for P4 : 500 fC input for 50 µs

10 run with process and mismatch at schematic level

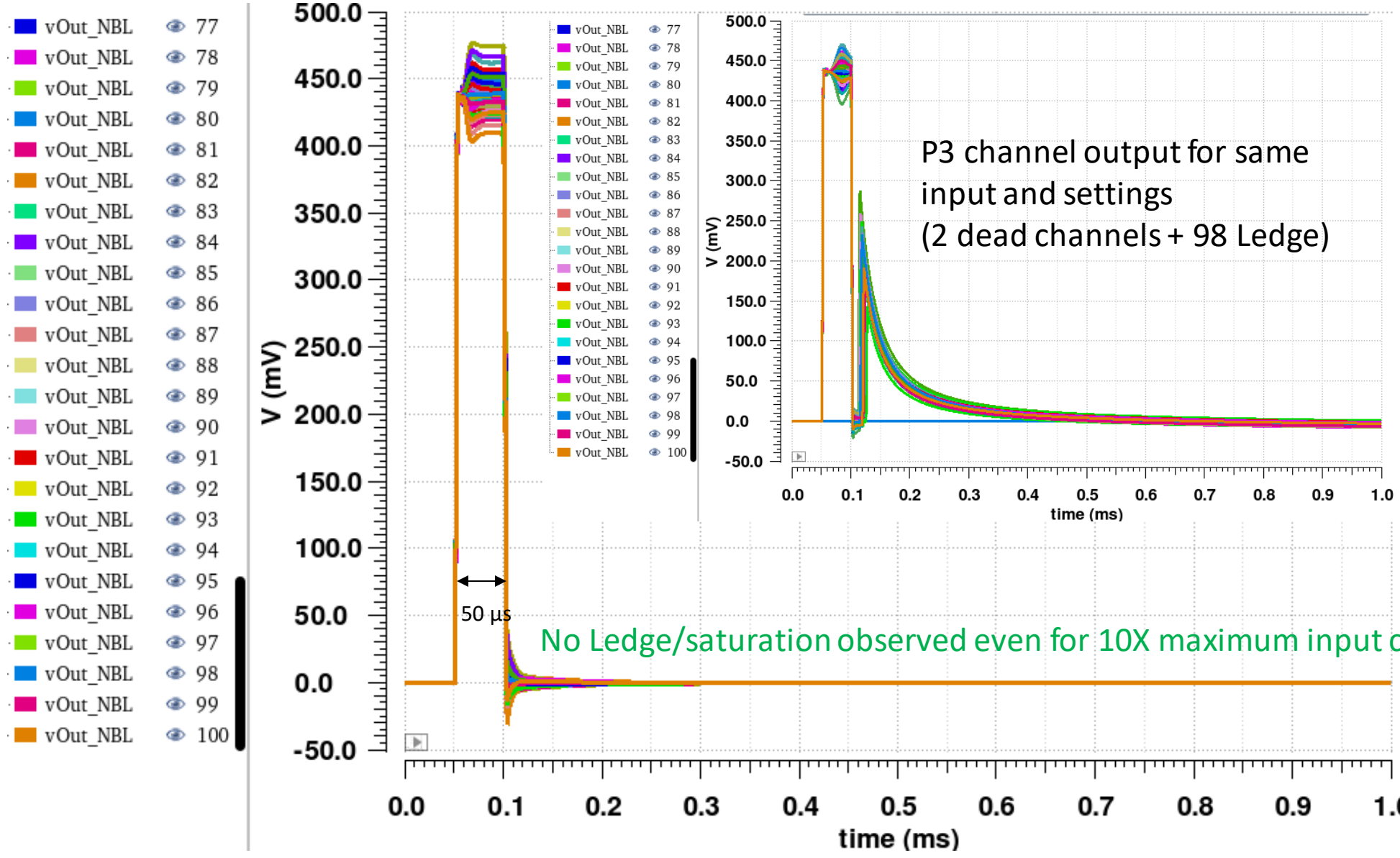



tPeak = 1 µs
Leakage = 500 pA
BL = 200 mV
Gain = 14 mv/fC,
Cdet = 150 pF

No Ledge/saturation observed even for 5X maximum input charge (100 fC)

# Monte-Carlo simulation of shower event at LN for P4 : 1 pC input for 50 µs

100 run with process and mismatch at schematic level

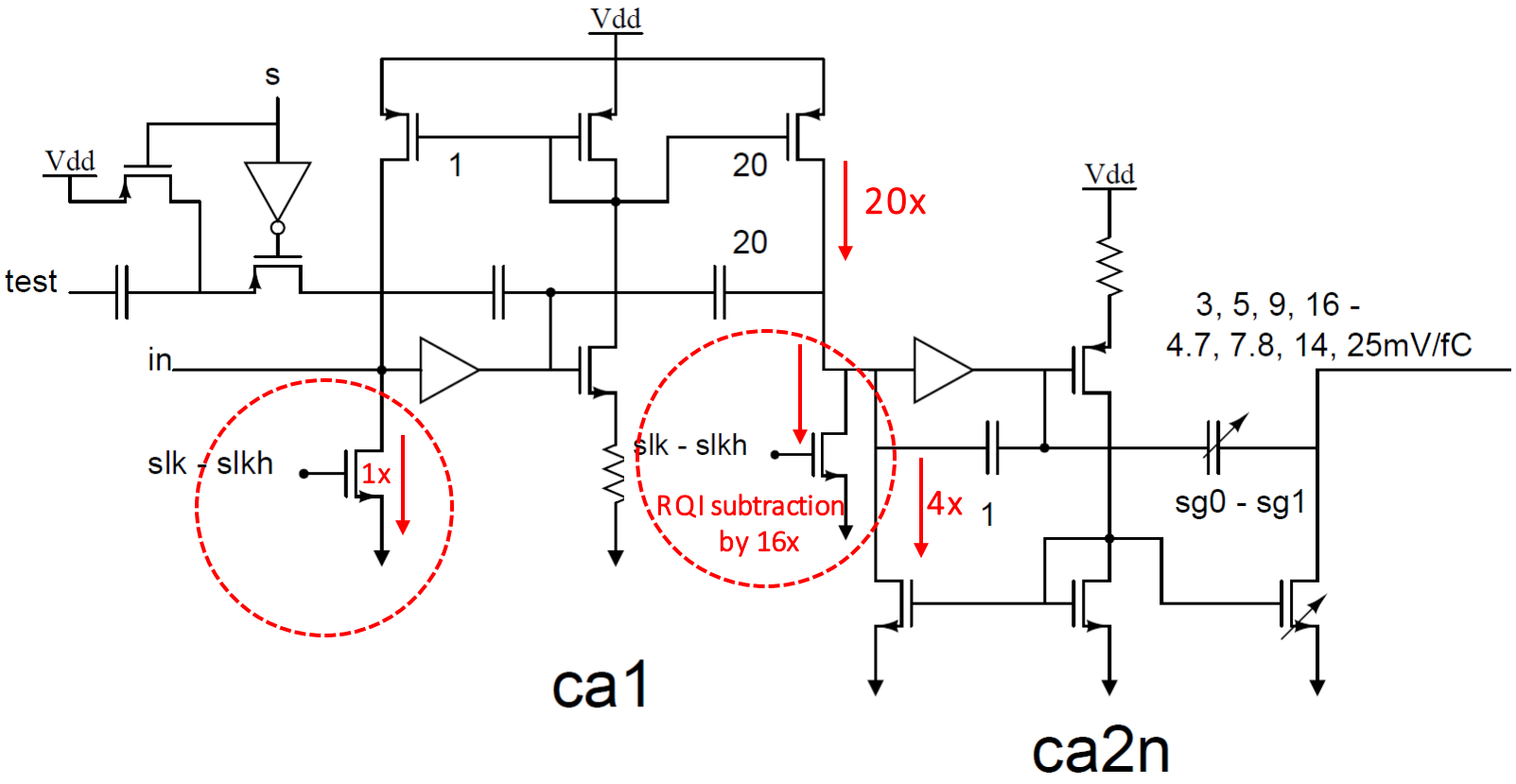



No Ledge/saturation observed even for 10X maximum input charge (100 fC)

tPeak = 1 µs
Leakage = 500 pA
BL = 200 mV
Gain = 14 mv/fC,
Cdet = 150 pF

# Baseline DC Shift Improvement in P4

# Proposed mitigation of baseline shift for different settings

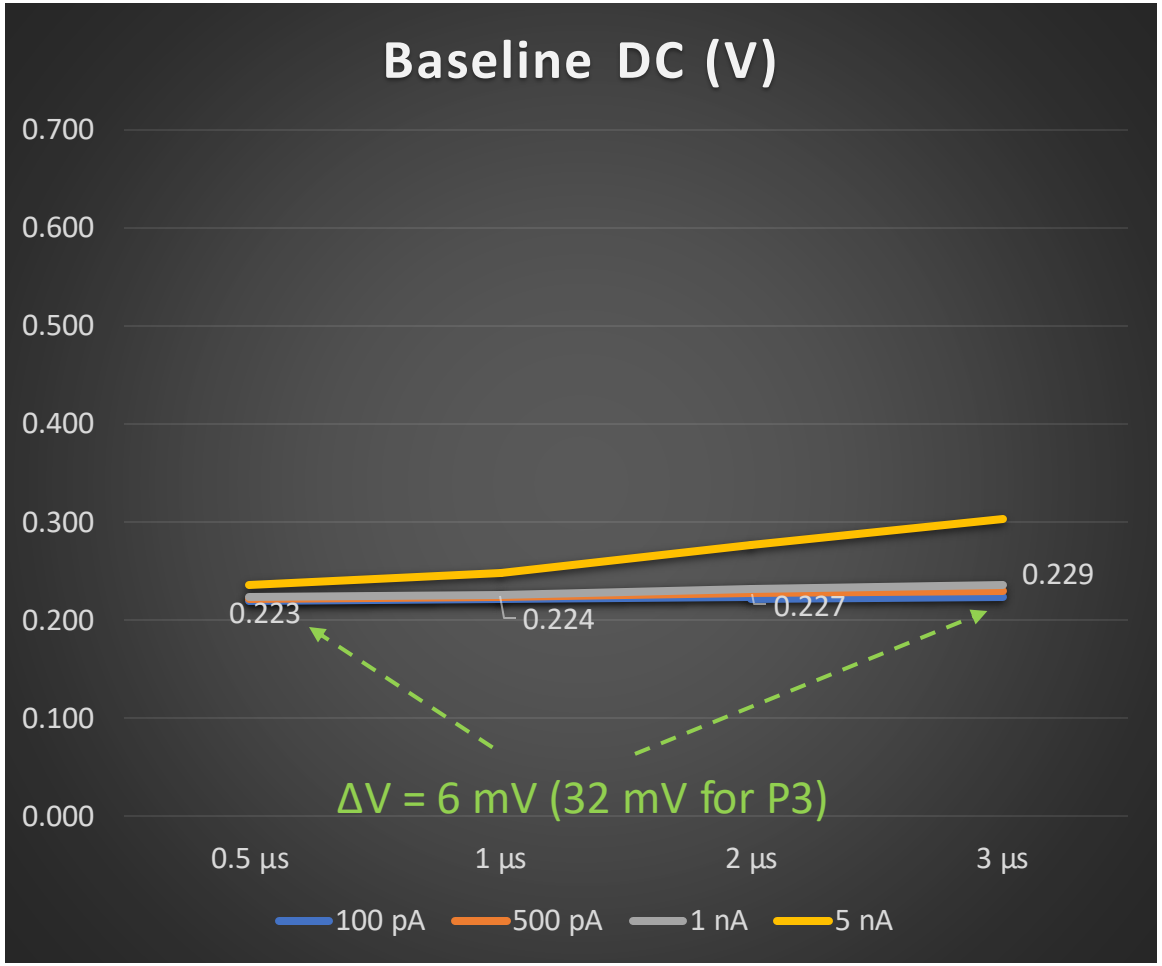


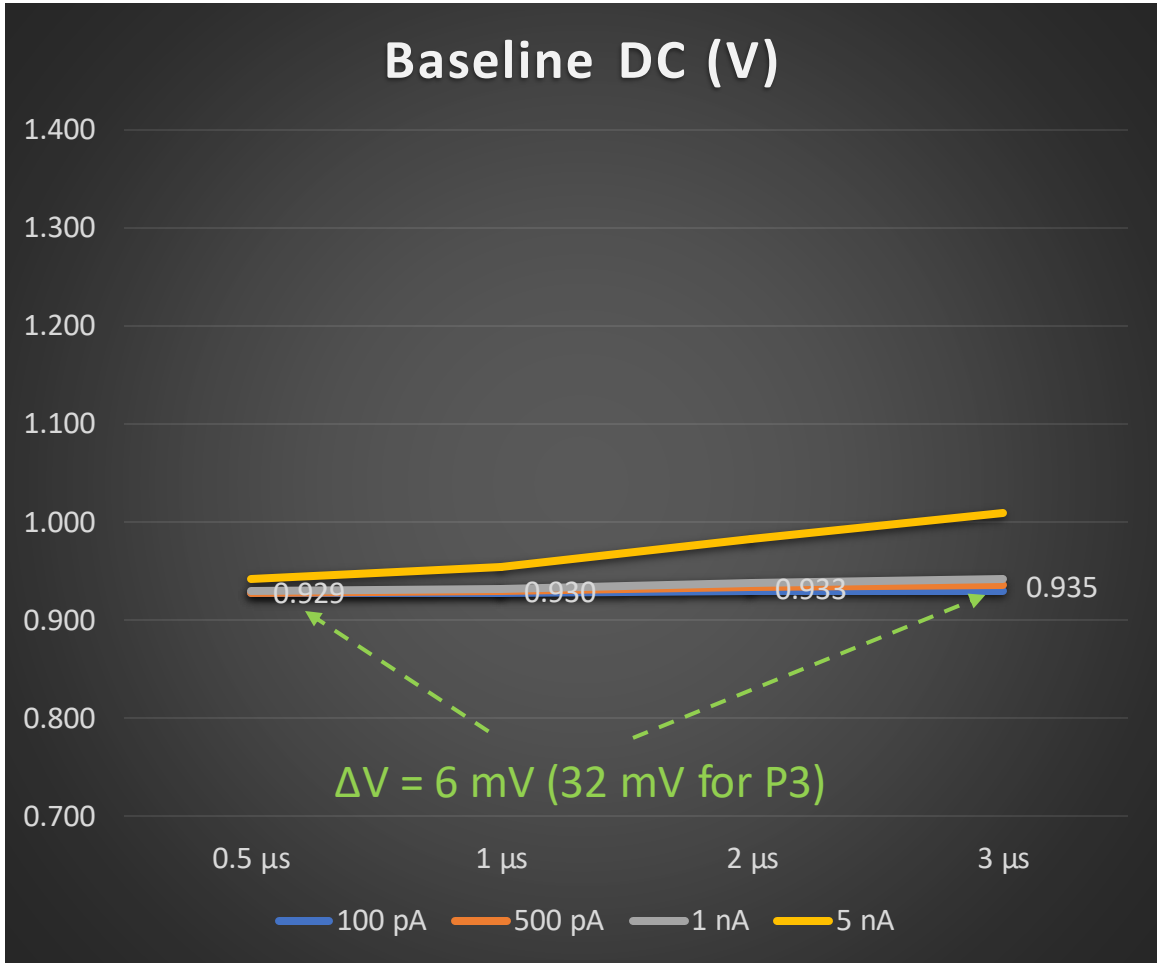

- RQI subtraction improves baseline shift
  - A factor of 16x RQI is optimal

- Previously in P1, all the RQI was completely subtracted (20x) in P1, which incapacitates adaptive continuous reset loop (leakage). Hence necessitating 1 GΩ resistor at input to make the loop work.

# Baseline shift for different settings with Proposed modifications

Setting: BL = 200/900 mV, Gain = 14 mV/fC, Cdet = 150 pF



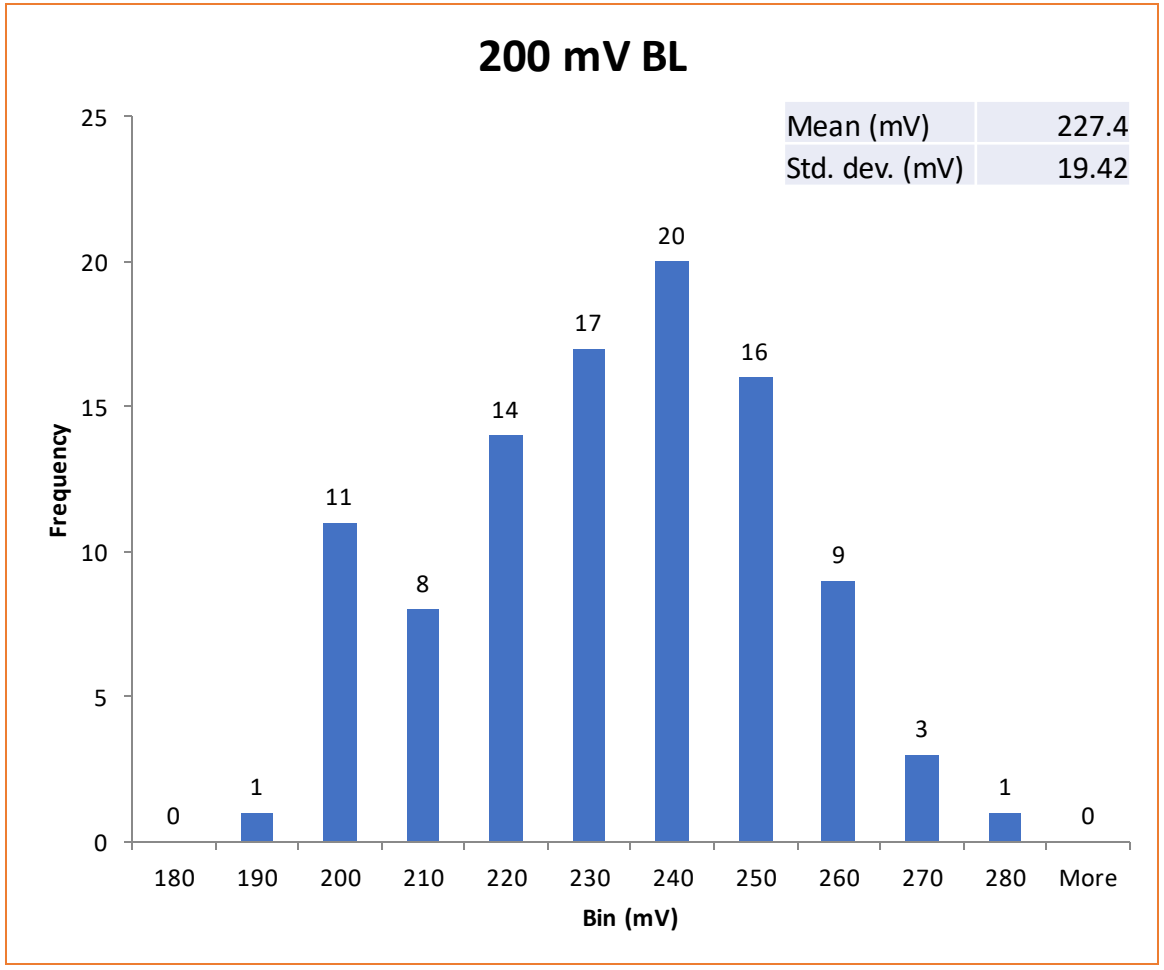



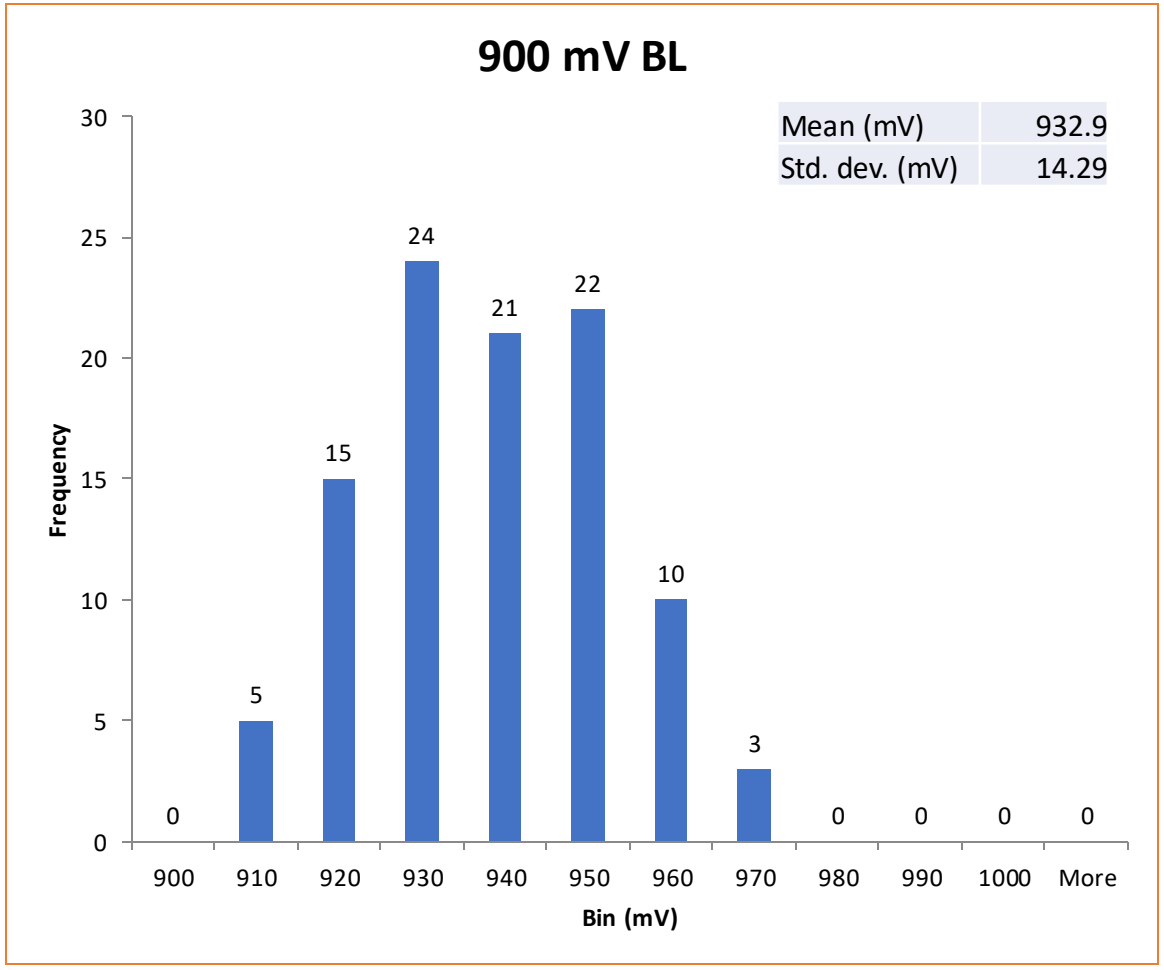

Baseline shift improved → Maximizes signal swings

# Other Performance Metrics of P4

# Proposed P4 FE ASIC Baseline DC Variation in LN – MC simulations

100 run MC simulations (PV+MM) at schematic level
Setting: BL = 200/900 mV, Gain = 14 mV/fC, Tp = 2 us, DC, Buffer not used, 500pA

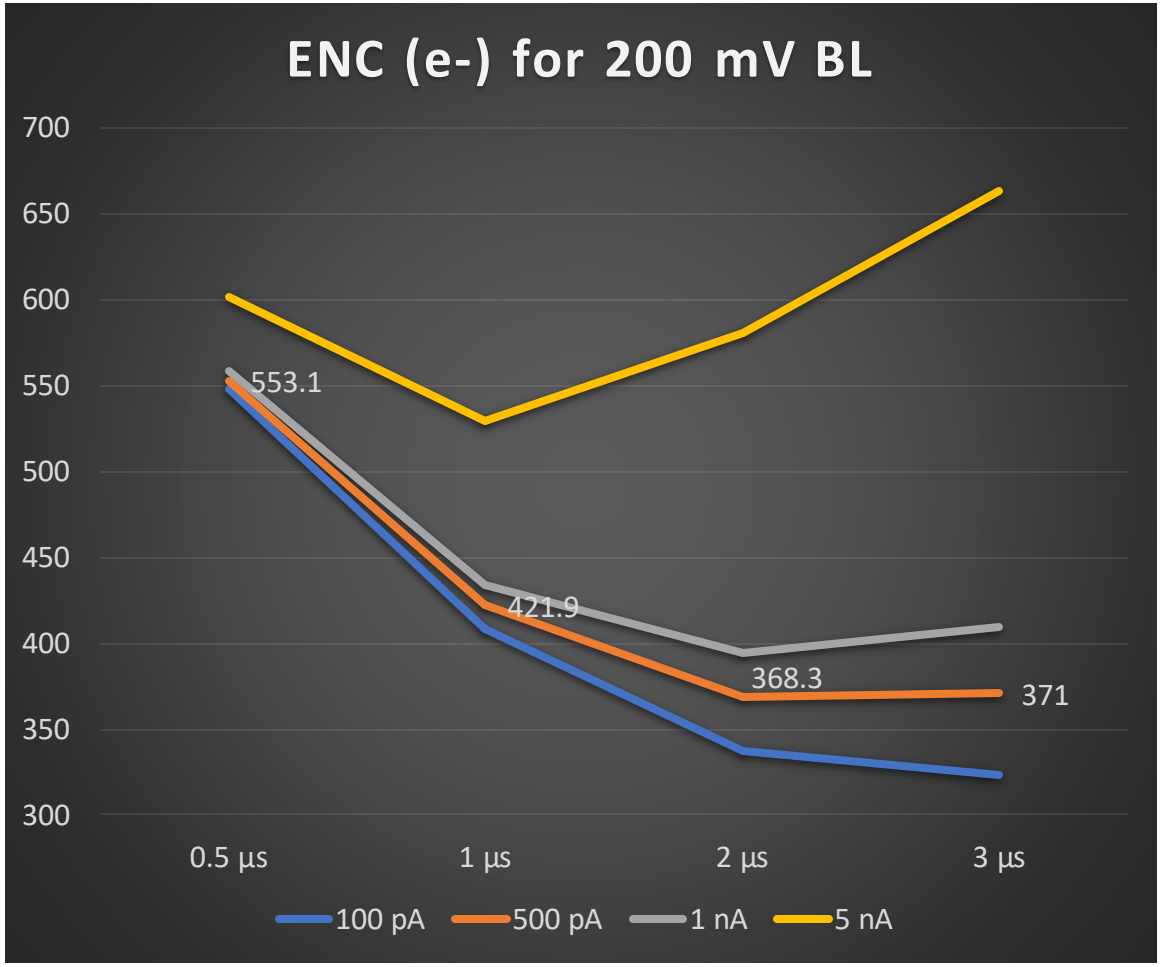


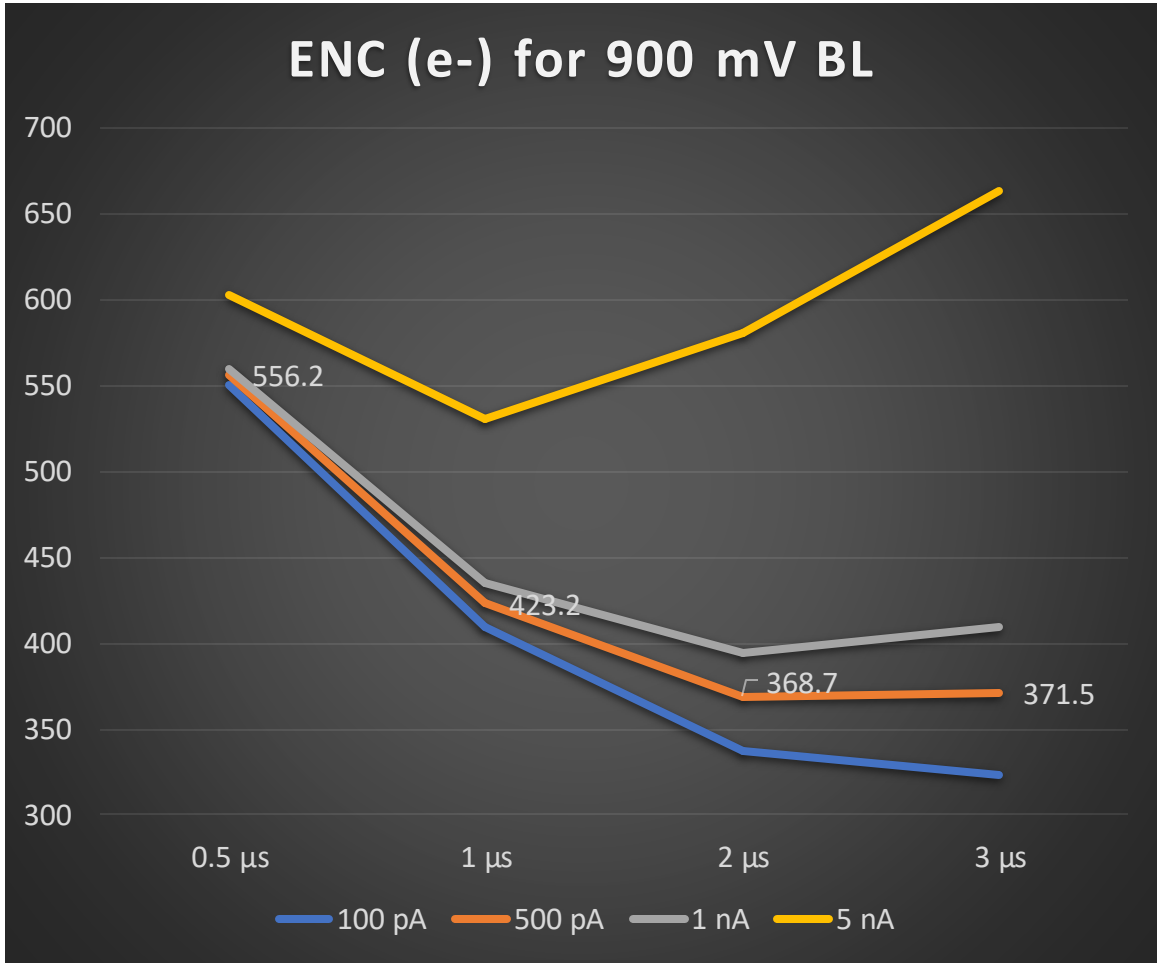




Slightly better than P3

# Simulated ENC of the proposed P4 channel

Setting: BL = 200/900 mV, Gain = 14 mV/fC, Cdet = 150 pF

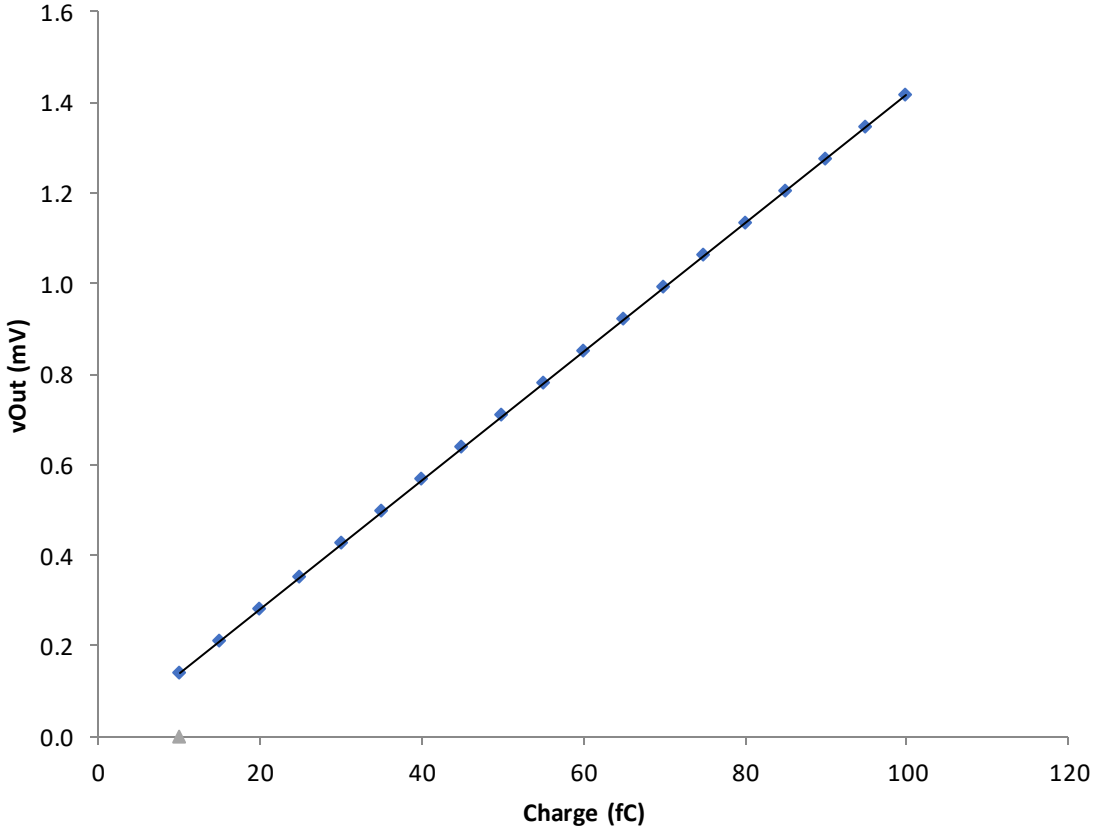


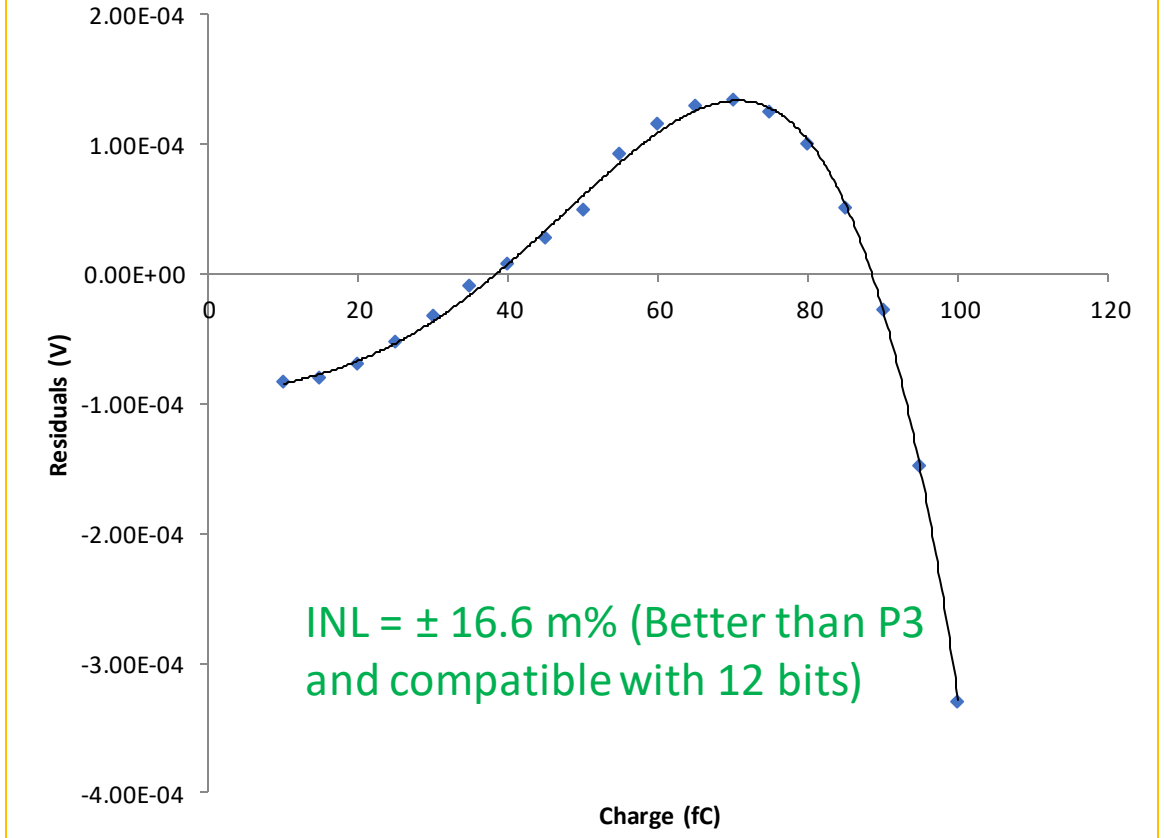




ENC almost similar to P3

# Proposed P4 simulation results – Linearity

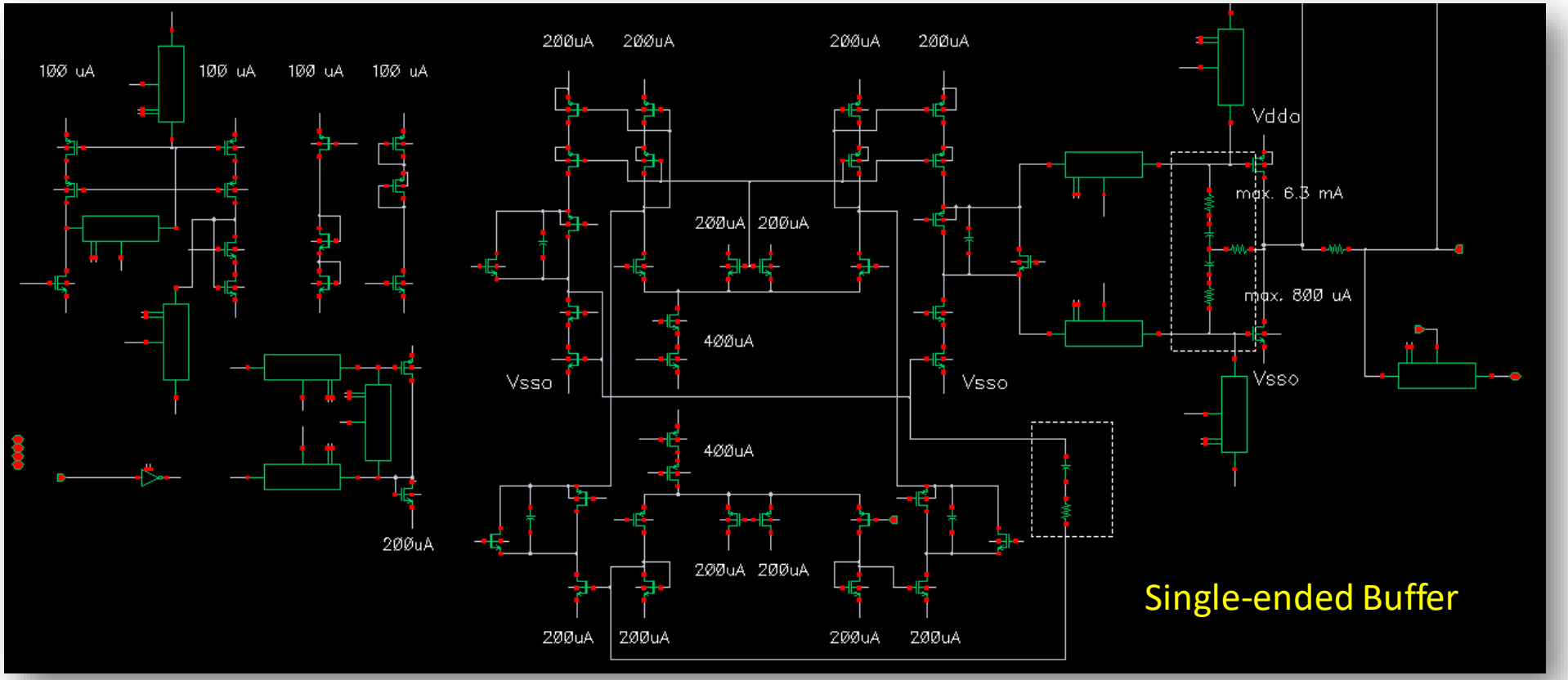
Setting: BL = 200 mV, Gain = 14 mV/fC, Tp = 2 us, 500pA, Cdet = 150 pF



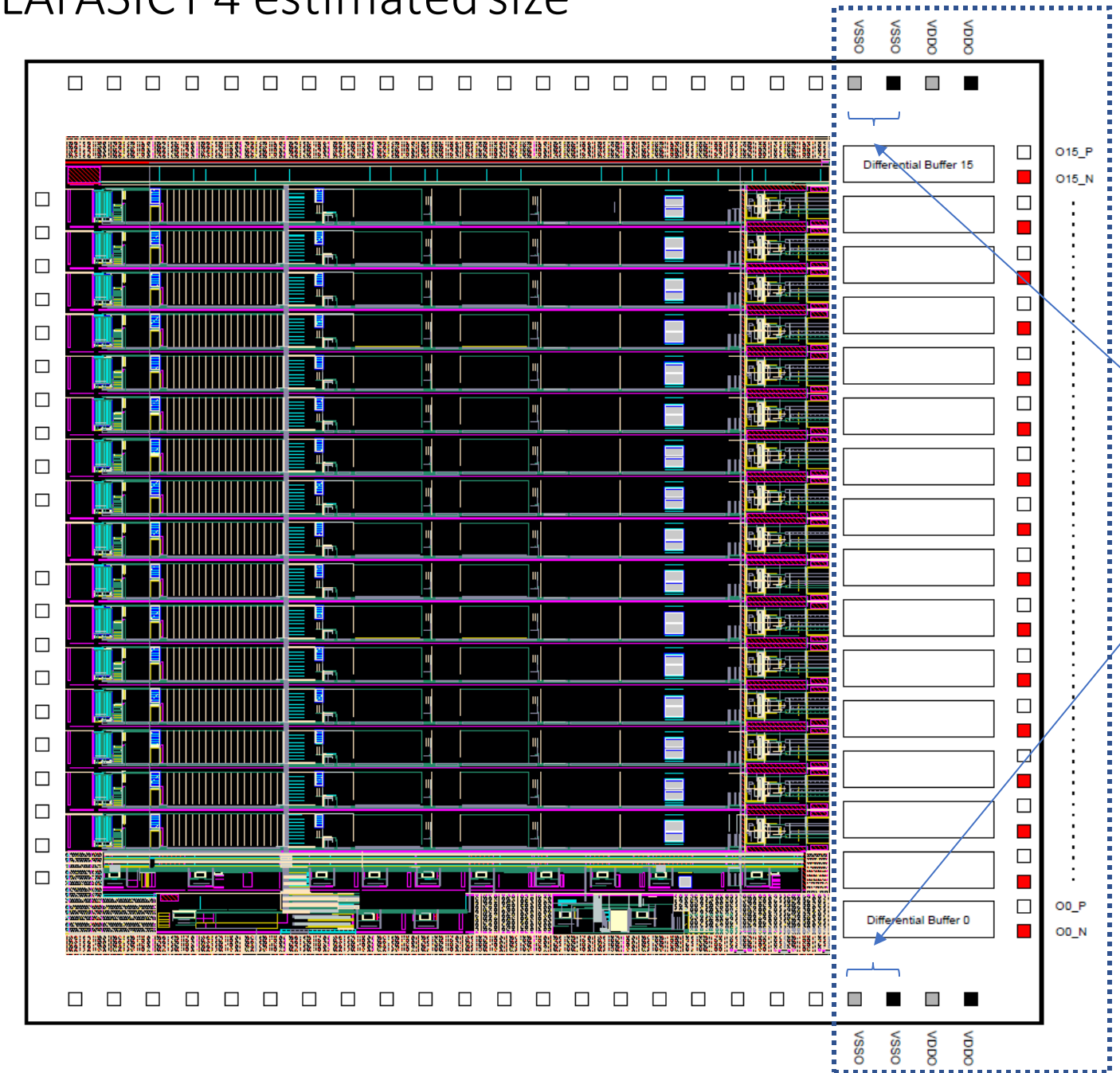
# Single-ended to Differential Converter (SDC) buffer

- Two options
  1. Porting the SDC design present in cold ADC (65 nm) → Vdd = 2.25 V
  2. Based on single-ended buffer core
     - Already present in 180 nm, highly linear and silicon-proven rail-to-rail operation
     - Need to modify for differential output and qualify with simulations
     - Addition of Common-Mode Feedback Circuit (CMFB)



# LArASIC P4 estimated size

- Differential buffers will reuse single-ended buffer output and supply pads
- Need 16 more output, 2 Vddo and 2 Vsso pads.
  - Pad count 100 (from 80)
- Estimated layout size = 7 mm x 6.2 mm (from 6.0 mm x 5.7 mm)



# Summary and Future Work

- Discussed existing P3 LArASIC
- Simulations performed with foundry models
  - Unfortunately cold models don't exist
- Proposed P4 LArASIC with schematic modifications to mitigate
  - BGR problem – Done
  - Baseline DC shift variability – Done
  - Ledge effect – Done
- To start work on layout and post-layout verifications – By end of March
- Differential buffer – By end of April
- All layout Modifications, extracted simulations and tapeout – End of June

# Backup Slides

# P3 Simulation results – Linearity testing in time domain

Setting: BL = 200 mV, Gain = 14 mV/fC, Tp = 2 us, 500pA, Cdet = 150 pF