Measurements on P2 and P3 FE ASIC and Experience of P2 FE ASIC in ProtoDUNE-SP

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Outline

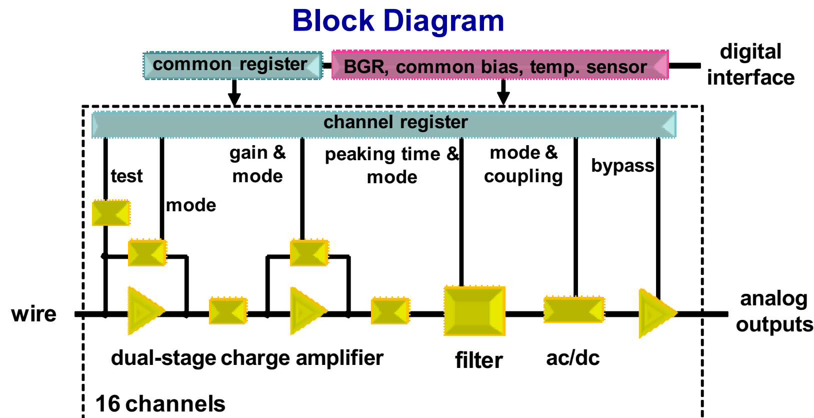
- A Brief History of FE ASIC
- Evolution of FE ASIC Test Board at BNL
- FE ASIC Basic Functionality & Performance
- Observations from Measurement
    - Pole-zero Cancellation
    - Baseline Distortion
    - Ledge Effect
    - Start-up Failure
- P2 Instrumented in ProtoDUNE-SP
    - QC and Yield
    - Performance and Stability
- Summary

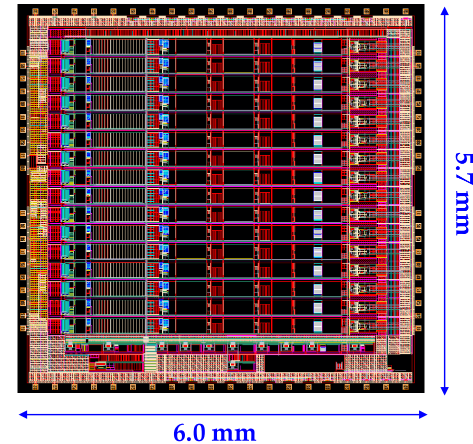
A Brief History of Cold FE ASIC Development

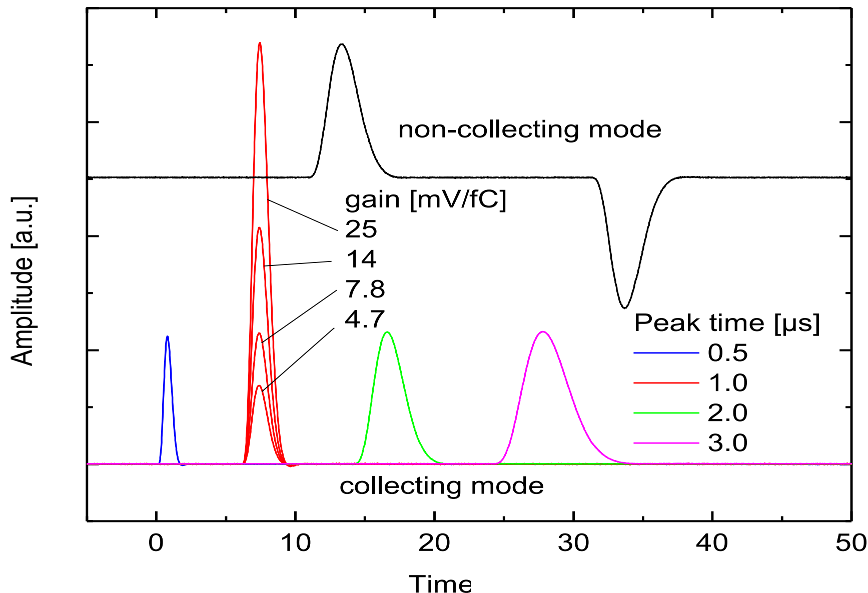
Version	Submission	Results
V1	02/2010	Functionality in LN2 achieved
V2	12/2010	Optimization of input MOSFET and resistance of input line
V3	07/2011	AC coupling and improvement of DC PSR
V4	03/2012	Improvement of uniformity of calibration response in LN2
V4*	06/2012	Improvement of cold yield, instrumented ***MicroBooNE (8,256 channels)***
P1	02/2016	Internal pulse generator, bias current options, BGR start-up
P2	08/2016	Pole-zero cancellation, external resistor and analog monitoring, instrumented ***ProtoDUNE-SP (15, 360 channels)***
P3	03/2018	Non-uniform baseline, default gain configuration
P4	N/A	Being developed

LArASIC -- Analog Front-End ASIC

16x ch programmable charge amplifier working at 77-300K for neutrino experiments

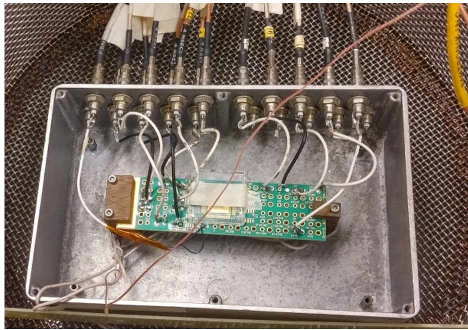


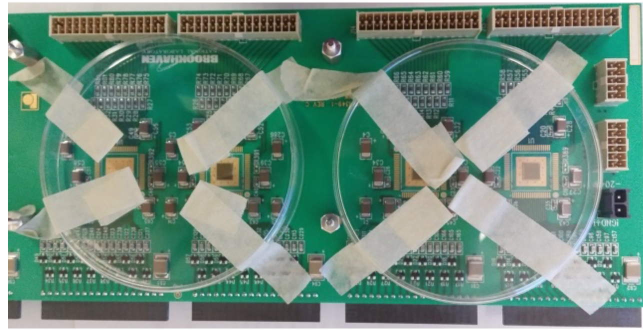


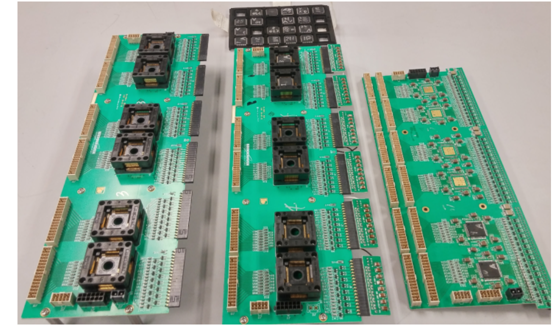


- P1/P2 Version (new features)
  - Built-in 6-bit DAC for calibration
  - Built-in analog monitoring output (P2)
  - Higher bias current options (1nA / 5 nA)
  - Smart reset
  - Increase ESD protection on I/O
  - Mitigate pole-zero cancellation (P2)
  - Increase the buffer-off drive capability
- P3 Version (new features)
  - Address the baseline distortion
  - Remap the register for gain setting (set 14 mV/fC as default)

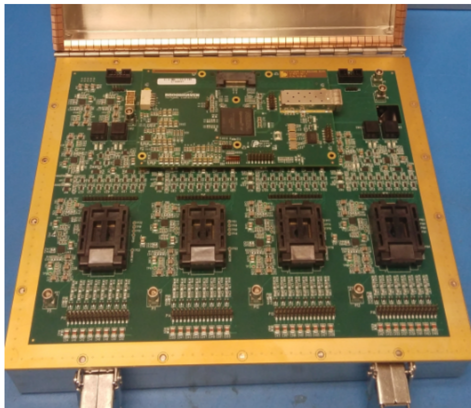
Evolution of FE ASIC Test Boards at BNL

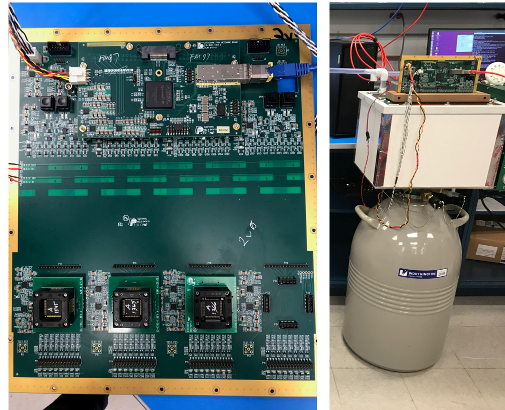

FE ASIC die


MB cryo test board with dies


MB cryo socket test board

Above: FE ASIC quick-checkout and characterization
Below: FE ASIC characterization and QC

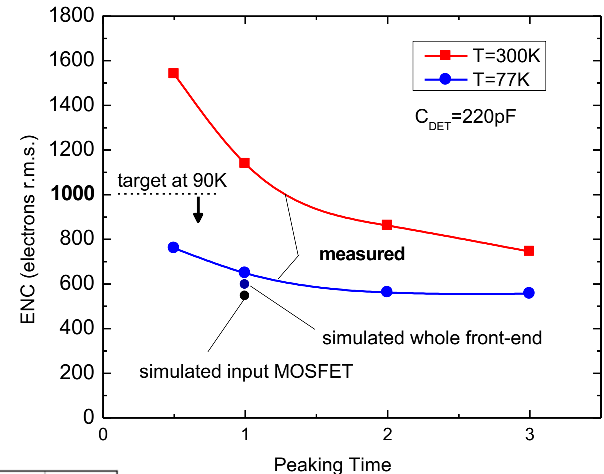

Quad ASIC test board for RT

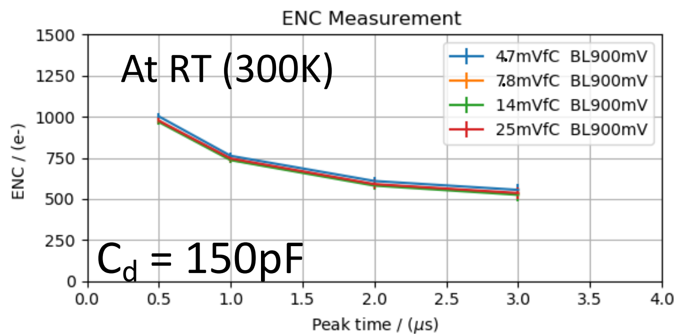

Quad ASIC test board for cryo

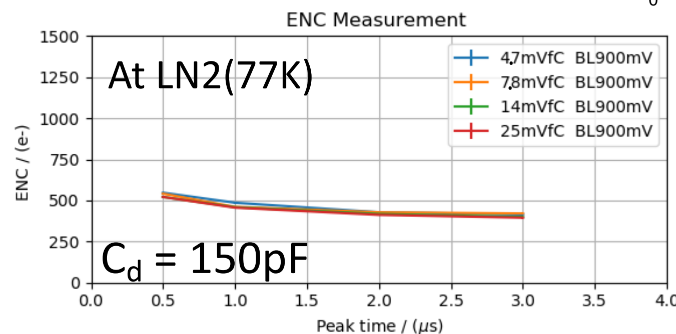
Toy TPC (150pF/120pF)
(emulate detector capacitance)

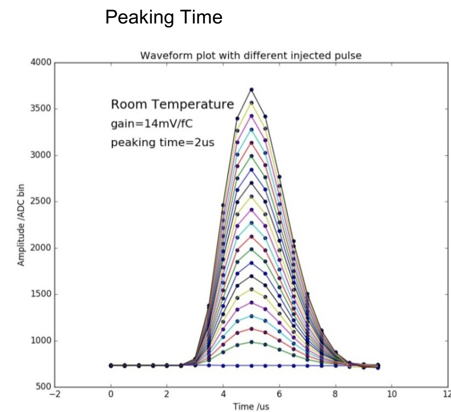
FE ASIC Basic Functionality & Performance

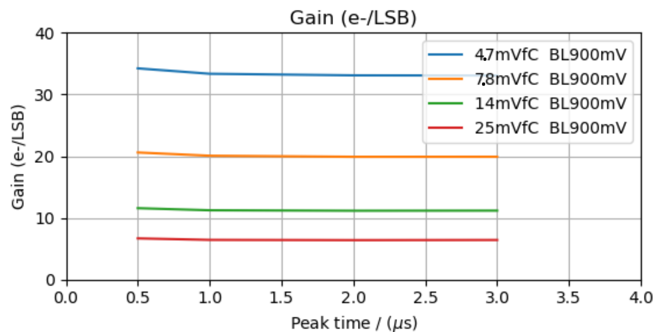
- Noise (ENC) in FE ASIC *vs* temperature and peaking time of the anti-aliasing filter
  - White series noise which is dominant at short peaking times decreases the most with temperature.
  - The remaining noise is dominated by 1/f noise, which is independent of the peaking time.
- Uniform gain among channels (or chips)

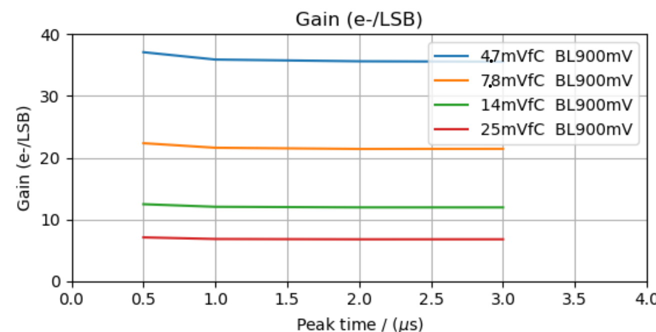










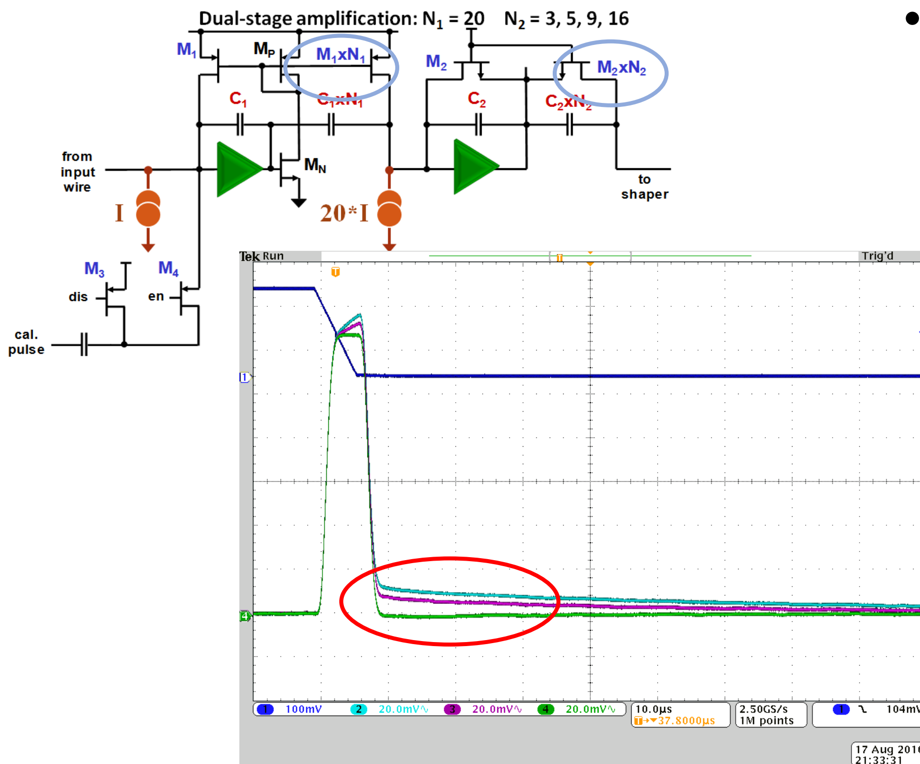


FE Configuration:
Baseline: 900mV
FE buffer: OFF
FE DC coupling
Leakage Current: 500pA
Calibration with FE internal DAC
No protection diodes for inputs

Note: Plots are made from data collected by 16-bit ColdADC with P2 FE ASIC

Address the Imperfect Pole-zero Cancellation (1)

- MSU has reported the excess baseline excursion of MicroBooNE FE ASIC
  - It is due to excess mismatch between M-C and MN-CN time constants in first or second stage
- Was observed both on MB (V4*) and P1 FE ASIC at cryogenic temperature
  - The imperfect pole zero cancellation is not related to the stress of the packaging

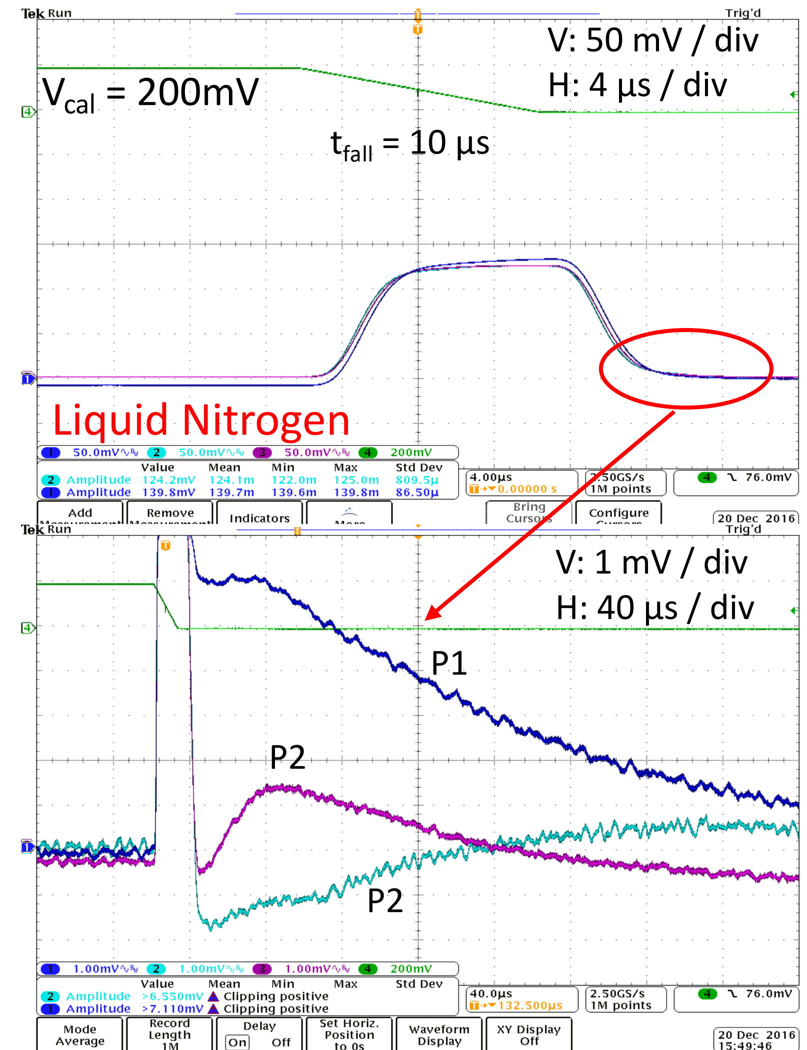


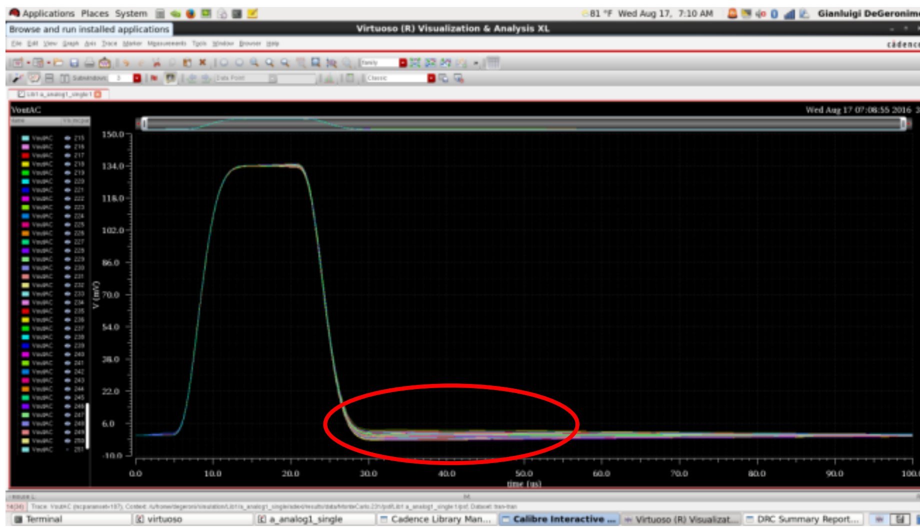
- Simulation confirmed the imperfect pole-zero cancellation

Simulation plot

Address the Imperfect Pole-zero Cancellation (2)

- P2 FE baseline recovery dispersion is < 1.5% of peak height
  - **P1: ~5 %**
  - P2 is consistent with the simulation
  - The degree of imperfect pole zero cancellation is proportional to Vcal*Tp
  - Baseline 900mV has smaller degree of imperfect pole zero cancellation as baseline 200mV

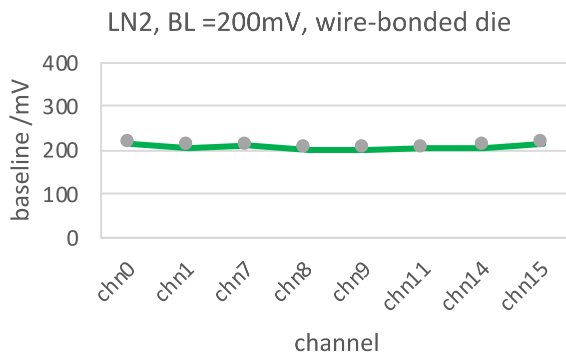


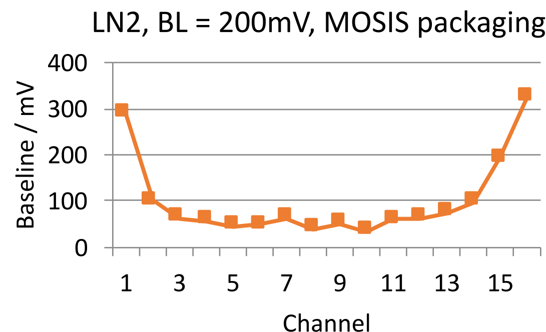


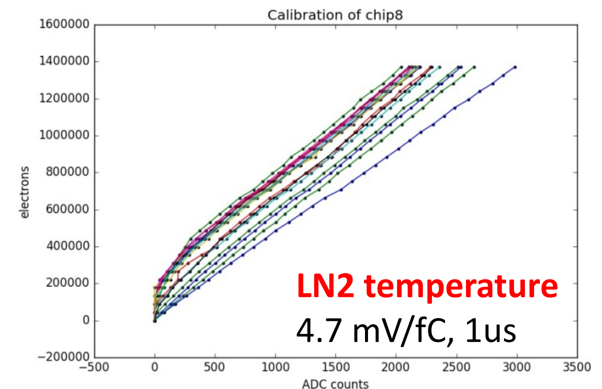
Simulation plot

Baseline Distortion Caused by Packaging (1)

- The baseline distortion is caused by excess stress from thermal pad and packaging stress in cryogenic operation
  - No degradation of baseline and good linearity on all channels with wire-bonded dies
  - ~10 types of packaging solutions from different companies were investigated
    - Quik-Pak, NovaPak, MOSIS/ASE
  - When the baseline is lower than 100mV, the FE channel may fail to amplify the injected pulse properly
- Why not see in MB (V4*) FE ASIC
  - The molding compound used in the package of MicroBooNE FE ASIC has smaller CTE (8 ppm/C), unfortunately that packaging house went to bankruptcy
  - The molding compound used in the new package has larger CTE (12 ppm/C)

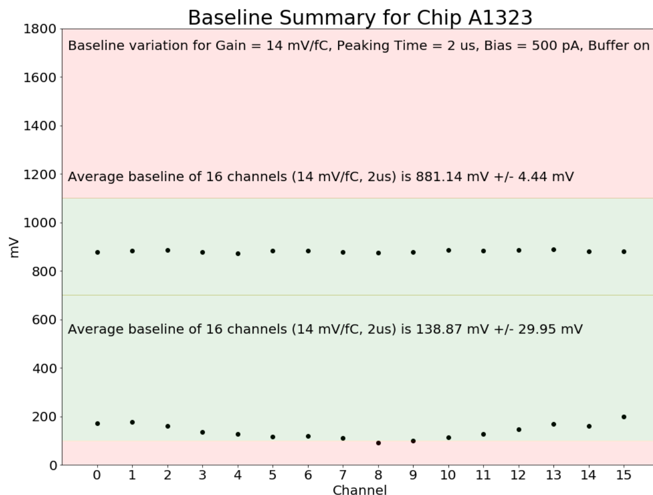






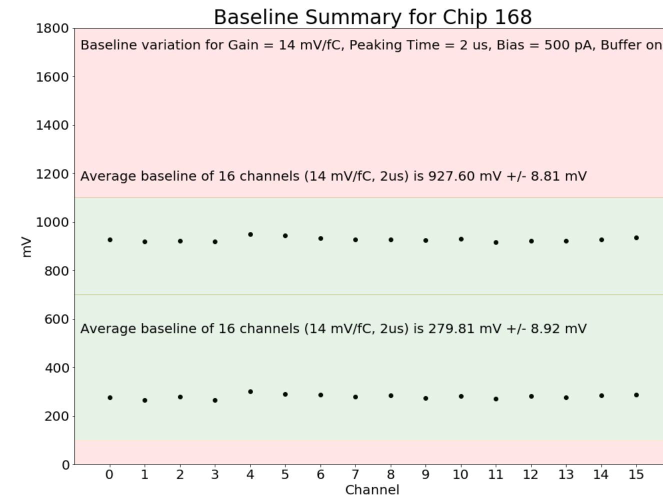
Baseline Distortion Caused by Packaging (2)

- Solution for **P2 FE ASIC**
  - MOSIS/ASE provides the best packaging solution
    - Low stress compound w/o thermal pad
    - Imperfect solution, **the baseline distortion still exists** though > 99% chips have baseline > 100 mV
      - Cold screening with a criterion of BL > 100 mV is required
- Changes on **P3 FE ASIC** design
  - Modify DC circuits for collection mode similar as the induction mode
    - Uniform baseline is observed with BL 200 mV with P3 FE ASIC



Version	P2	P3
Total	1146	188
BL failures	4	0
	0.35%	0.00%

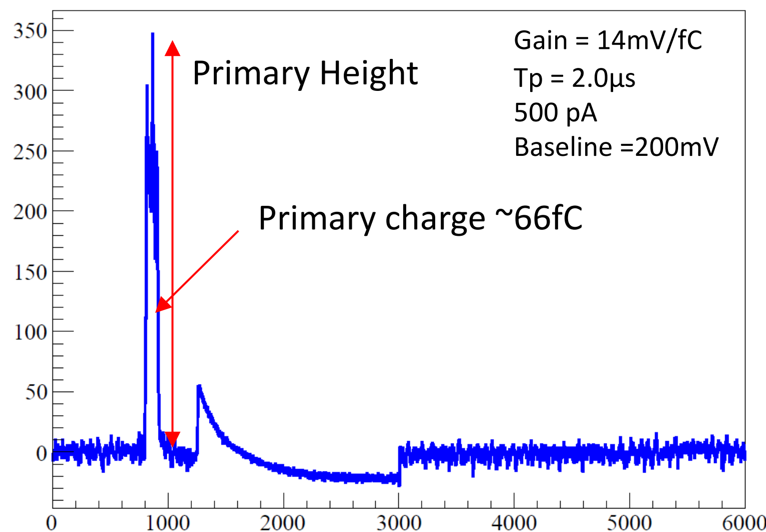
BL failures: A chip with any channel BL < 100 mV is treated as a bad chip



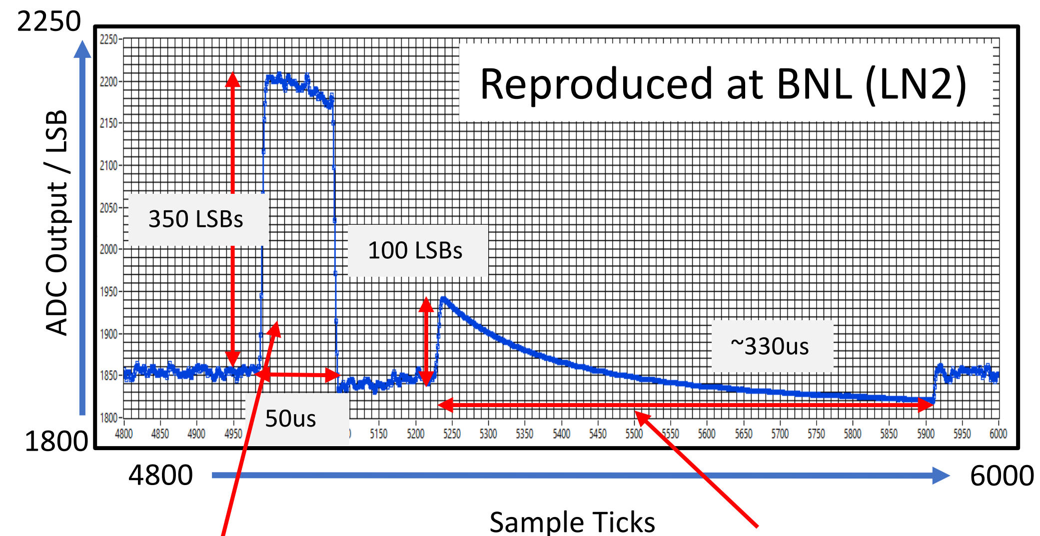
Ledge Effect on P2 FE ASIC (1)

- It comes from circuit related to FE pre-amplifier
  - Ledge threshold at 200mV FE baseline is as low as ~60fC.
  - Ledge threshold is significantly increased with 900mV FE baseline
  - The cause of ledge is explained in Nara's slides
- Dispersion has been found in the charge thresholds to create a ledge
  - This has escaped ASIC testing for ProtoDUNE-SP (P2)
  - No ledge behavior has been observed in MicroBooNE (V4*)

Channel 7205 (Run 4696, Event 328)



First observed in ProtoDUNE-SP (LAr)



Total charge ~225fC;

Saturated Region

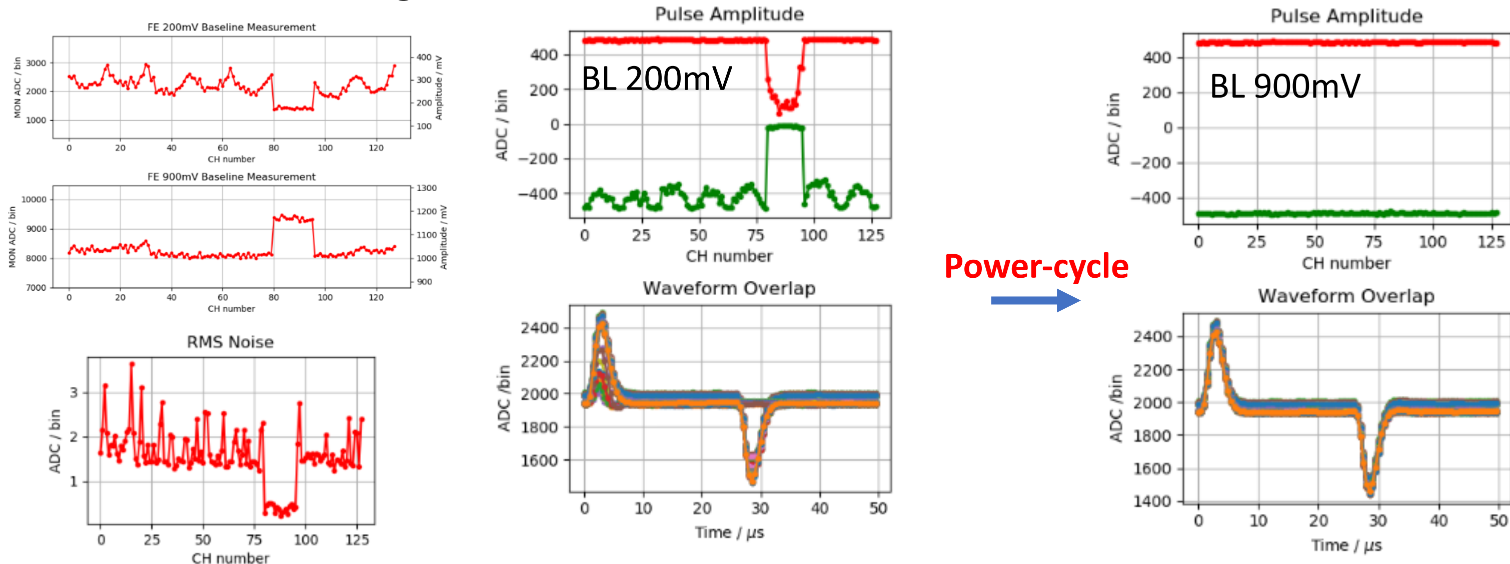
It appears that a large *and long* induced current signal is more likely to create a ledge

Ledge Effect on P2 FE ASIC (2)

- Ledge effect is not observed on MB (V4*) and P1 FE ASIC
- Same ledge effect is observed on P3 FE ASIC
- Mitigation solution for ProtoDUNE-SP
  - By switching the FE baseline to 900mV, ledge events have been reduced to a negligible amount
    - 900mV baseline has ~3X higher charge threshold to show ledge effect
    - 107 events @ 7GeV beam, ledges found on only 2 channels among 2560 channels with 900mV FE baseline setting.
- Further mitigation solution for APA7/SBND
  - 470 MOhm resistor is placed at each FE input and ground to increase the ledge threshold
    - Ledge threshold @ 200mV FE baseline > 200fC
    - No ledge effect observed @ 900mV FE baseline
    - FE baseline shift with 470MOhm reduces dynamic range slightly
    - Combined by 470 MOhm at FE input, the noise increases about $30e^-$

Cold Start-up on P2 FE ASIC

- Cold start-up is likely related to the BGR circuit (more in Nara's talk)
  - By chance abnormal behaviors observed at cryogenic temperature
  - 4 out of 1024 FE chips on ProtoDUNE-SP were identified with start-up
    - No cold screening procedure for these 4 chips applied in APA1-APA5
    - They passed the FEMB thermal cycle test
    - Power-cycle and 900mV baseline setting may bring them back to alive
  - Some FE chips may be at the threshold of start-up
    - Observed from FEMB production for APA7 and SBND that some FE chips escaped from the cold screening test as well



Baselines, noise, response to charge pulser are abnormal when start-up at LN2

Note: plots are provided from a SBND FEMB LN2 pre-screening

P2 FE ASIC QC for ProtoDUNE-SP

- FE ASIC chips for APA1 to APA5 passed QC test at RT
  - Criteria for passing: selection cuts for uniform FE response
    - Combine results over many ASIC test cycles for each channel to get expected pedestal, gain and ENC distributions
    - Cut ASICs with any of those values >5 sigma from channel expected response
  - 1,850 chips tested at warm
    - Rejected ~113 (5.6%) with warm selection cuts
  - Thermal cycle test on FEMB rejected and replaced FE failed at LN2
    - 1 chip on two FEMBs (8x2) failed at LN2 (~6%)
- FE ASIC chips for APA6 passed QC test at both RT and LN2
  - Rejected ~4% of the FE ASICs in the cold screening test
    - Collection baseline < 100 mV
    - Failed to observe calibration pulse
    - Power cycle failure (start-up issue)
    - Input pin dead to external pulse
  - Only 1 FE ASIC replaced on all 21 FEMBs for APA6 (~0.6%)
- FE ASICs were tested under the thermal cycle (RT --> LN2) on FEMB

FE ASIC during ProtoDUNE-SP Installation and Commissioning

- Installation
  - A FE channel on a FEMB was likely contaminated
    - Sweaty hand, oil, dust
    - Inactive at warm but back to alive at cold
  - ESD damage caused by handing
    - 7 channels on 6 FE chips were inactive though strict ESD protection procedure was followed
  - FEMBs with issue were replaced
- Commissioning
  - Warm checkout before LAr filled (07/08/2018)
    - 1 inactive FE channels (back to alive at cold, likely contaminated)
  - Cold checkout after LAr filled (09/13/2018)
    - Only 4 channels on 4 FE chips were inactive at cold
  - Detector operation configuration (180kV drift on, bias on)(09/23/2018)
    - 4 FE ASICs on 4 FEMBs on APA1-APA5 suffer start-up issue
      - They can be brought back to alive by power-cycle
  - 2 more inactive channels on APA6 were observed Nov.27, 2019

P2 FE ASIC QC for APA6/APA7/ICEBERG/SBND

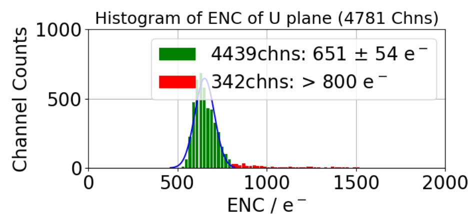
- 1561 FE chips went through cold screening test
  - First run with 1146 chips in Summer, 2018
  - Second run with 415 chips in Winter, 2019
  - Chips passed the test are applied for APA6/APA7/ICEBERG/SBND
  - Warm screening was skipped
    - Skipping warm screening test can save time but not a good practice
      - Some defect FE channels may inactive at warm but active at cold
  - Overall yield is ~90%

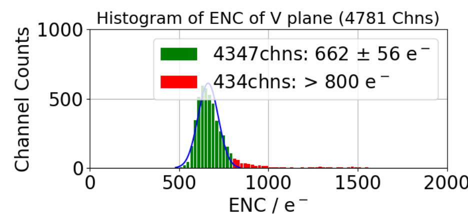
Run#	1st Run	2nd Run
Failure Mode at LN2	# of chip	# of chip
Baseline out of range	4	0
No response to calibration pulse	2	2
Power cycle failure (start-up issue)	14	9
Input pin dead to external pulse	22	6
Other failures (socket issues or other errors)	67	15
Total failures at LN2	109	32

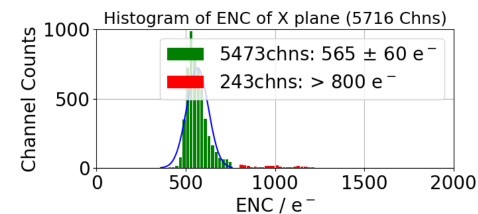
3.8%

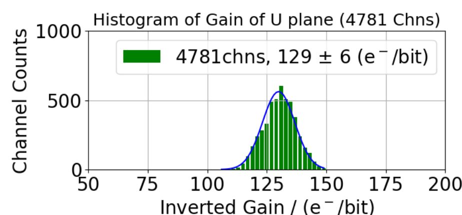
P2 FE ASIC in ProtoDUNE-SP Operation

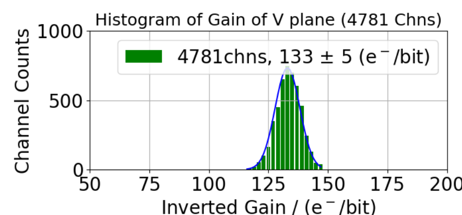
- Promising noise performance with drift and bias on
  - ENC of **collection (X) plane** (5473 of 5760 channels) : **565 ± 60 e⁻** (raw data)
  - ENC of **induction (V) plane** (4347 of 4800 channels) : **662 ± 56 e⁻** (raw data)
  - ENC of **induction (U) plane** (4439 of 4800 channels) : **651 ± 54 e⁻** (raw data)
- Uniform gain measured by on-board calibration pulser
  - Inverted gain of collection (X) plane: **135 ± 6 e⁻/bit , 0.59% Nonlinearity**
  - Inverted gain of induction(V) plane: **133 ± 5 e⁻/bit , 0.81% Nonlinearity**
  - Inverted gain of induction (U) plane: **129 ± 6 e⁻/bit, 0.78% Nonlinearity**
  - Note: Nonlinearity is mainly contributed by on-board calibration pulser (FE-ASIC nonlinearity < 0.5%)

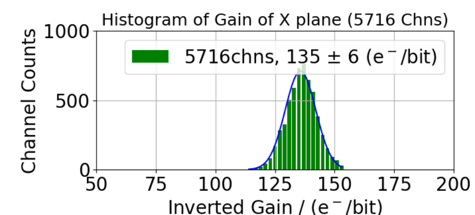


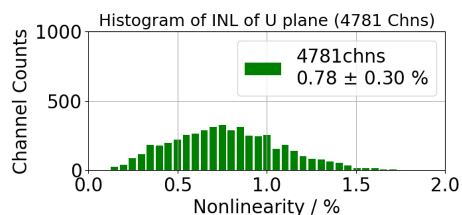


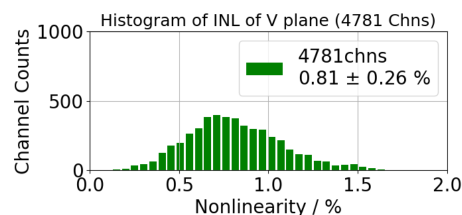


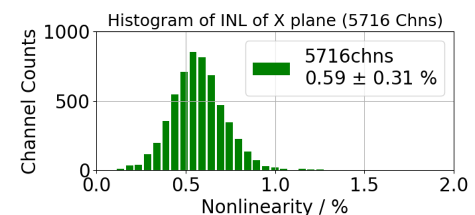






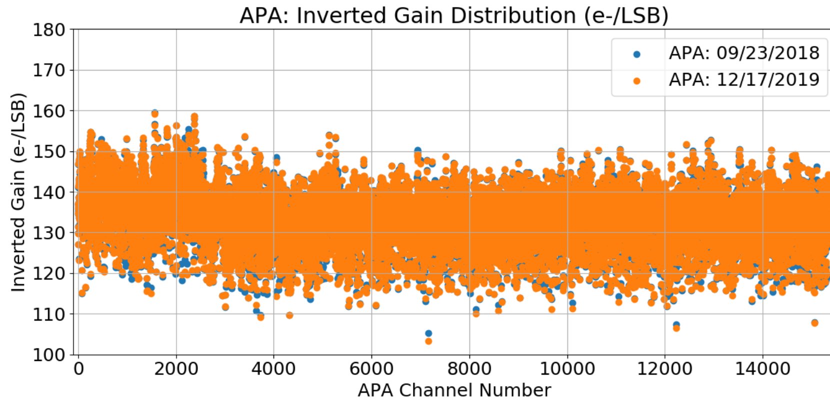


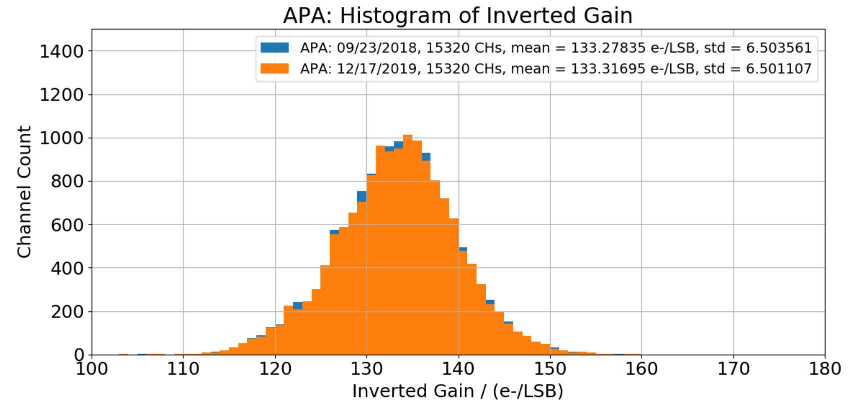




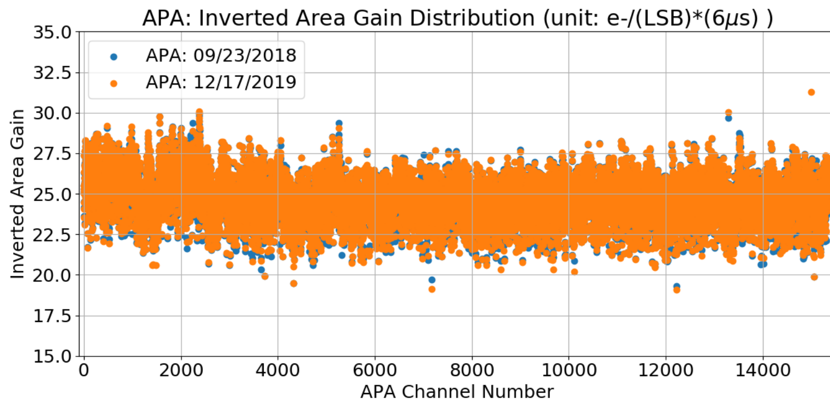
Stability of CE in ProtoDUNE-SP

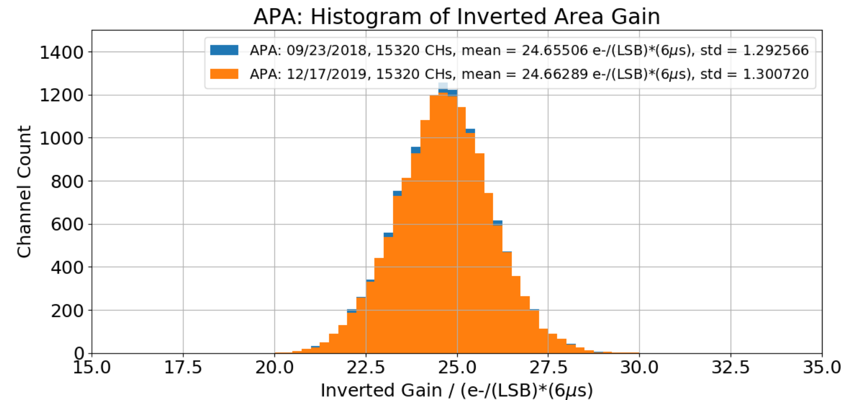
- No measurable degradation is observed over a year





Gain calculated from peaks indicates no degradation (0.03%) in the pulse amplitude





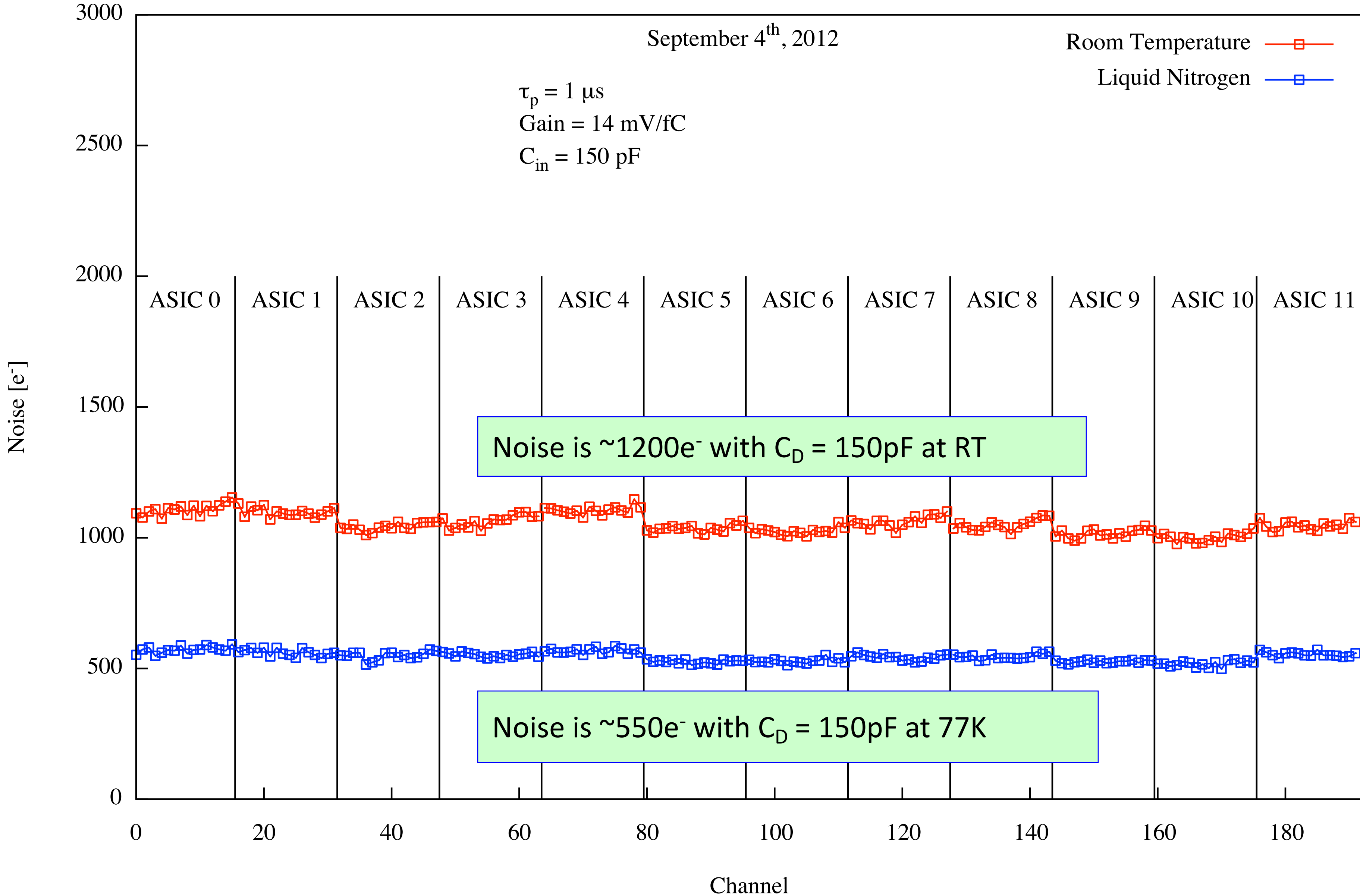
Gain calculated from areas indicates no degradation (0.03%) in the shape of pulse waveform

Summary

- A series of test stands have been developed at BNL to characterize performance and screening FE ASICs rapidly
- **LArASIC is proved to be a good front-end chip with excellent performance for cryogenic operation**
  - P2 FE ASIC has been instrumented in ProtoDUNE-SP successfully
    - Baseline distortion is mitigated by MOSIS packaging with low stress compound w/o thermal pad
    - Pole-zero cancellation is significantly improved
    - Ledge effect is addressed with mitigation solutions
    - Cold screening test is required due to ~4% P2 failed at cold
  - P2 has been chosen to instrument SBND as well
- P3 FE ASIC addressed the baseline distortion in the design
- P4 FE ASIC is being designed
  - Continuous improvements for a robust design for DUNE Far Detector
  - To address the ledge effect and add SE-DIFF converter

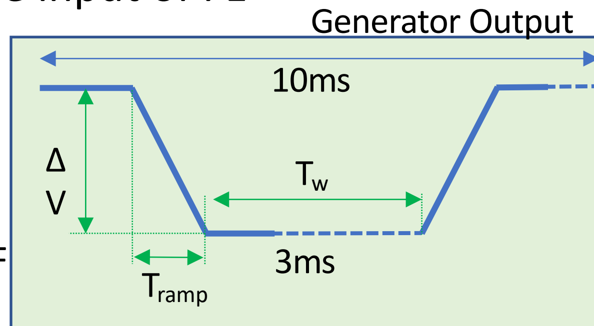
Backups

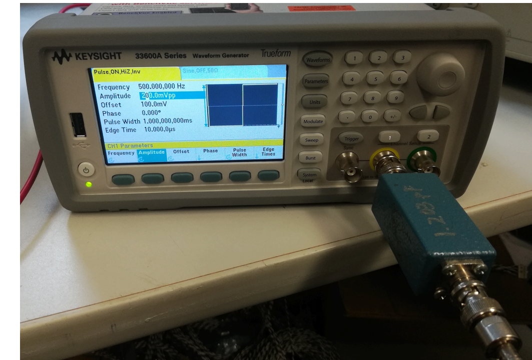
Noise *vs.* Temperature: 12 ASICs (192 channels) (MicroBooNE)



Emulating Shower Signal in FEMB Bench Testing

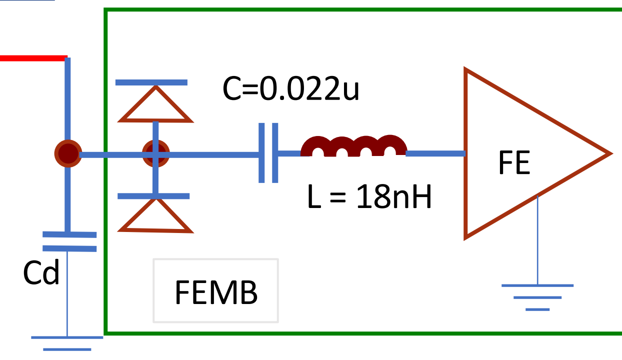
- One FEMB with Toy TPC (Cd = 150pF) in LN2
- Calibration pulse injected to the input of FE
  - Waveform generator 33600A
    - Amp (ΔV) = Programmable
    - Freq = 100Hz
    - Pulse width (T_w) = 3 ms
    - T_{ramp} : programmable
  - Calibration Cap (C_{cal}) = 1.203 pF
  - **FE setting**
    - **14mV/fC, 2us, 500pA,**
    - **BL (FE) = 200mV / 900mV**



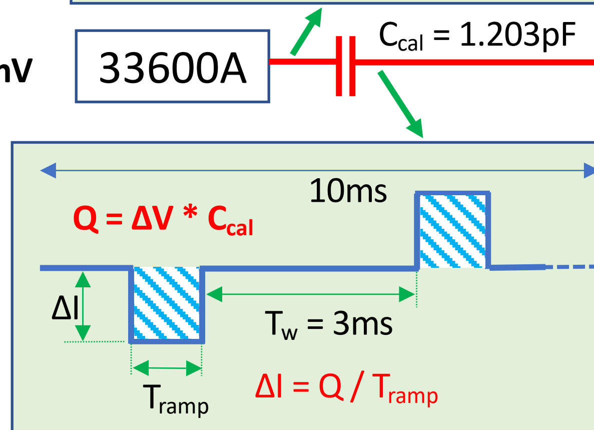


33600A

C_{cal} = 1.203pF

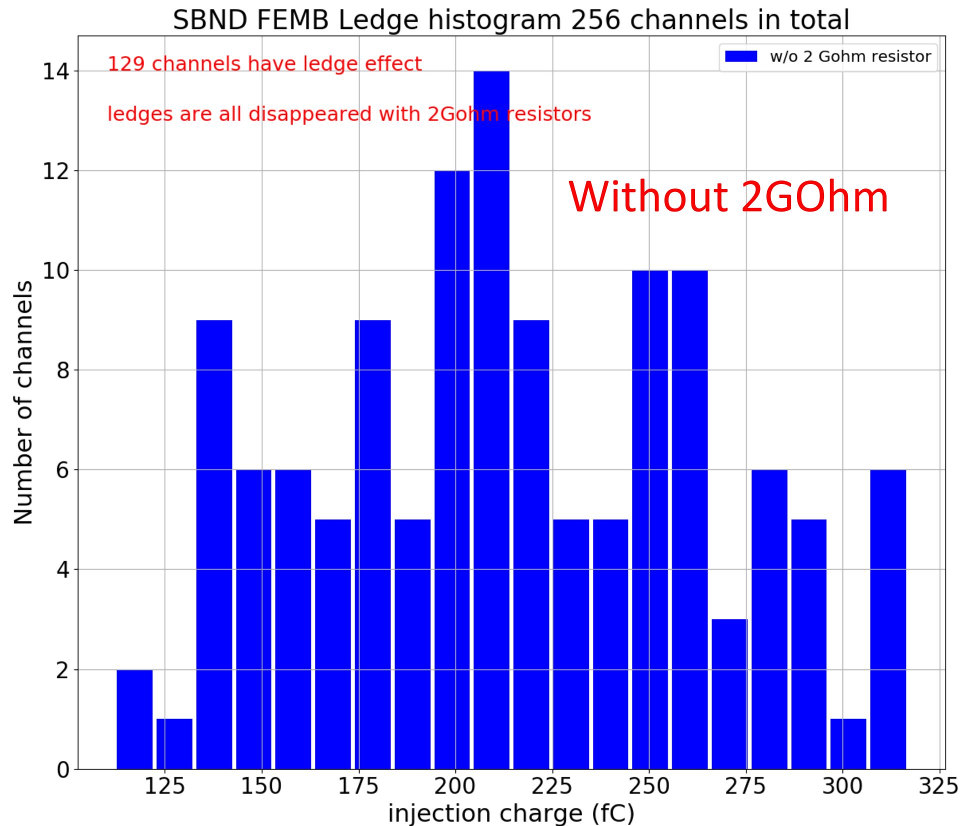


Shower signal induces current.
Ramp signal through capacitor to emulate the current



Ledge Effect Test on SBND FEMBs

- 2 SBND FEMBs (total 256 channels) are tested with and w/o 2 GOhm

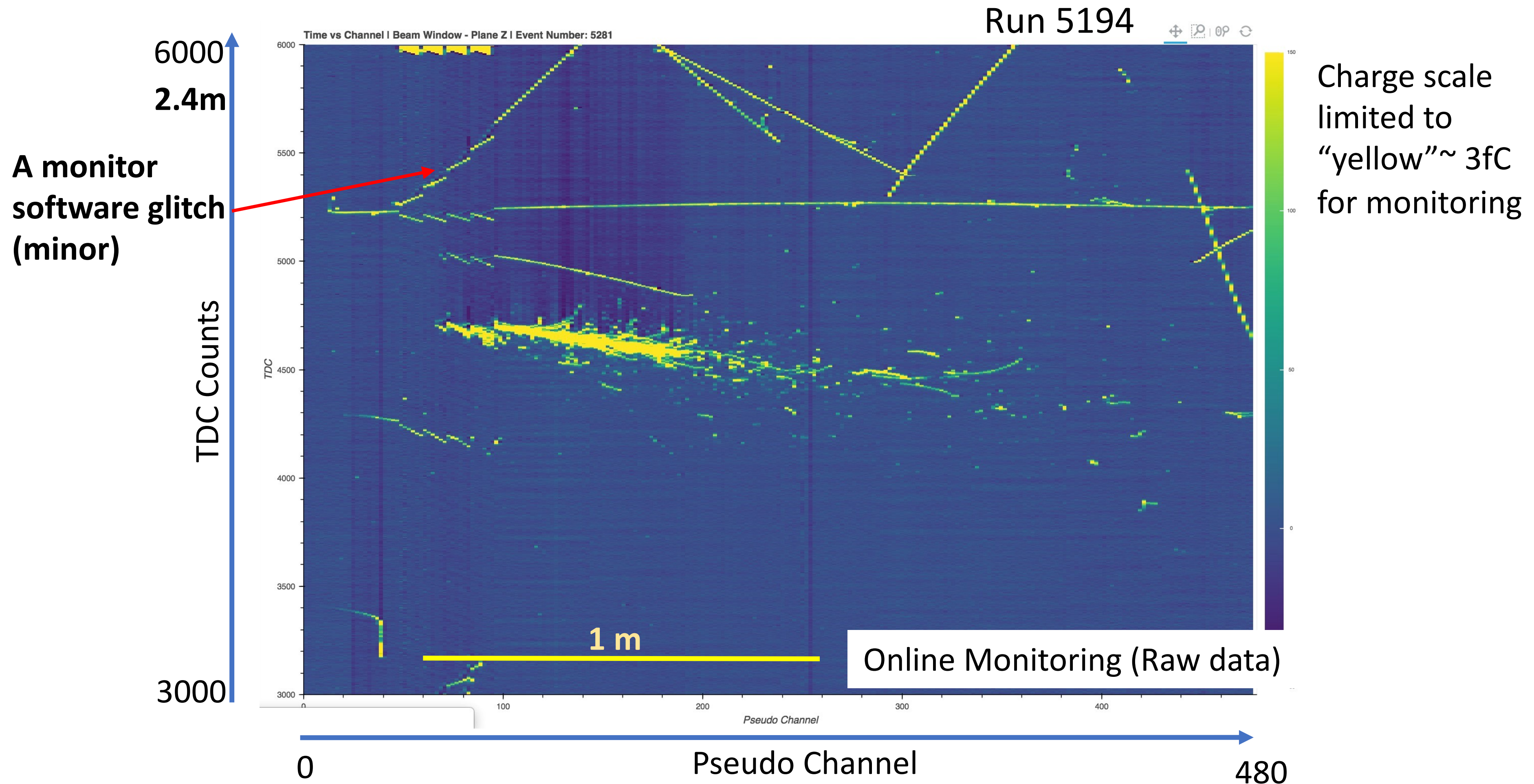


- ➢ FE internal cap (185fF) combined with external calibration pulse from generator can get charge up to 333 fC
- ➢ **900mV** FE baseline
- ➢ Without 2 GOhm， ~50% channels has ledge threshold < 325 fC
- ➢ **With 2 GOhm, no ledge effect < 333fC observed**

As a reference, ProtoDUNE FEMBs don't have 2 GOhm resistor.
107 events @ 7GeV beam, ledges found on only 2 channels among 2560 channels with 900mV FE baseline setting.

Shower Event with 900mV Baseline under 7Gev Beam

- ProtoDUNE has changed the baseline to 900mV
  - ledge events have been reduced to a negligible amount



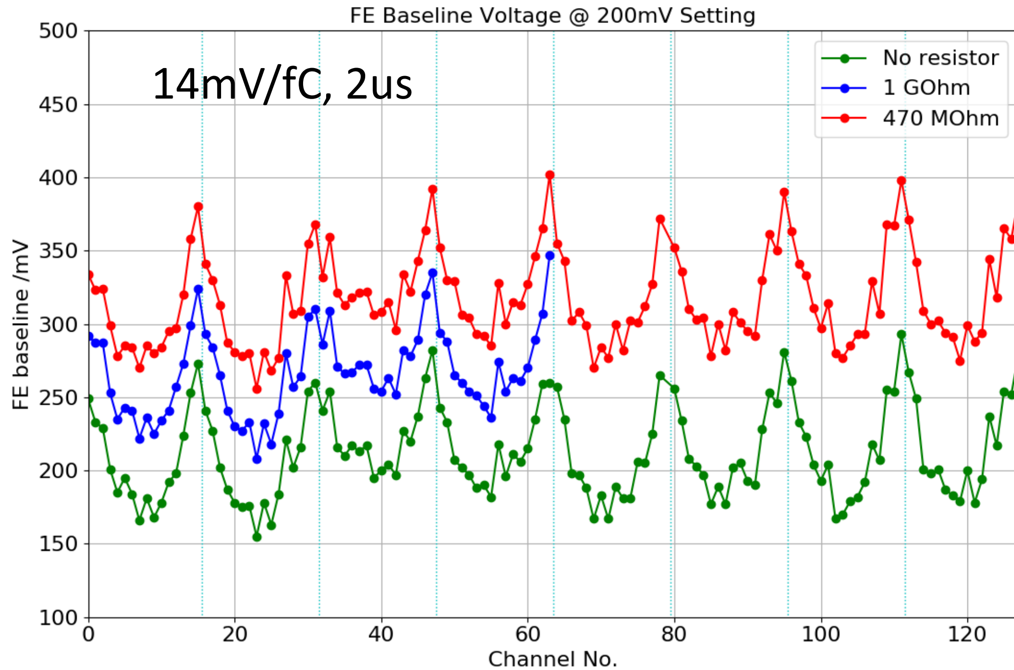
P2 FE ASIC Dynamic Range Study

- The requirement for the upper end of dynamic range at 60.8 fC

FE Baseline	Gain / (mV/fC)	Dynamic Range From Design / fC	With External Cap (1.203pF)	
			ΔV when FE saturation / mV	Charge when FE saturation / fC
900mV	25	36	28	34
	14	**64**	51	**61**
	7.8	**115**	93	**112**
	4.7	191	151	182
200mV	25	64	50	60
	14	114	88	106
	7.8	205	160	192
	4.7	340	265	319

- The FE dynamic range of each channel is same, which is unrelated to ledge effect
- Gain of 14mV/fC barely meets the upper end of dynamic range requirement (60fC)
  - One may use 7.8mV/fC gain instead to keep margin of the upper end of dynamic range
- At the same time, the resistors will be added at FE ASIC input to mitigate ledge effect
  - Optimization of input resistance is being studied, which doesn't require layout change of FEMB

External resistor shifts FE baseline up

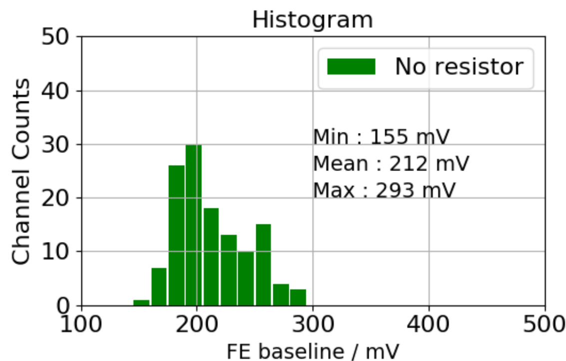


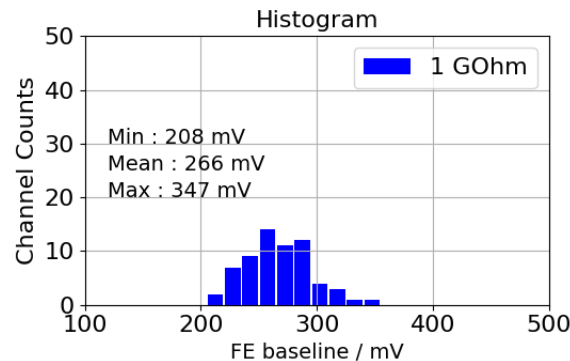
FE Baseline 200mV

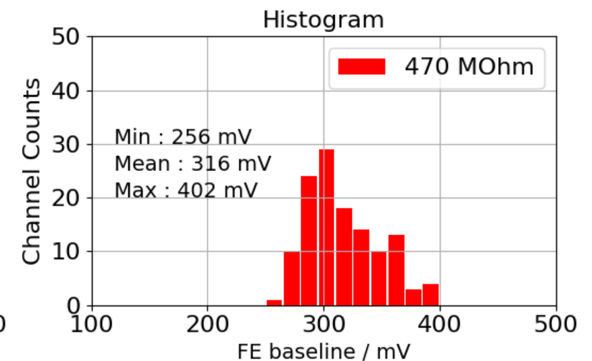
470MOhm makes FE baseline rise about **100mV/50mV**, which decreases the dynamic range of FE response.

14mV/fC: 106 – **100/14** = 99fC

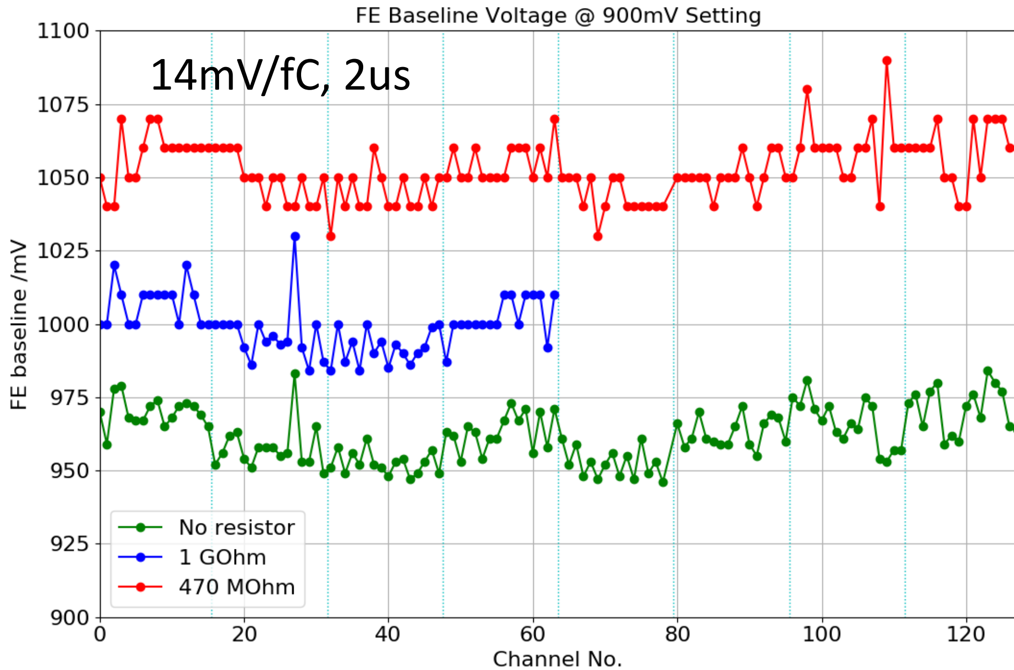
7.8mV/fC: 192 – **50/7.8** = 186fC







External resistor shifts FE baseline up

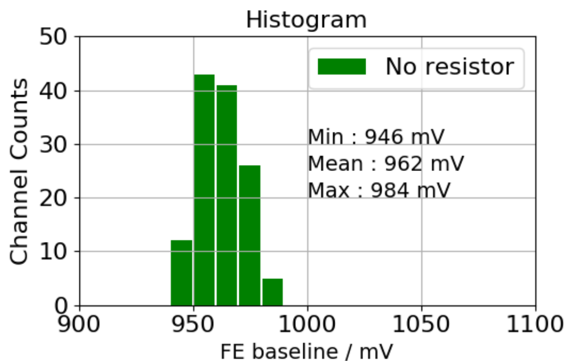


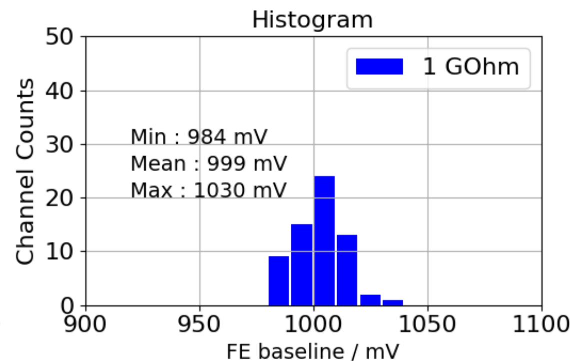
FE Baseline 900mV

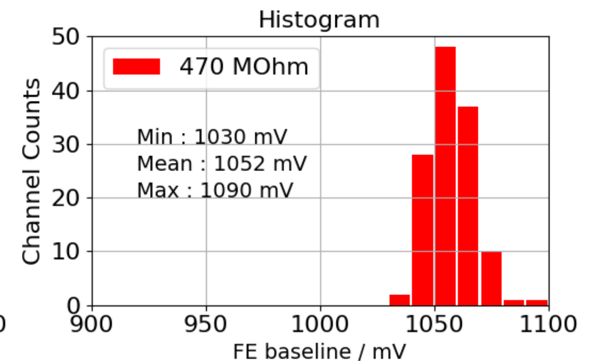
470MOhm makes FE baseline rise about **100mV/50mV**, which decreases the dynamic range of FE response.

14mV/fC: 61 – **100/14** = 54fC

7.8mV/fC: 112 – **50/7.8** = 106fC

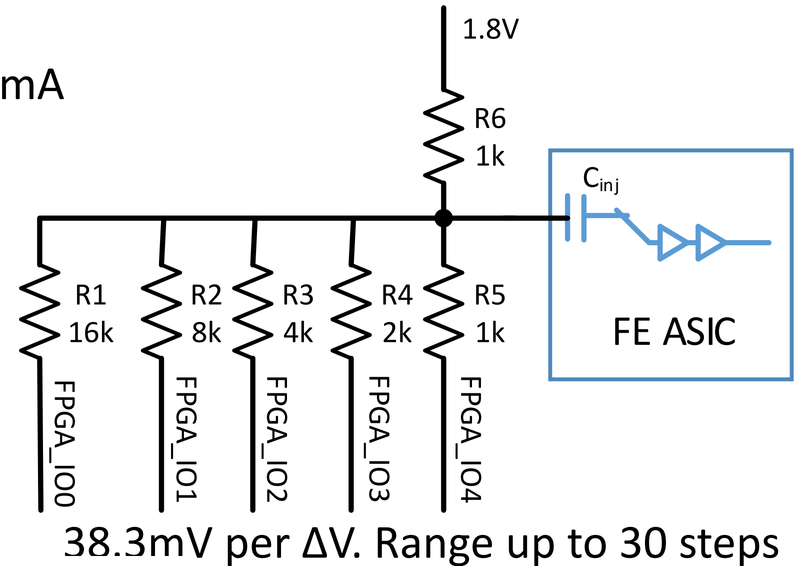




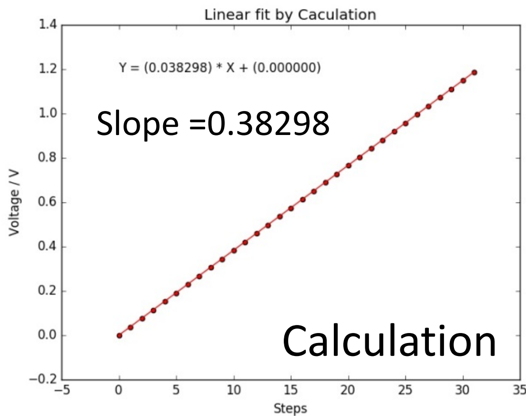


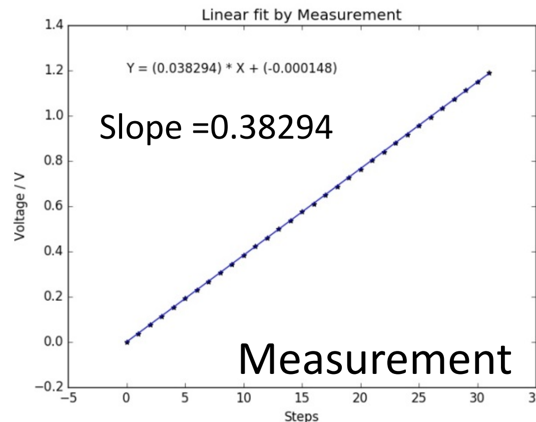
Pulse Generator: FPGA "DAC"

- Schematic
  - FPGA IO source or sink current limit: 2mA
  - Maximize source current: 0.574mA
  - Maximize sink current: 1.187mA
  - R6 = 1kΩ
  - **R1 = 16.02kΩ (1%)**
  - **R2 = 8.06kΩ(1%)**
  - **R3 = 4.02kΩ(1%)**
  - **R4 = 2.00kΩ(1%)**
  - **R5 = 1.00kΩ(1%)**



38.3mV per ΔV. Range up to 30 steps



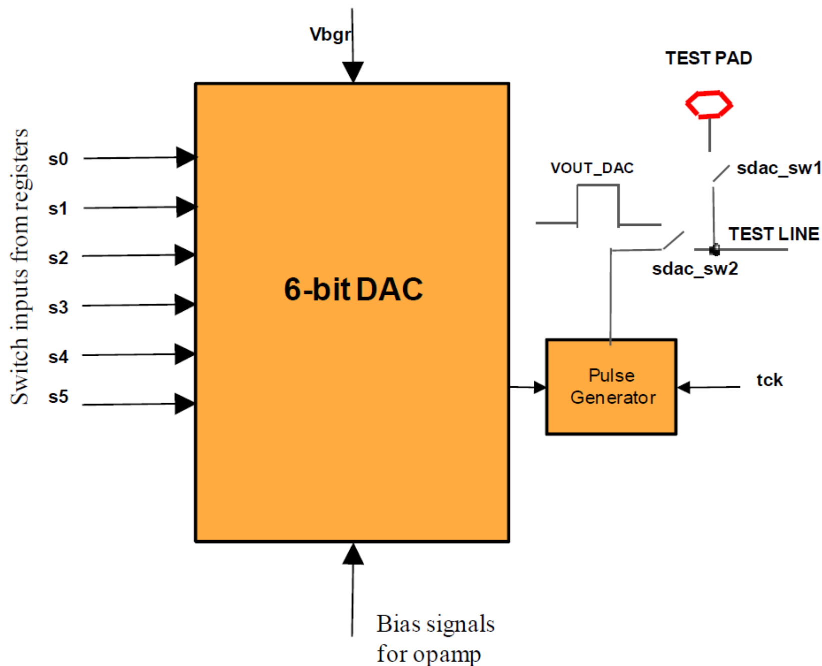


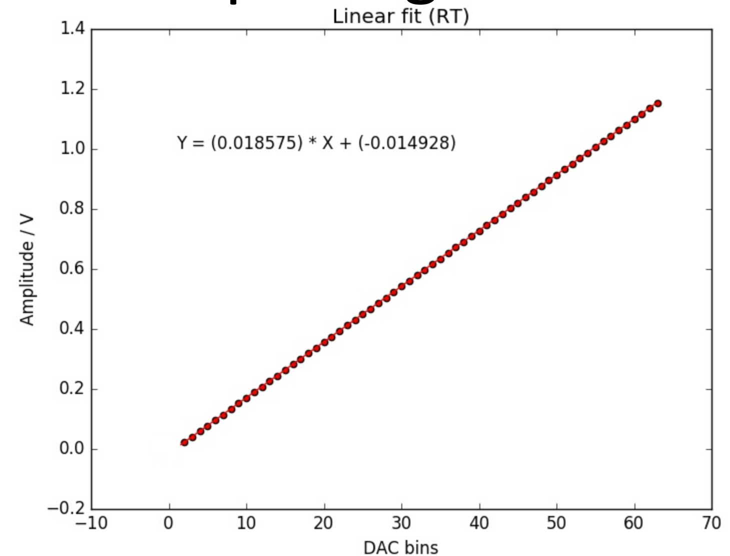
FPGA "DAC" works well at both room and LN2 temperatures

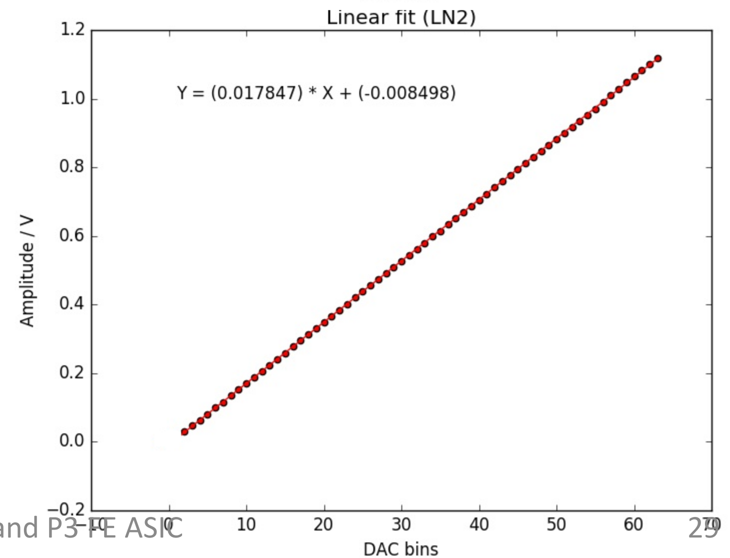
Very good agreement between calculation and measurement

Internal Pulse Generator of P1 FE-ASIC

- P1 FE ASIC integrated 6-bit internal pulse generator



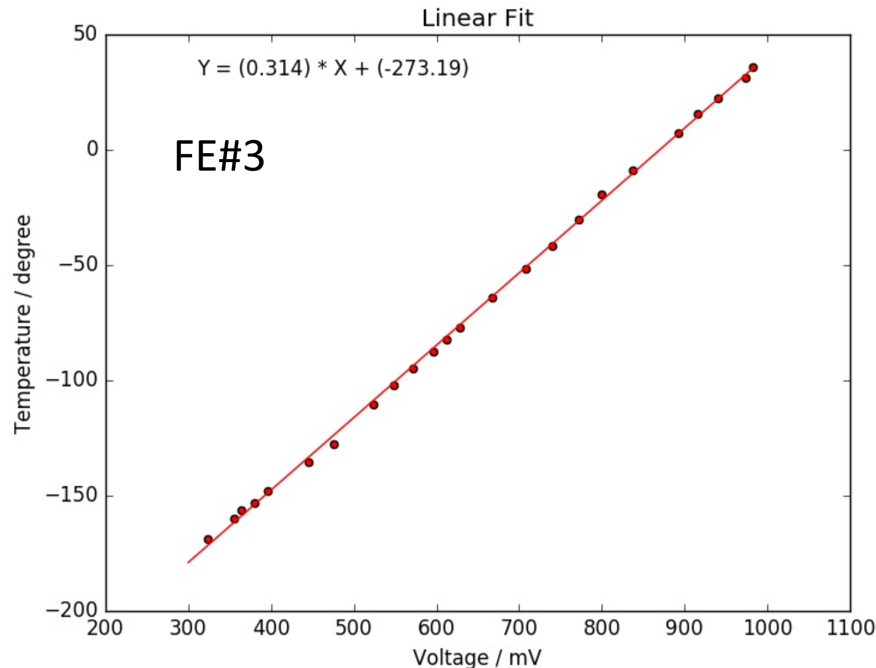


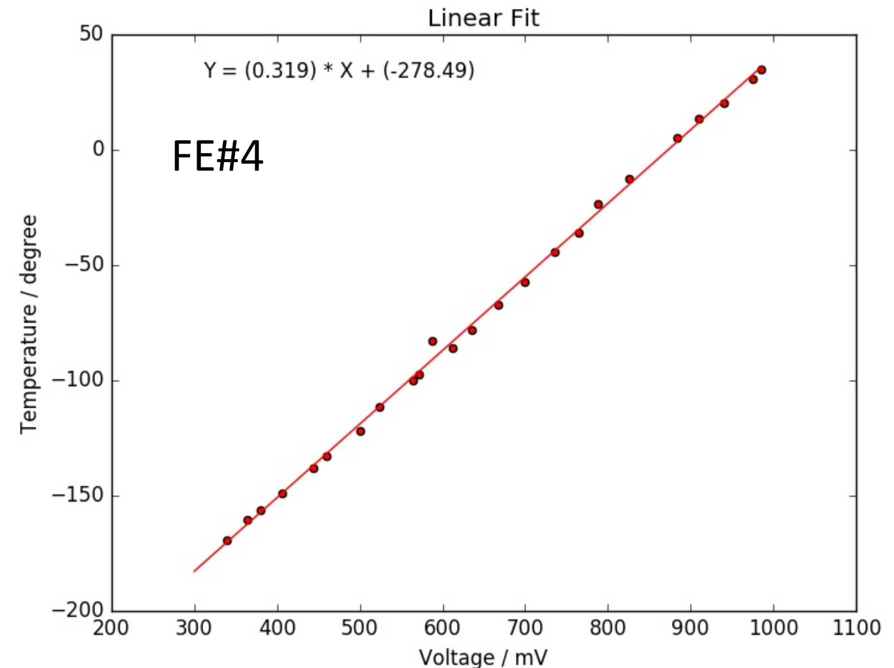


- Output Voltage Range: 0 to 1.18V
- Resolution: 18.75mV
- Power: 1mW
- Temperature Range: 27°C to -200°C
- Settling time: < 130ns
- Linearity: $\pm$ 0.12 %

Temperature Calibration at BNL

- Two FE chips on AM#27 were used for temperature calibration at BNL with same setup (7m data cable and 15m LEMO cable) as CERN
- Thermometer
  - OMEGA HH374 (-200 to 1372 °C)

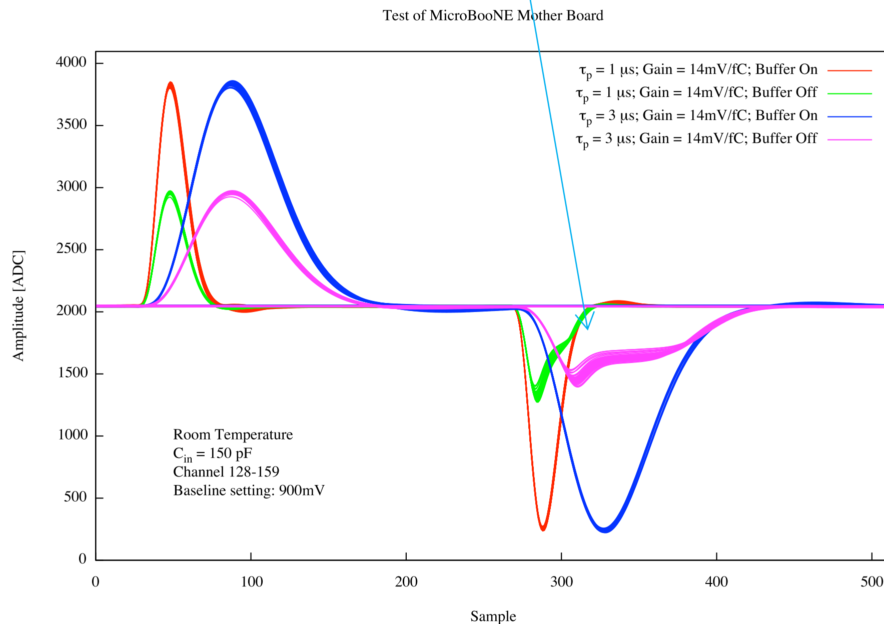




Calibrated parameter from FE#3 is applied to calibrate cold box FE temperature data

Test result of Buffer-off Drive Capability of Last Stage

- MB FE ASIC
  - To prevent distortion on positive (switches) and negative pulses
  - ***Distortion in bench test***



- P1 FE ASIC
  - Increase the buffer-off drive capability of last stage

- P1 FE ASIC
  - To prevent distortion on positive (switches) and negative pulses
  - ***Distortion is resolved in bench test***