Cold FE ASIC Schedule & Test Plan

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Outline

- Introduction
- Schedule of Cold FE ASIC Development
- Test Plan of Cold FE ASIC
- Summary

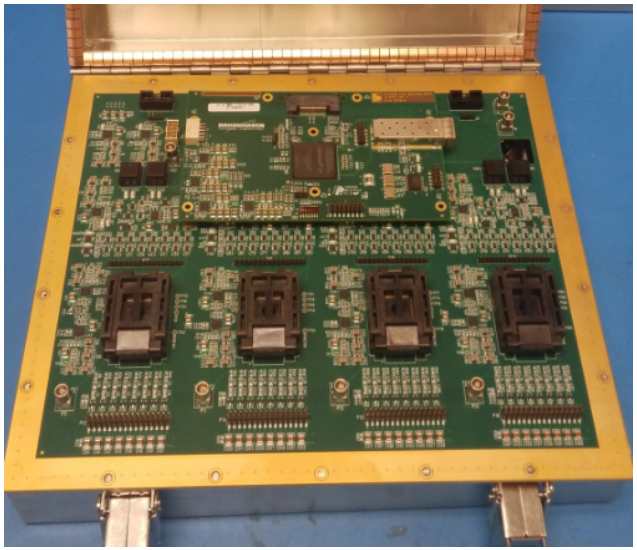
Introduction

- Cold FE ASIC is continuing development towards a robust design adaptable to future design rule and process technology changes for DUNE experiment
- Development of P4 FE ASIC will address the following issues
  - Eliminate ledge effect
  - Add SE-DIFF converter
  - Improve cold start-up
  - Optimize baseline variation
- Test stand is available in the lab to evaluate different versions (V4*/P1/P2/P3) of FE ASICs
  - Provide inputs to the development of P4 FE ASIC

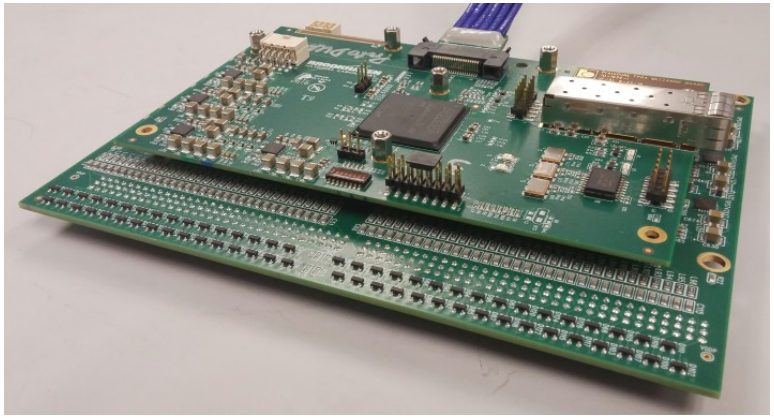
Schedule of Cold FE ASIC Development

- 04/2020: simulation studies concluded, design closed
- 06/2020: post layout simulation concluded, ready for MPW submission
- 09/2020: P4 ASIC MPW run and packaging
  - Contact MOSIS for MPW run of TSMC 180nm
  - Contact IMEC-US for MPW run of TSMC 180nm
  - Contact ISE for packaging
  - Order 240 dies from 6 wafers in MPW run
- 12/2020: P4 ASIC evaluation, preparation of engineering run
  - Make minor update of design if necessary
  - Schedule float of 2 months for system integration test together with ColdADC and COLDATA
- 03/2021: FE ASIC ENG run and packaging
  - Order 6 wafers for ProtoDUNE-II
  - Total ~5,000 dies, sufficient to instrument 10,240 channels
- 06/2021: FE ASIC QC for FEMB production

Test Plan of Cold FE ASIC (1)



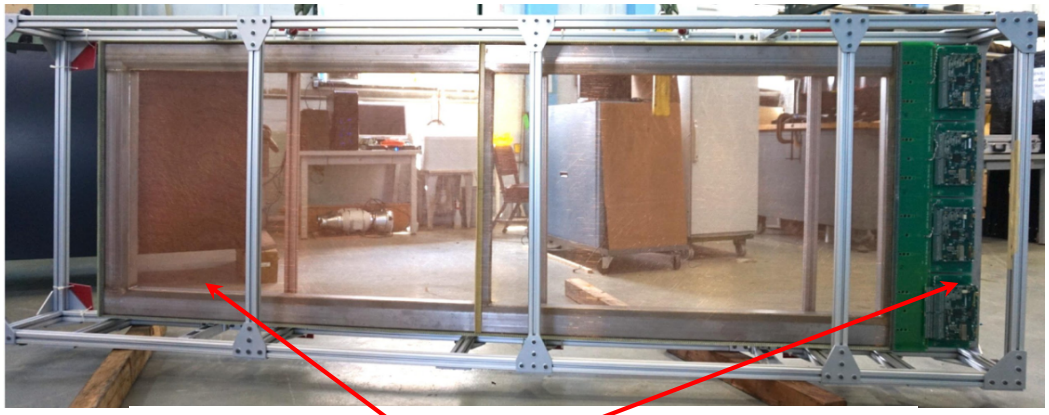
Quad socket FE ASIC test board



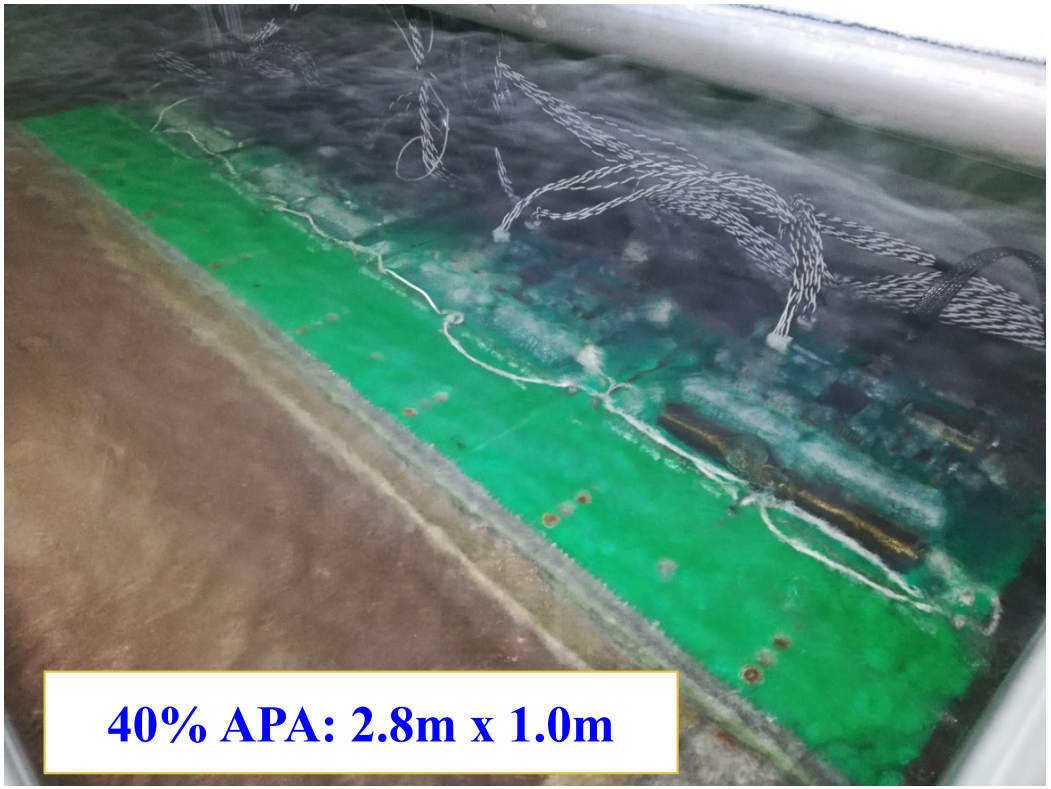
FEMB (inside CE box)

- P4 ASIC MPW run will provide sufficient (~240) chips for lab evaluation and system integration test
- Lab test to check both functionalities and performance
  - Quad socket FE ASIC test board will be used for the lab test
  - FEMB will be used to characterize the performance
  - Both FE ASIC test board and FEMB design will be revised for the different outputs of P4 ASIC
- Integration test will be performed with 40% APA at BNL
  - APA7/ICEBERG (if discharge problem solved) test with 2 months of schedule float

Test Plan of Cold FE ASIC (2)



40% APA (DUNE) and FEMBs



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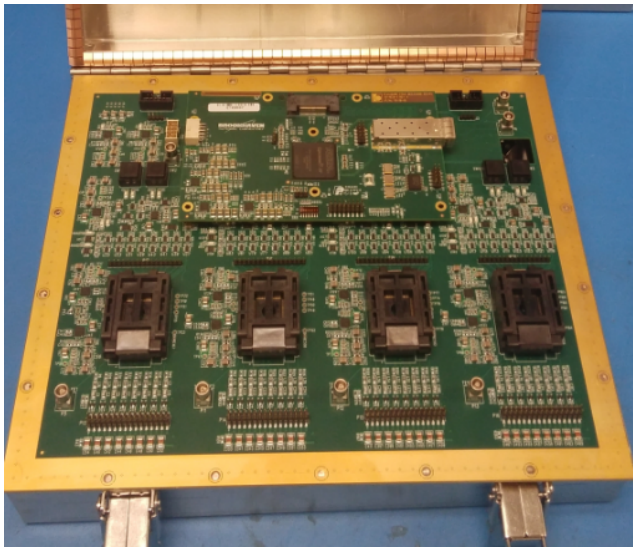
Test Plan of Cold FE ASIC (3)

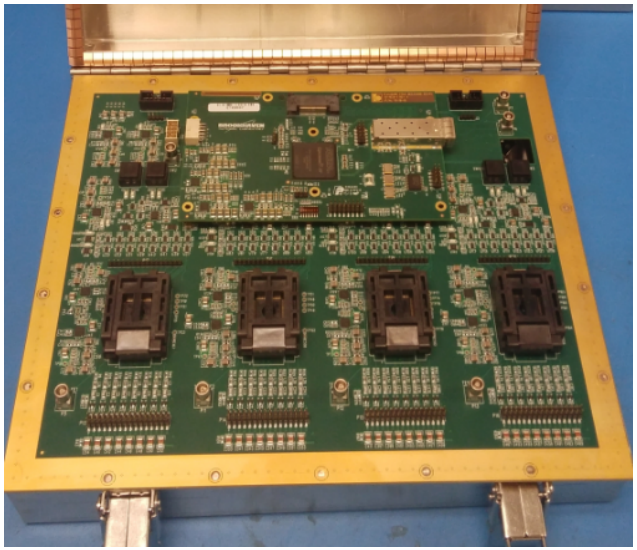


Quad socket FE ASIC test board

Cryogenic Test System (MSU)

- FE ASIC ENG run will provide sufficient chips for ProtoDUNE-II
- QC test for FEMB production will be the main focus
  - Quad socket FE ASIC test board will be ready for the QC warm test
  - Extended version of quad socket FE ASIC test board will be revised for QC cold test
- If cold start-up issue is addressed properly, will re-evaluate the necessity of QC cold test

Test Plan of Cold FE ASIC (4)



Quad socket FE ASIC test board

Cryogenic Test System (MSU)

- QC procedures for the final production are not described in details here
  - They are likely to remain very similar to the ones already used for ProtoDUNE (see Shanshan's FEMB talk)
  - Quad socket FE ASIC test board may evolve to ***octal*** socket board, such that we can meet the required throughput.
  - Some of the selection criteria may change based on the tests done for the ENG run of ProtoDUNE-II

Summary

- Cold FE ASIC is continuing development towards a robust design for DUNE experiment
- Current plan is to have MPW run in 06/2020 and ENG run in 12/2020
  - Nara is the leading engineer for P4 ASIC design
  - Strong support from BNL ASIC team (Mietek, Vamshi, Sandeep and Gregory), ready to mitigate schedule risk
  - MPW run will provide sufficient chips for lab evaluation and system integration test
  - ENG run will provide sufficient chips for ProtoDUNE-II
- Quad socket FE ASIC test board and FEMB will be main test platform for FE ASIC test
  - Extended version of quad socket FE ASIC test board will be revised for QC cold test
  - If cold start-up issue is addressed properly, will re-evaluate the necessity of QC cold test
  - DUNE production QC procedures will be evolving based on ProtoDUNE-II experience

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