Latest Progress of "LArASIC + ColdADC + FPGA" FEMB at BNL

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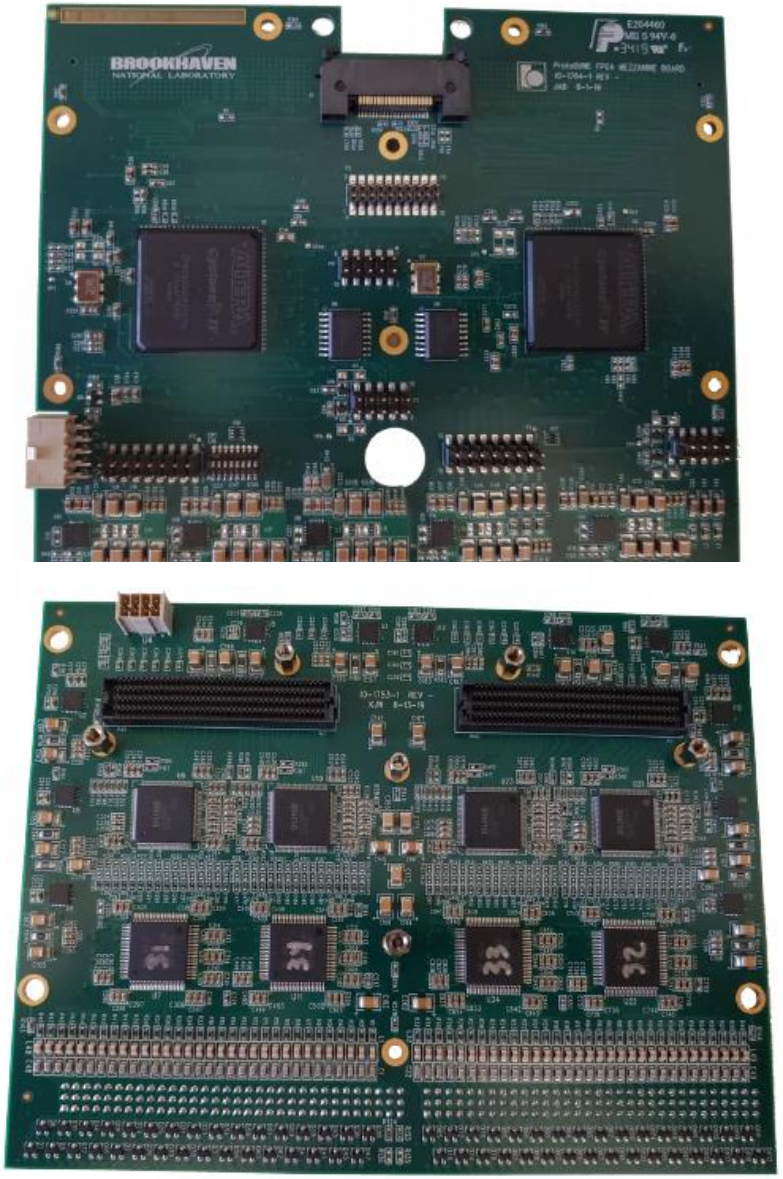
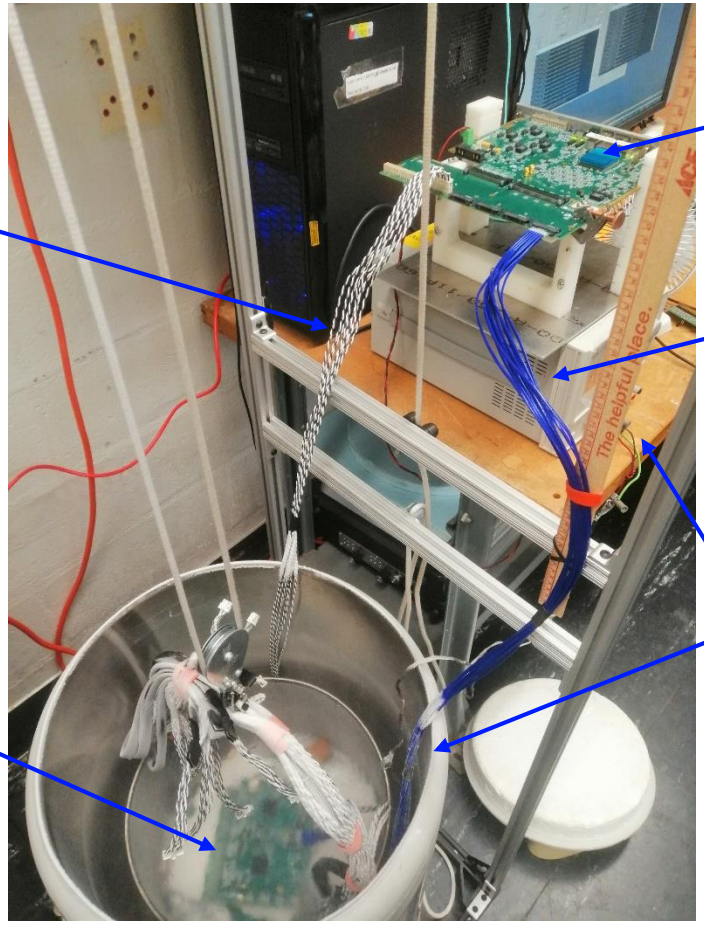
"LArASIC + ColdADC + FPGA" FEMB

- **First FEMB with ColdADC**
  - FPGA Mezzanine (FM) with 2 Altera Cyclone IV GX FPGAs
  - Improved cold data cable with 2 tabs for reliable mounting
- 128 channel DUNE Analog Motherboard (AM)
  - 8x ColdADC chips
  - 8x LArASIC P3 chips
  - Will be compatible with DUNE COLDATA Mezzanine
- Compatible with ProtoDUNE WIB
  - 4 resistors on WIB to be replaced for raising AM supply voltage
  - Configuration scripts will require an update
  - Identical data format/channel mapping as ProtoDUNE FEMB



"LArASIC + ColdADC + FPGA" FEMB

- Work stably at both RT and LN



ProtoDUNE WIB

ProtoDUNE 7m power cable

ProtoDUNE 7m data cable

Dewar is grounded at the power supply

FEMB and Toy TPCs are isolated from Dewar

The common return path of FEMB is only through cold cables

Common Configuration for FEMB

- LArASIC
  - 500pA leakage current, buffer off, DC coupling
  - 2 baselines x 4 shaping times x 4 gains
- ColdADC
  - Power rails
    - VDDA2P5/VDDD2P5 = 2.5V, VDDD1P2 = 2.1V, VDDIO = 2.25V
  - CMOS reference
    - BJT reference is powered down
    - To avoid ADC overflow
      - At RT: VREFP = 0xff (2.371V), VREFN = 0x00 (0.055V), VCMI = 0x60 (0.930V)
      - At LN2: VREFP = 0xe0 (2.257V), VREFN = 0x10 (0.181V), VCMI = 0x60 (0.978V)
  - SDC bypassed, single-ended input
  - Currently ADC data hasn't been manually calibrated
- DC coupling on board
  - FE outputs is directly connected to ColdADC inputs through 0 Ohm
- Dual-FPGA FM
  - Each FPGA controls 4 LArASICs and 4 ColdADCs separately
  - Interface to WIB is same as ProtoDUNE FEMB
- Grounding scheme
  - Follow the ProtoDUNE grounding and isolation rules inside cryostat
    - 7m ProtoDUNE power and data cables
- 120pF Toy TPCs

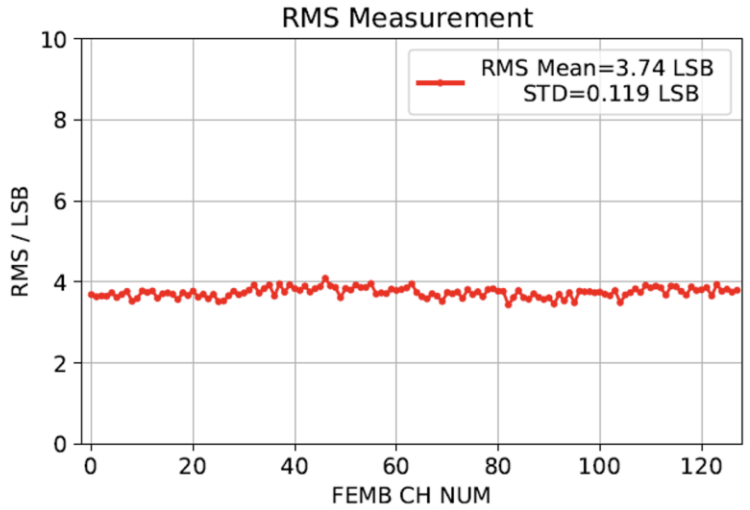
Preliminary Power Consumption

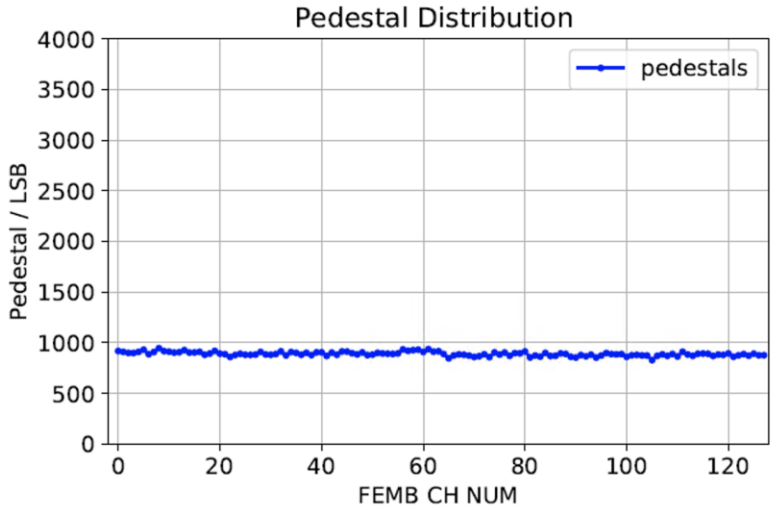
	Voltage measured at WIB side / V	Current measured at WIB side /mA
4.2V for FM	4.20	60
2.8V for FM	2.89	549
1.8V for FM	1.71	418
4.2V for AM	4.24	1915
BIAS for FM/AM	5.00	32

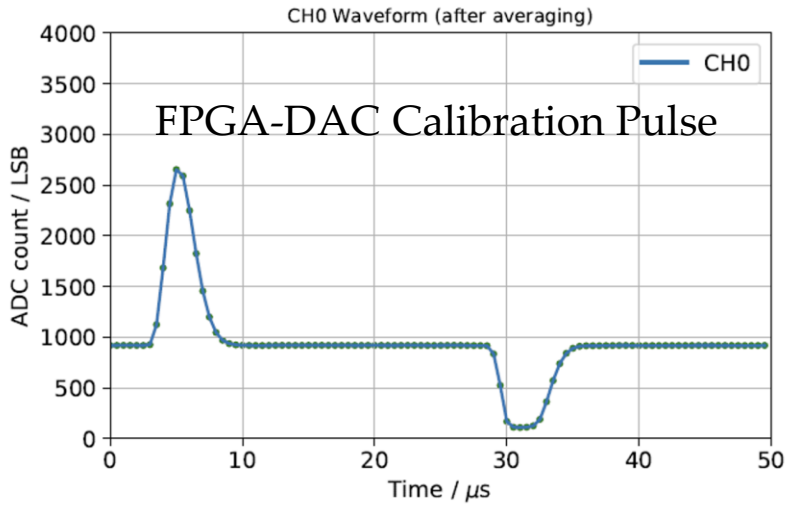
- Currently there is only one 4.2V power rail for both FE ASIC and ColdADC before regulators
  - FE ASIC nominal voltage: 1.8V
  - ColdADC nominal voltage
    - VDDA2P5/VDDD2P5 = 2.5V, VDDD1P2 = 2.1V, VDDIO = 2.25V
  - 8x LArASIC total current = ~450mA at RT
  - 8x ColdADC total current = ~ 1450mA at RT
  - The voltage loss through 7m cable is ~180mV through 4.2V (AM) power line
    - 3 AWG20 wires for 4.2V(AM)
  - 4.2V(AM) can be optimized to 3.0V to lower the power drop on regulators

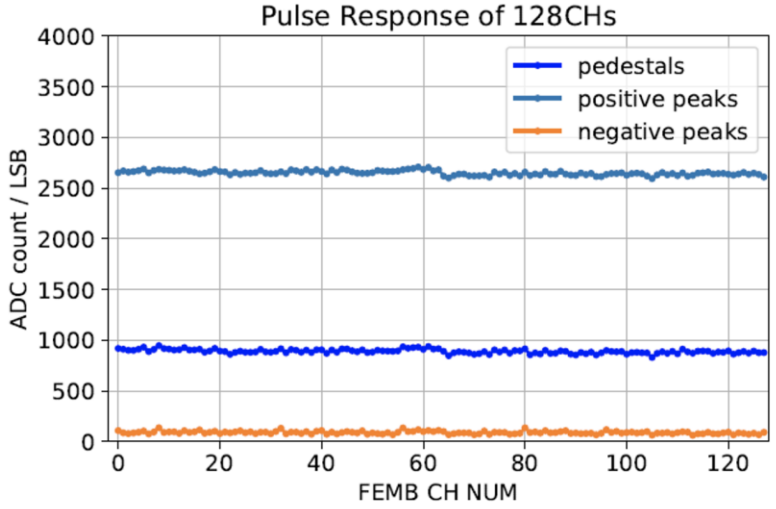
Checkout Result at Room Temperature

FE: 14mV/fC, 200mV BL, Tp 2.0μs





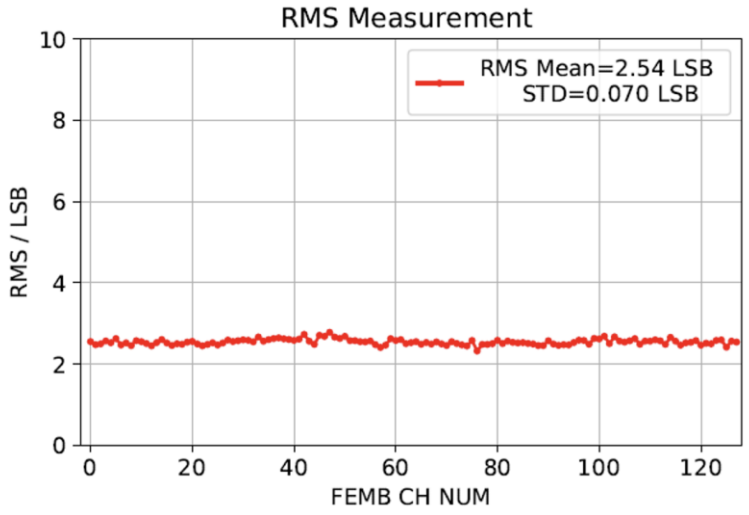


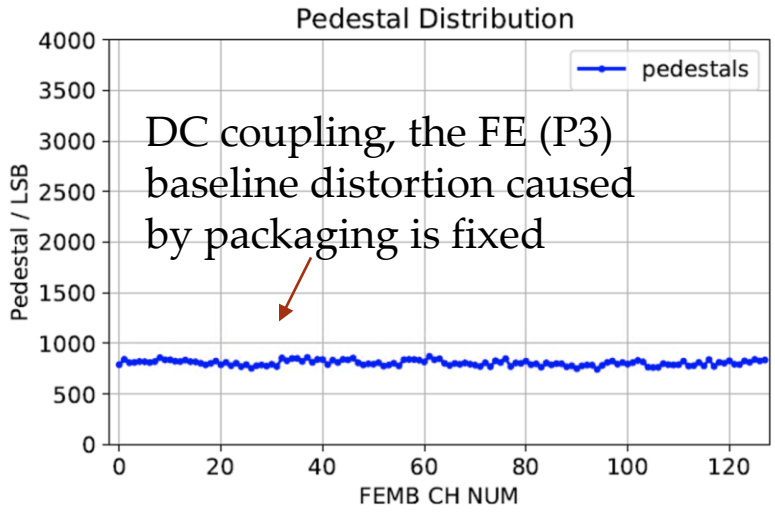


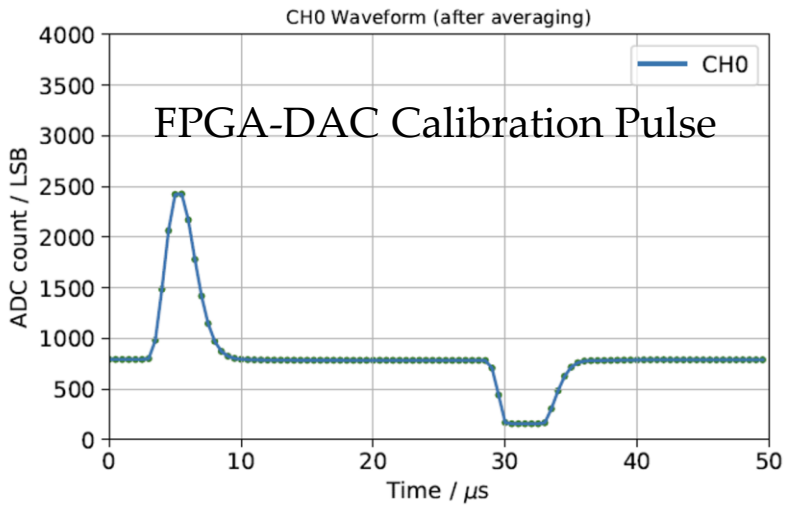
The checkout procedure takes < 1 minute

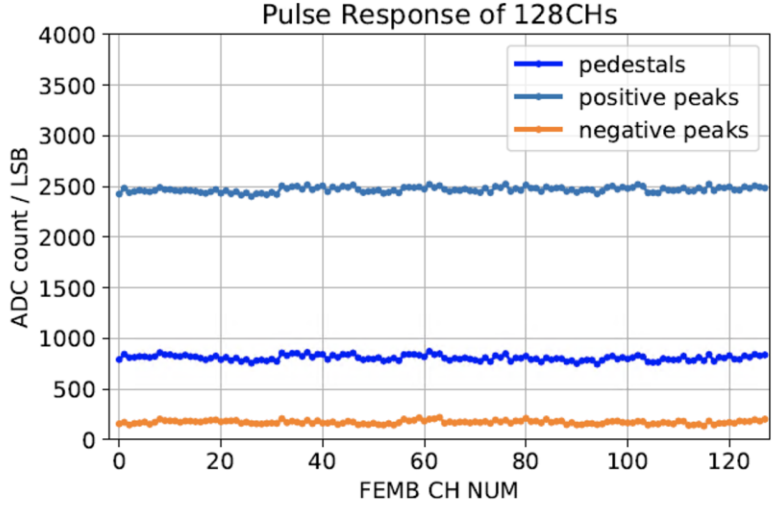
Checkout Result at LN2 Temperature

FE: 14mV/fC, 200mV BL, Tp 2.0μs

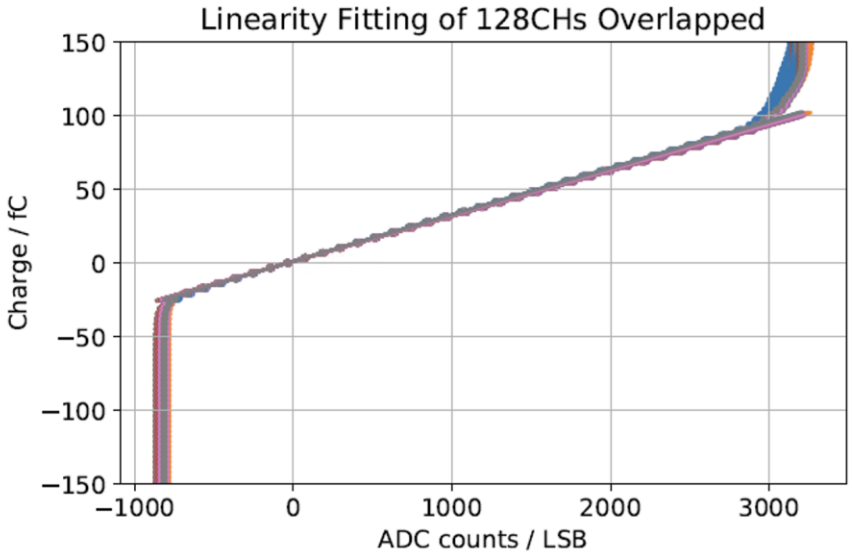


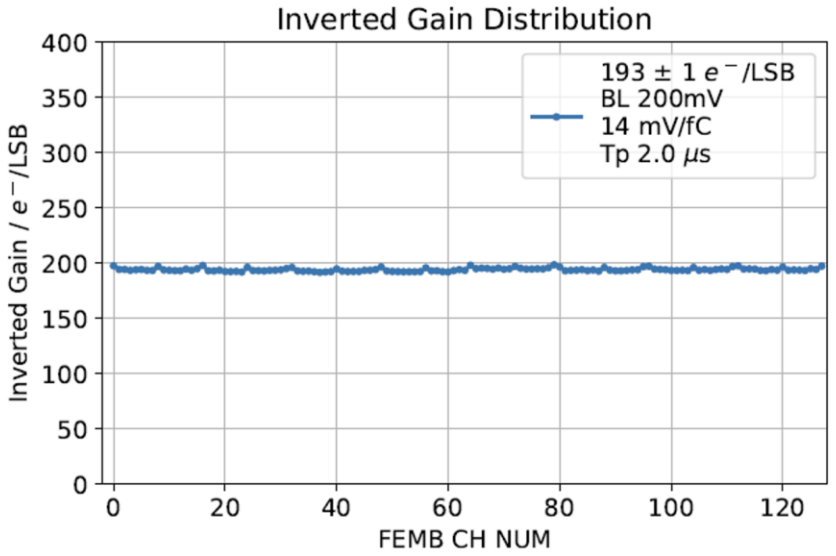


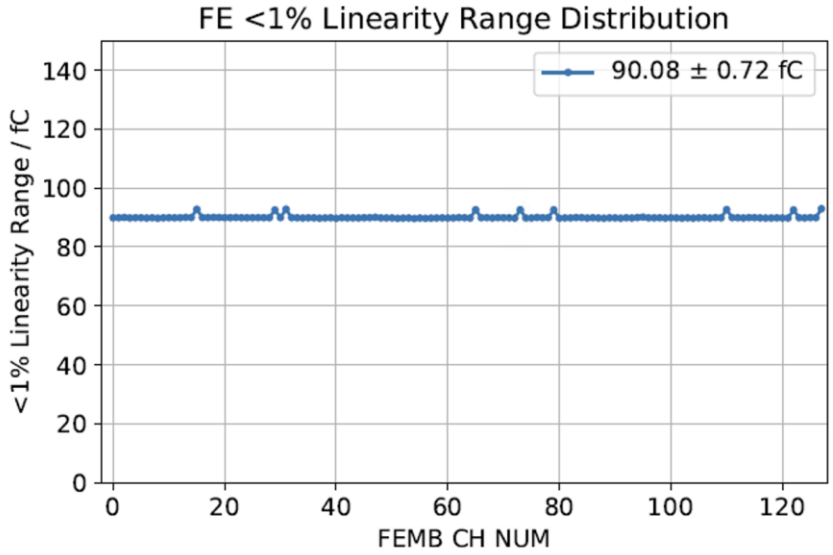


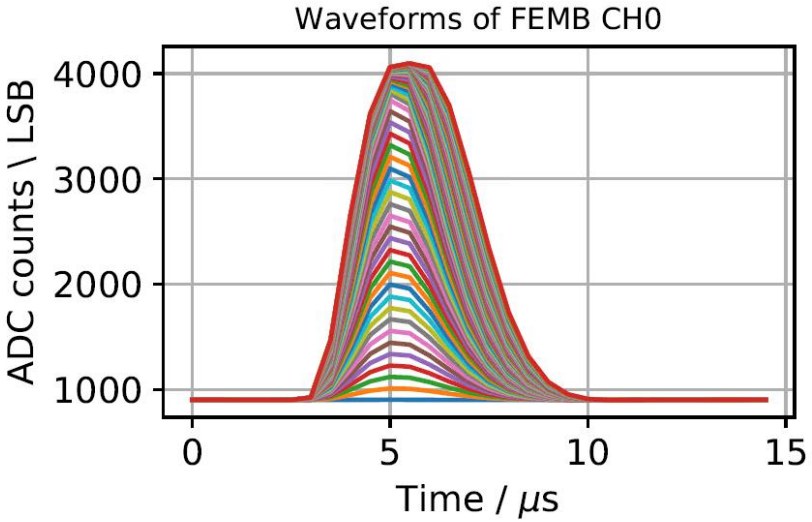


FEMB Performance Characterization at RT (1)

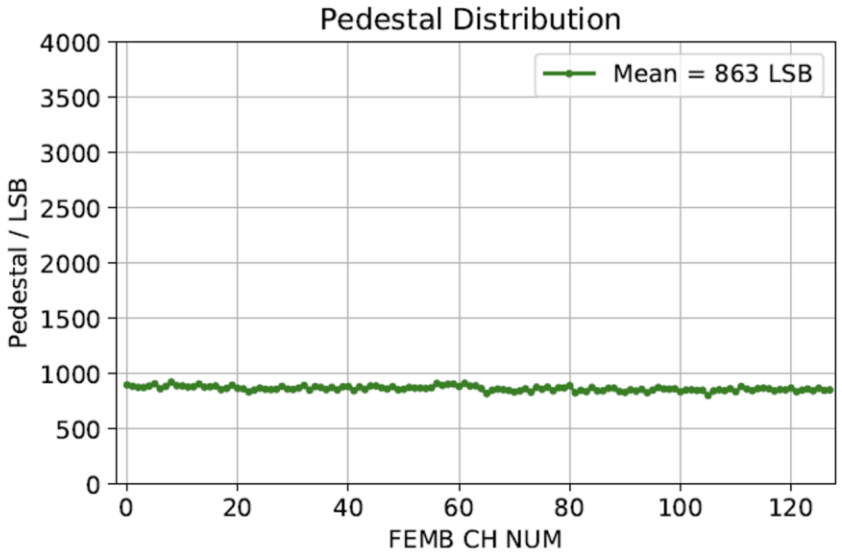


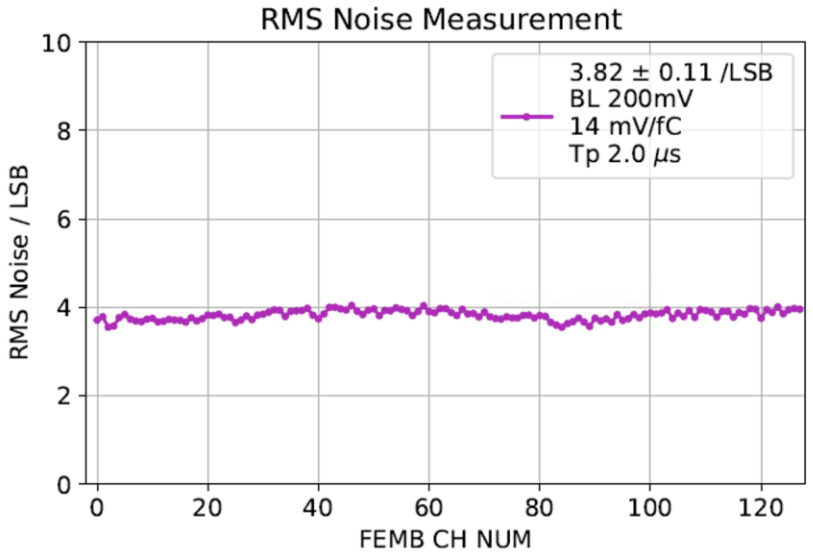


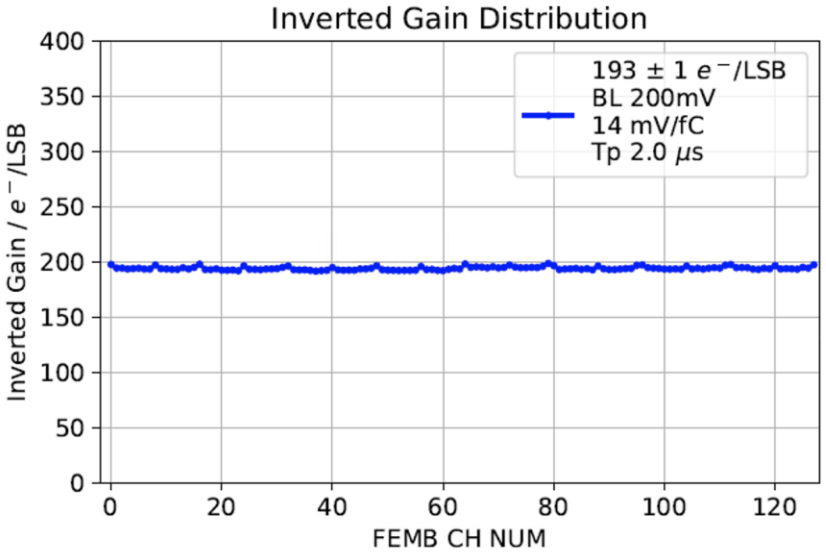


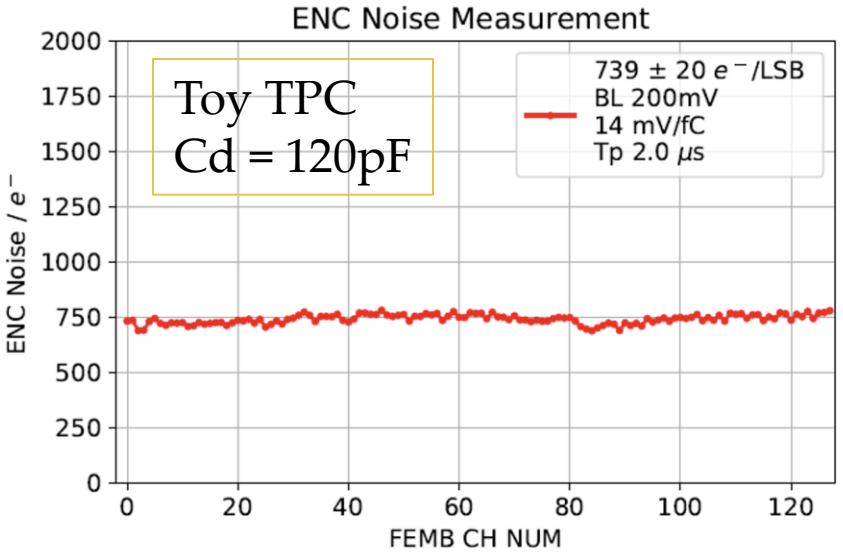


FEMB Performance Characterization at RT (3)

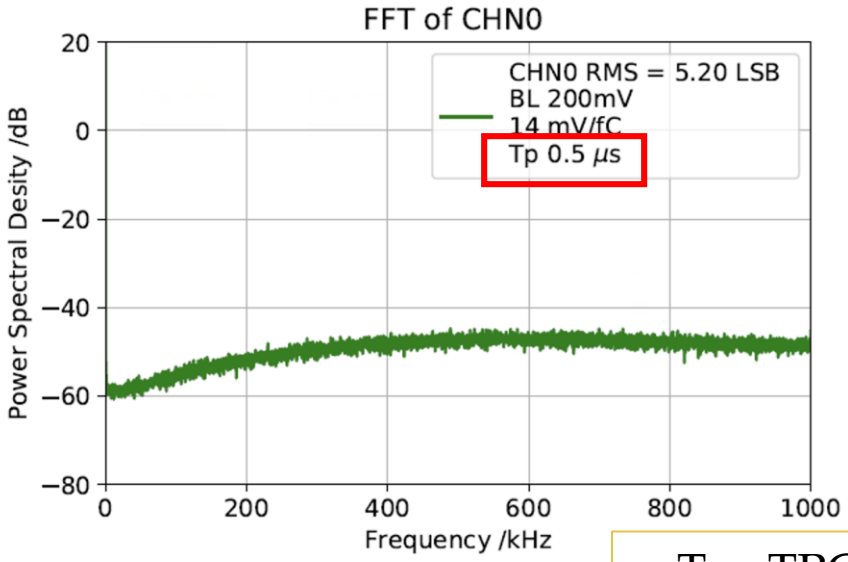


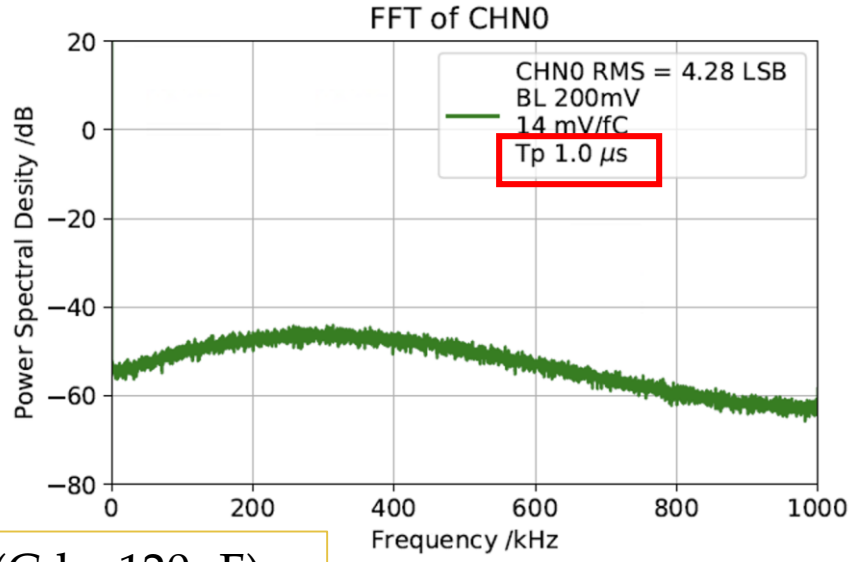




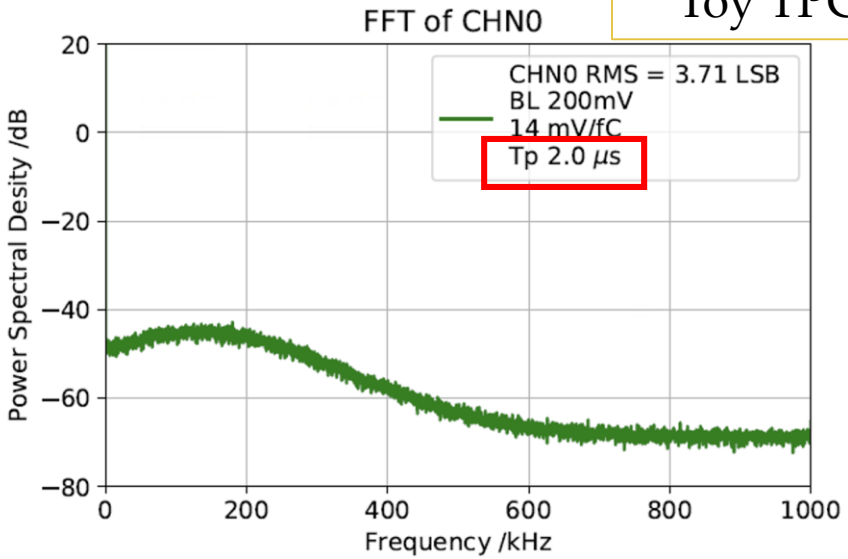


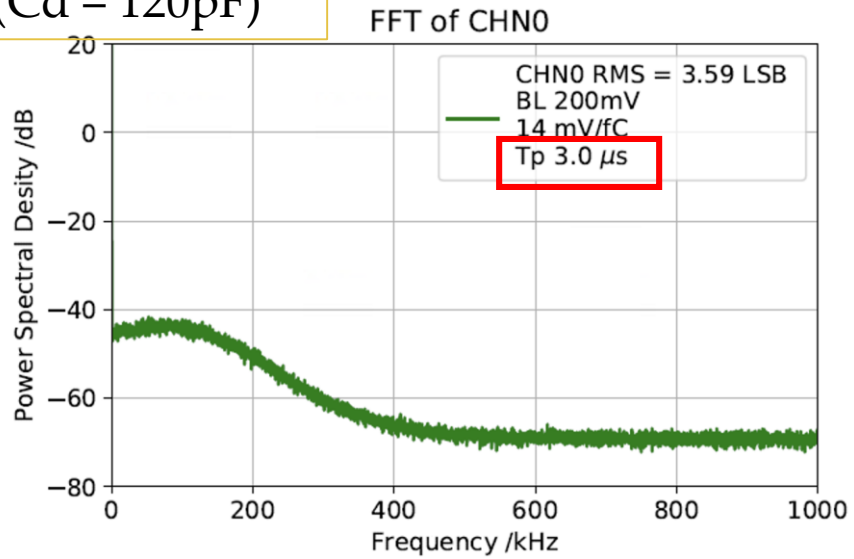
FEMB Performance Characterization at RT (4)



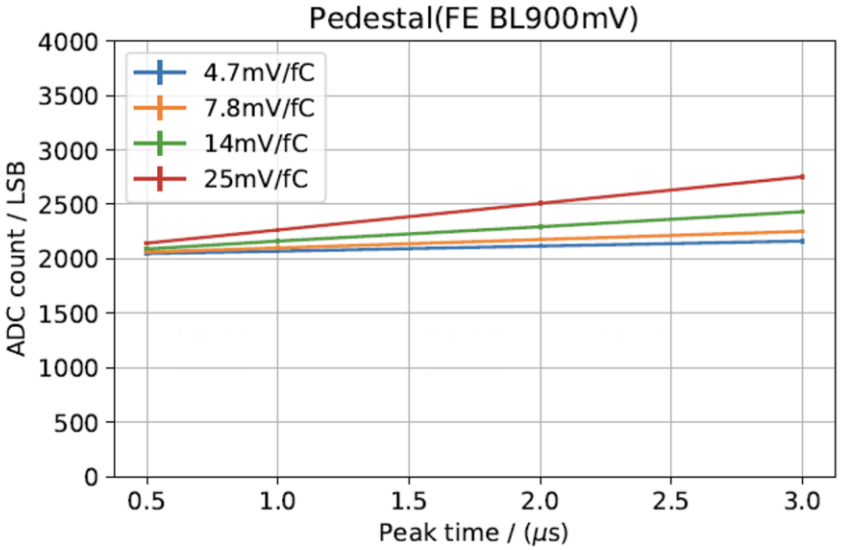


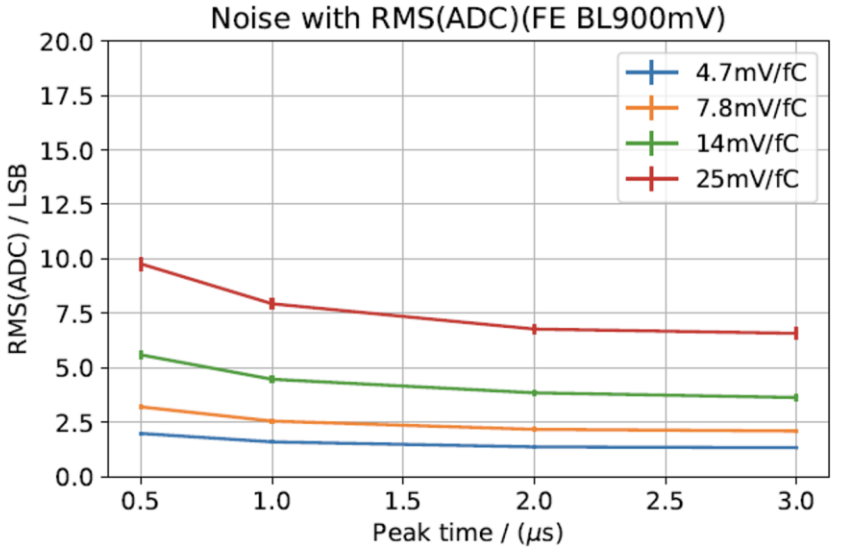
Toy TPC (Cd = 120pF)

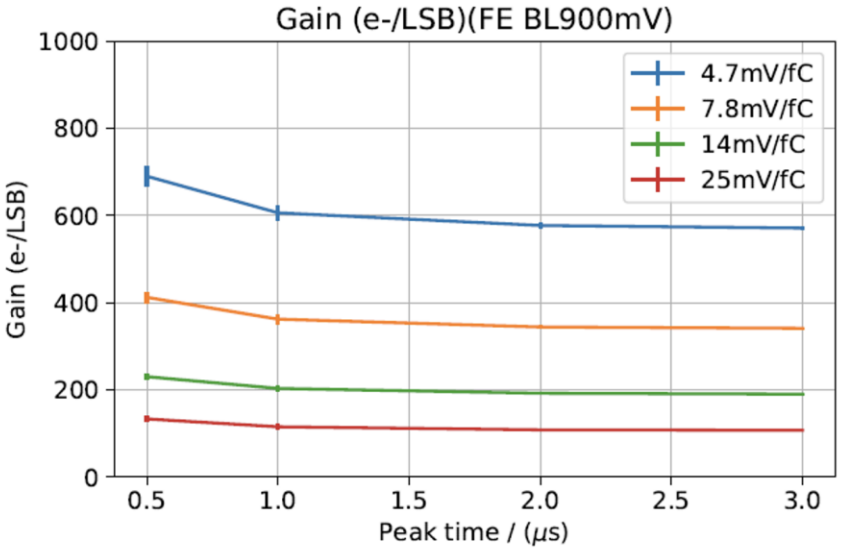


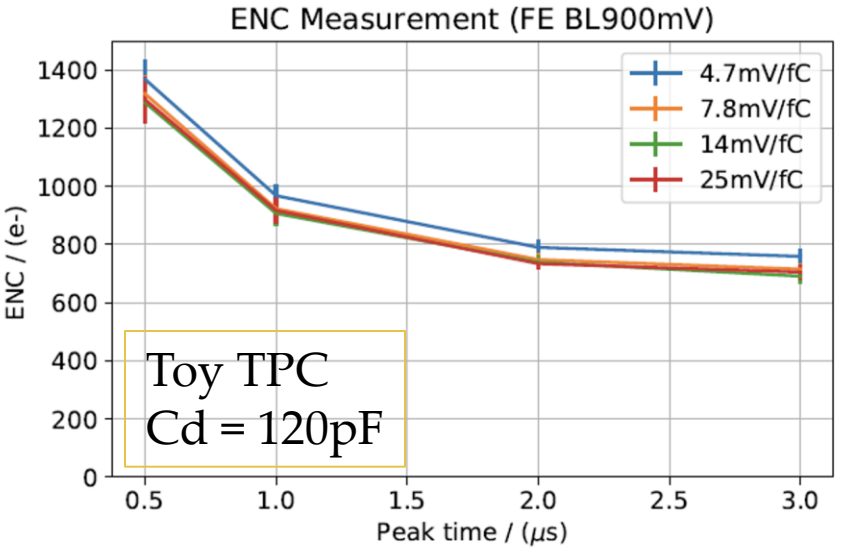


FEMB Performance Characterization at RT (5)

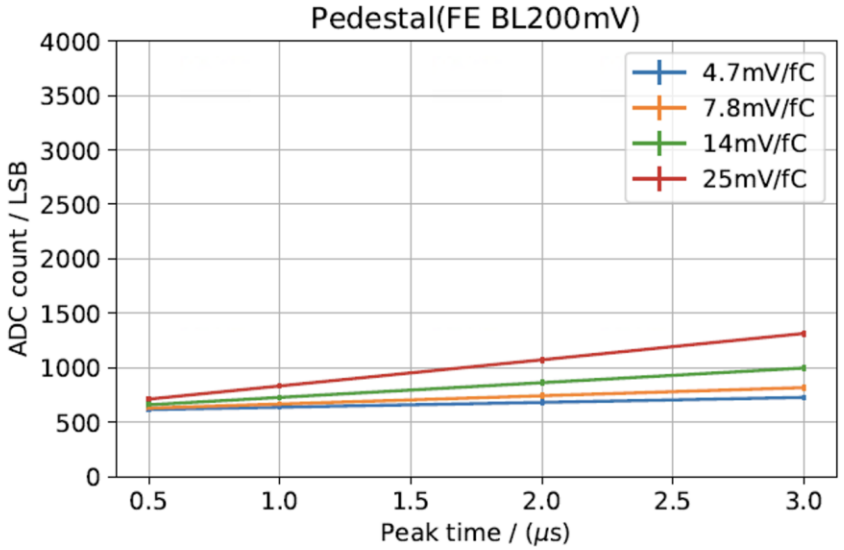


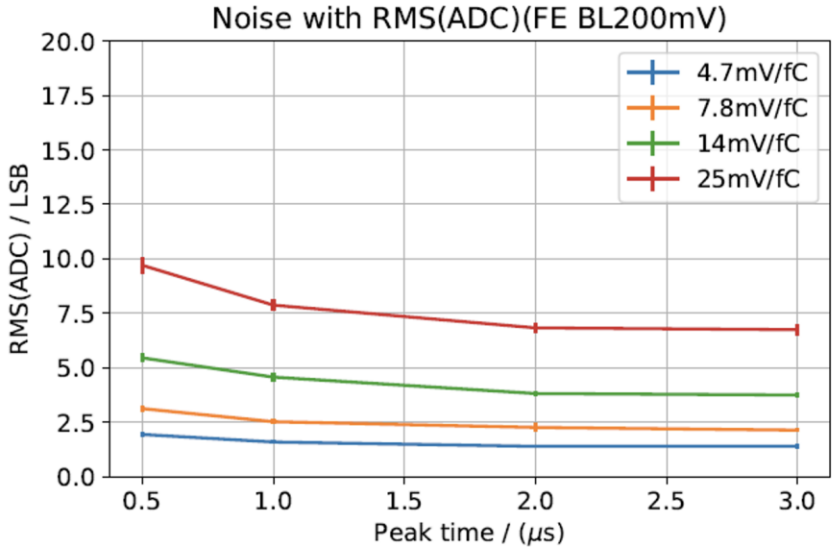


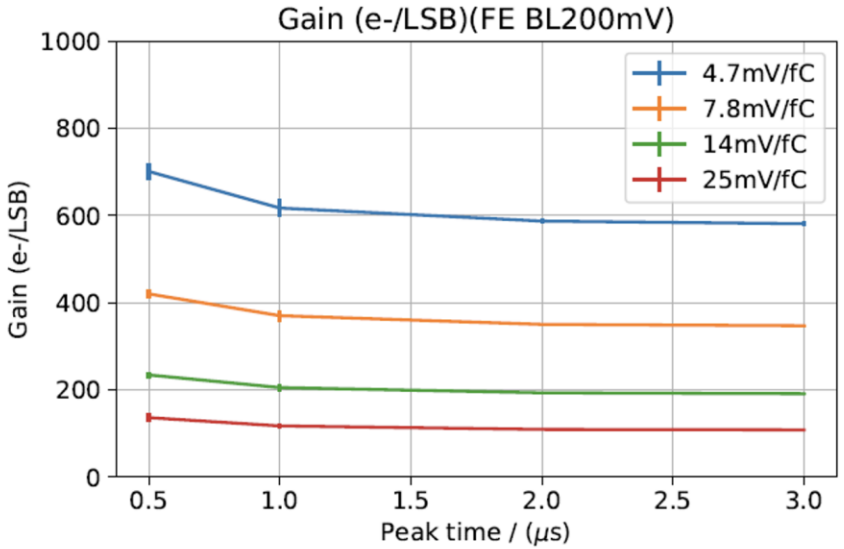


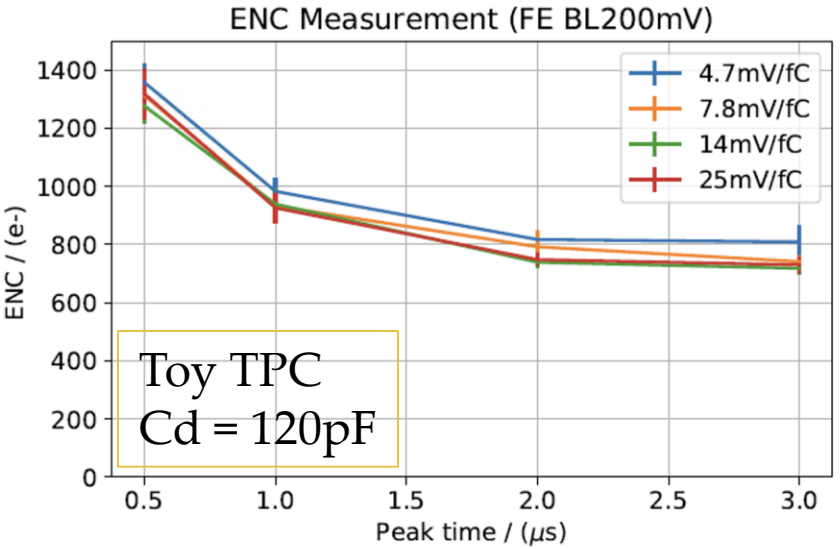


FEMB Performance Characterization at RT (6)

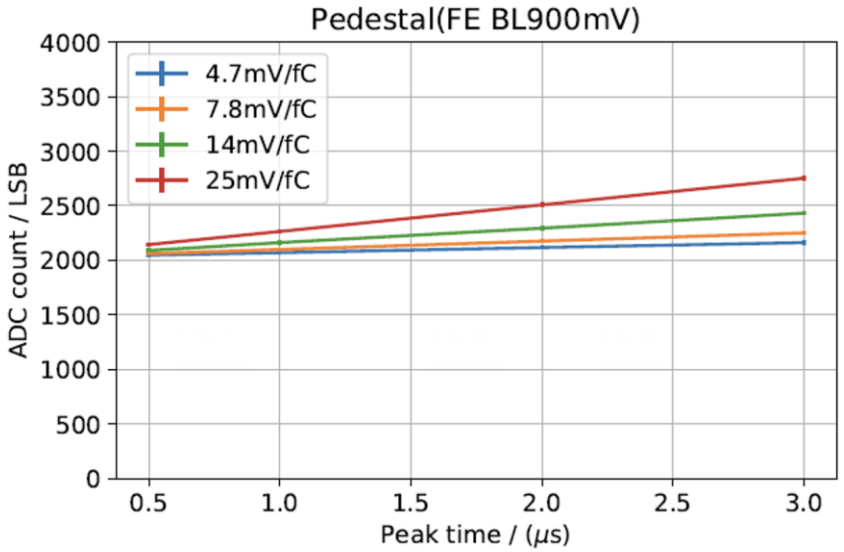


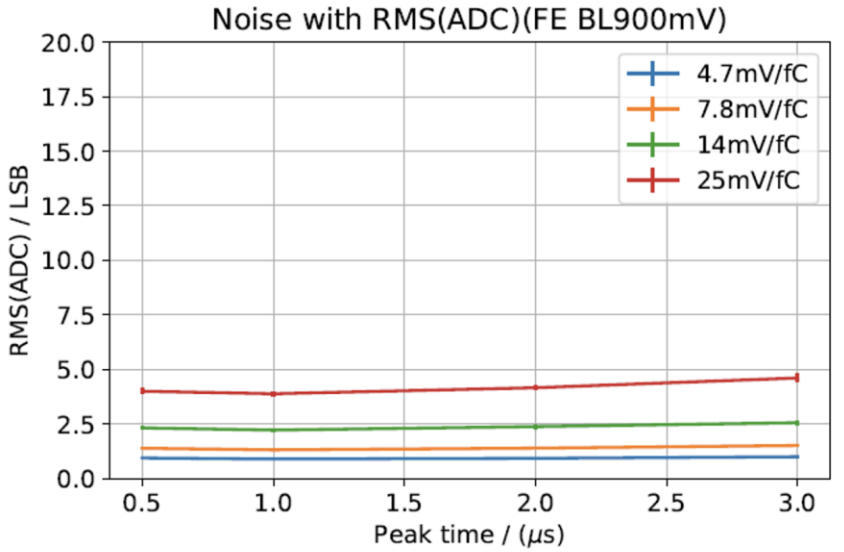


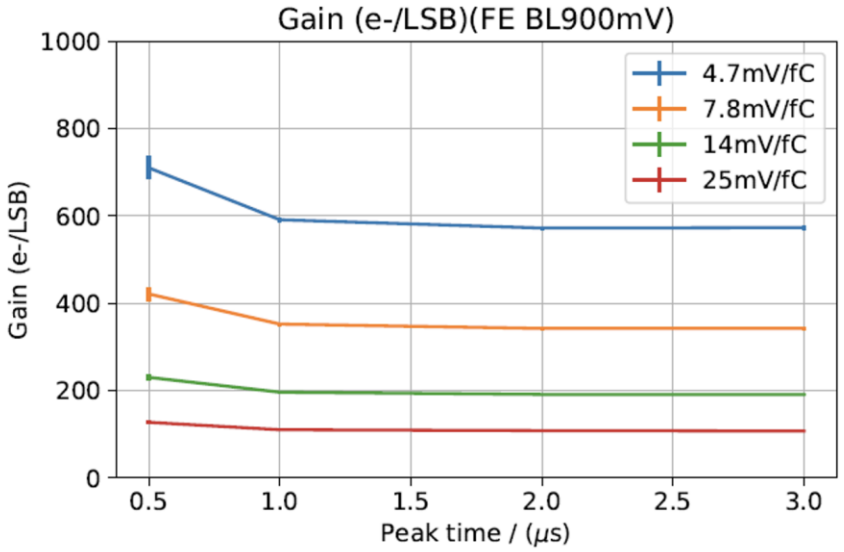


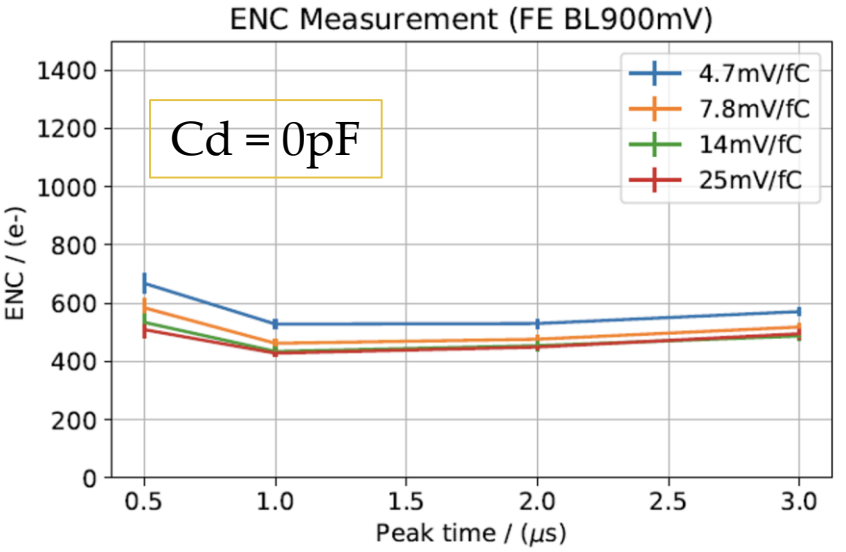


FEMB Performance Characterization at RT (7)

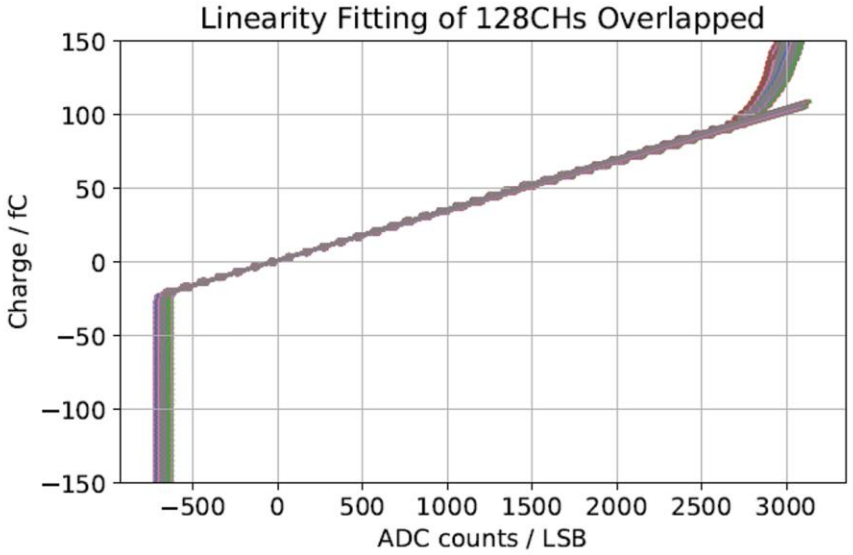


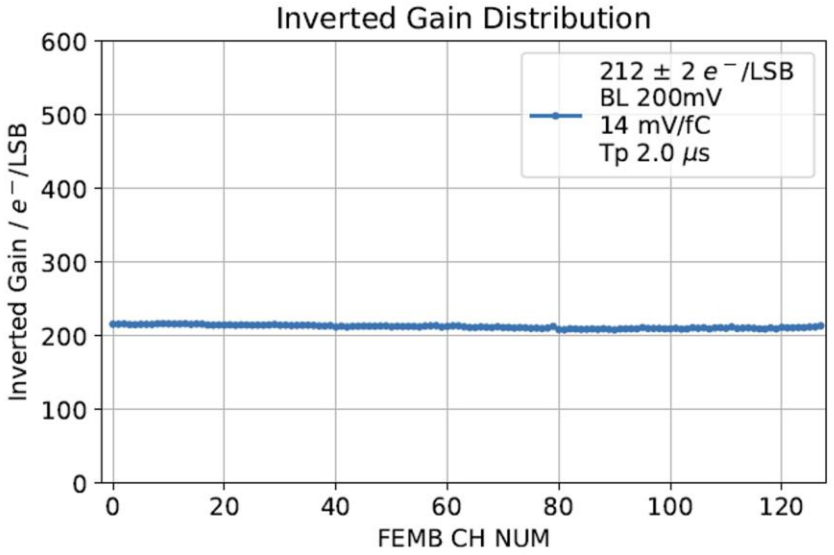


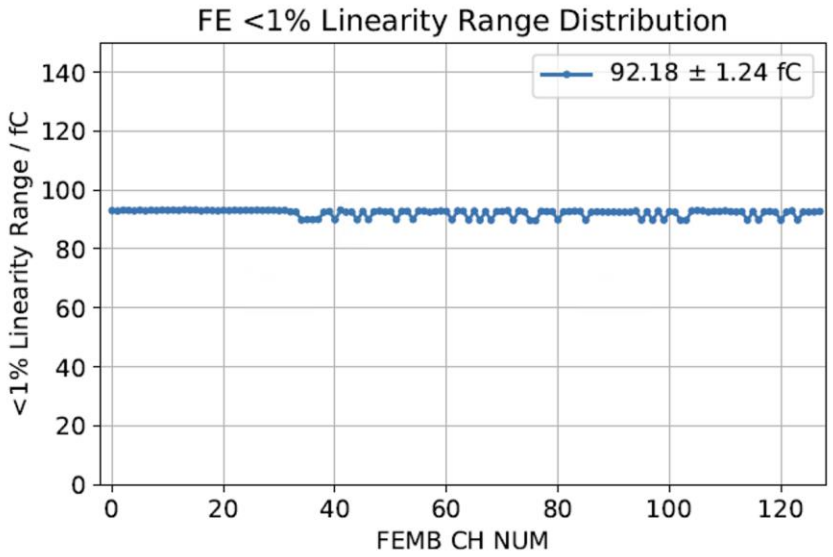


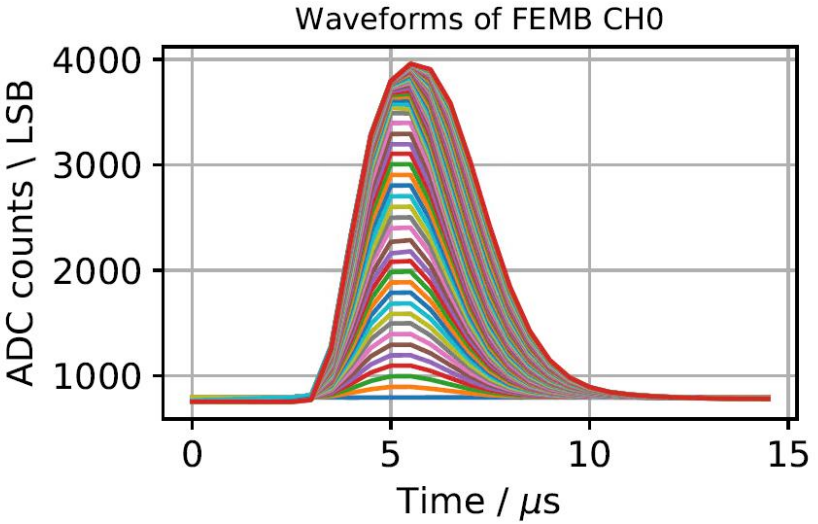


FEMB Performance Characterization at LN2 (1)

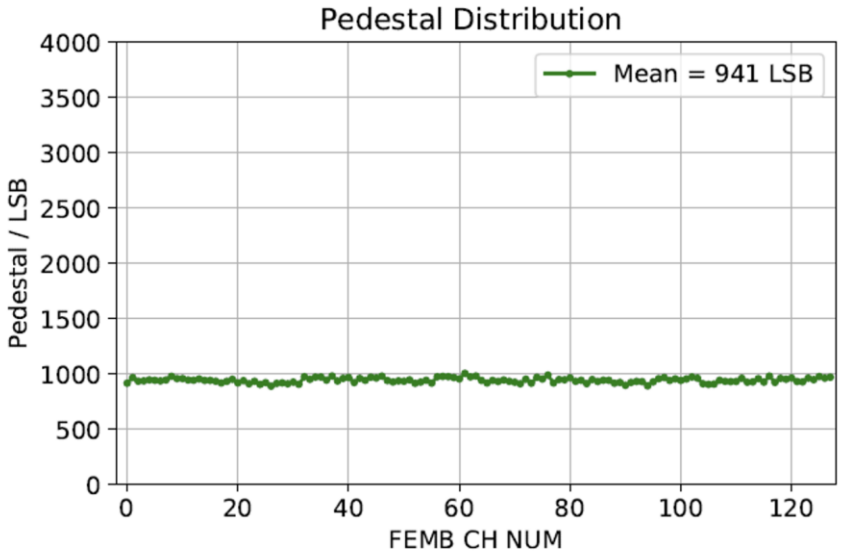


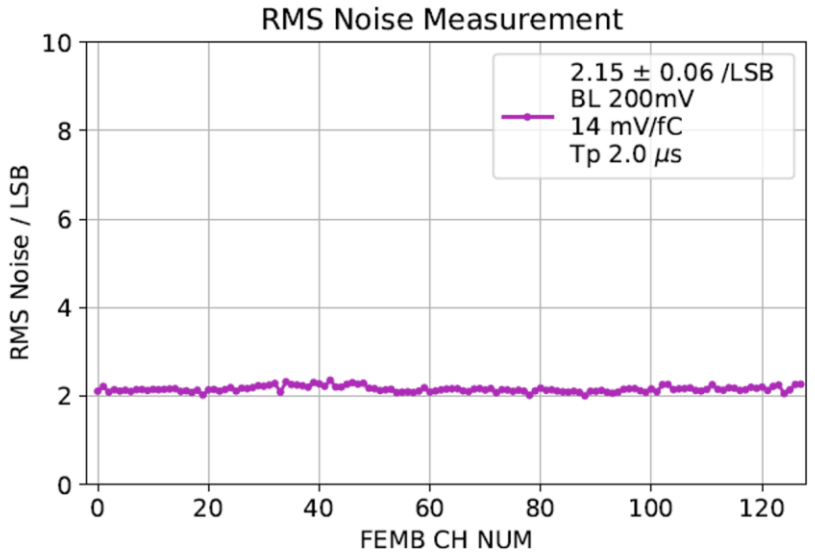


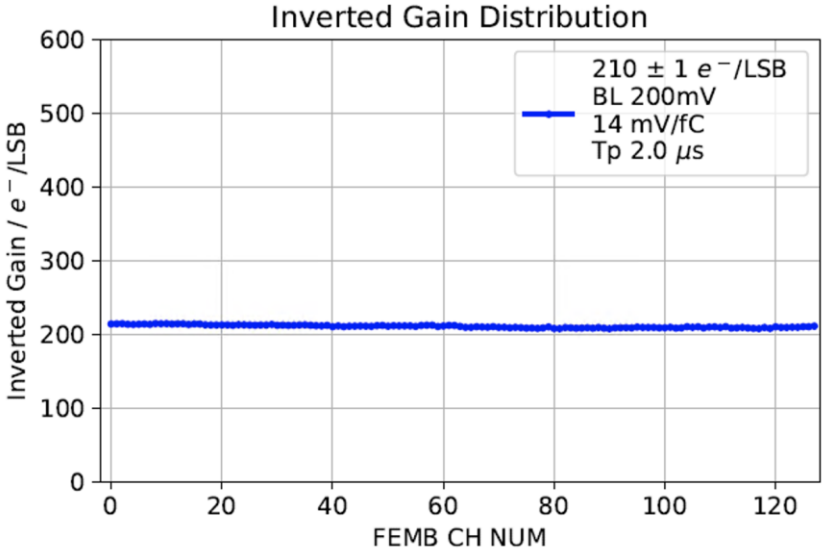


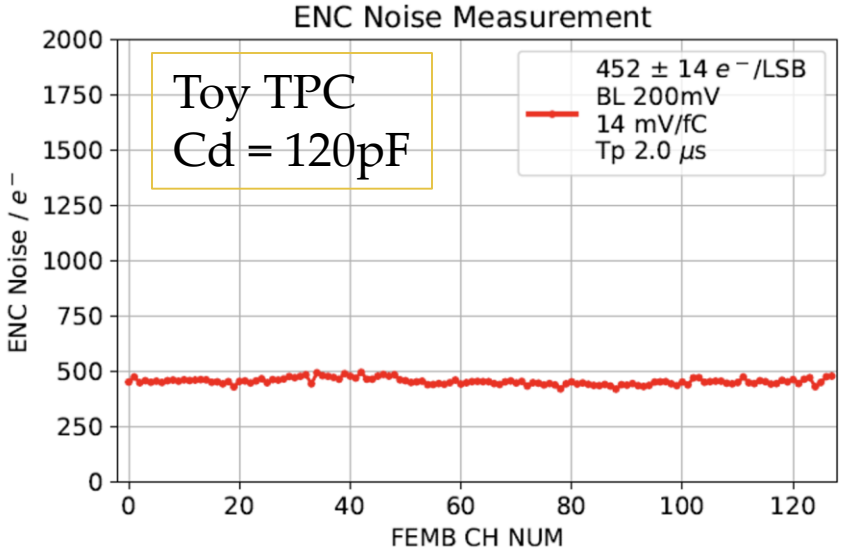


FEMB Performance Characterization at LN2 (3)

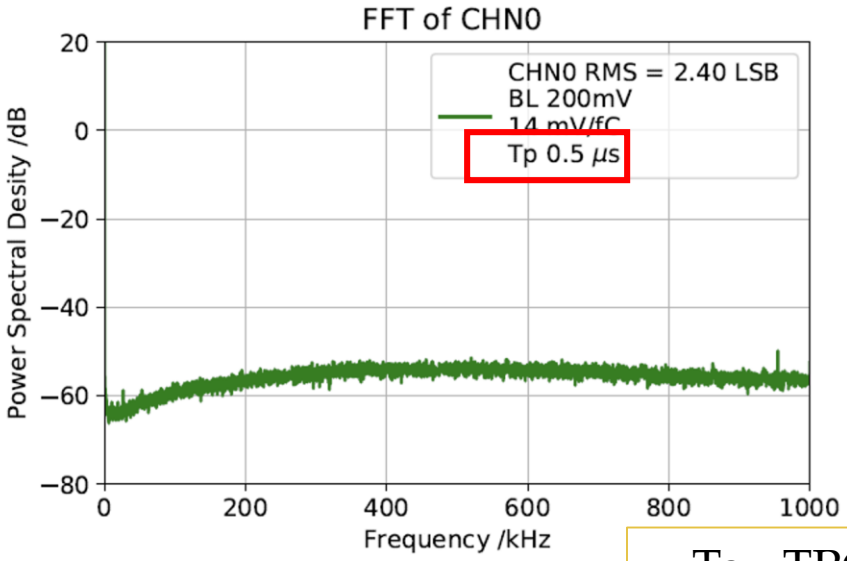


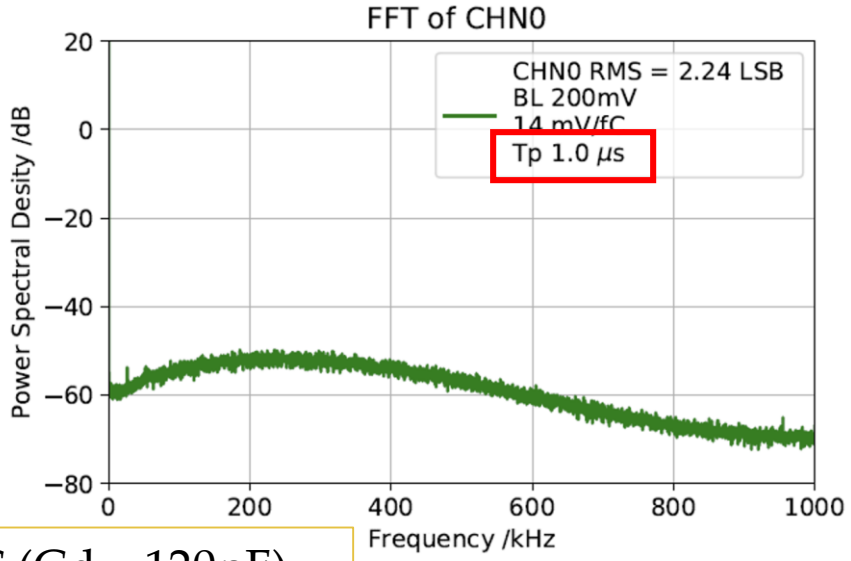




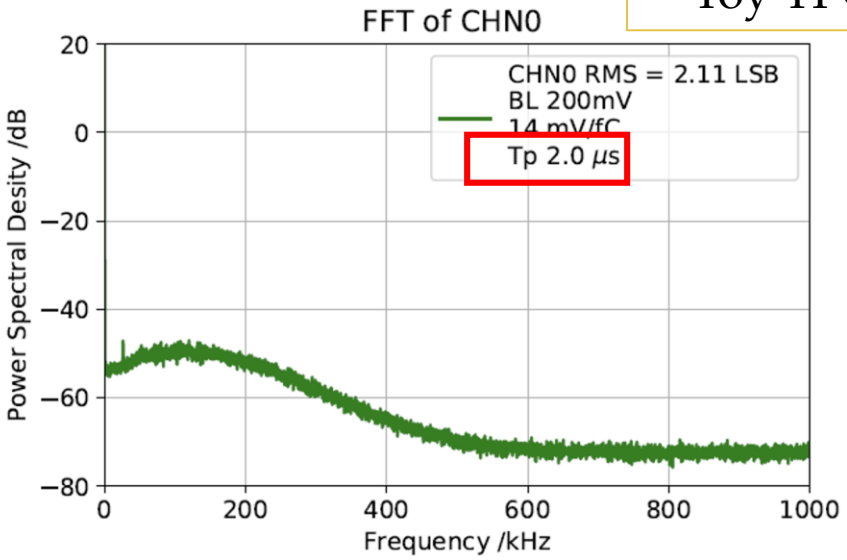


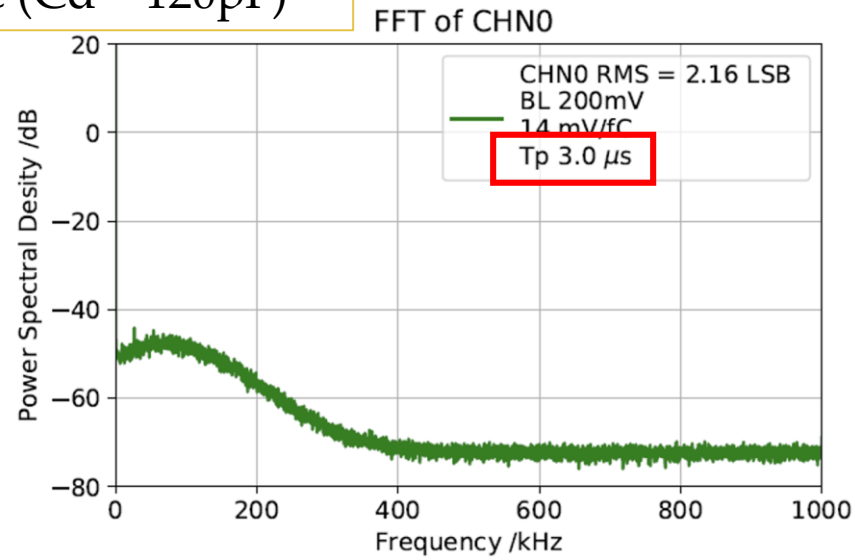
FEMB Performance Characterization at LN2 (4)



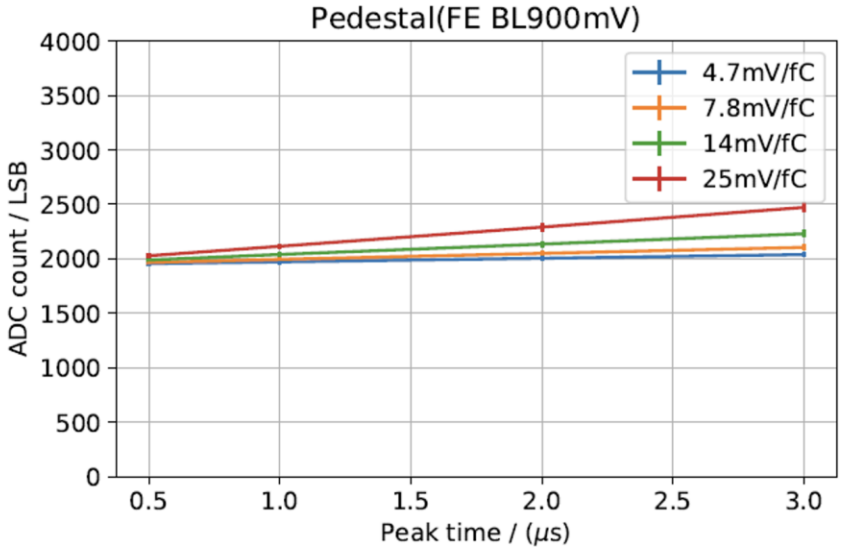


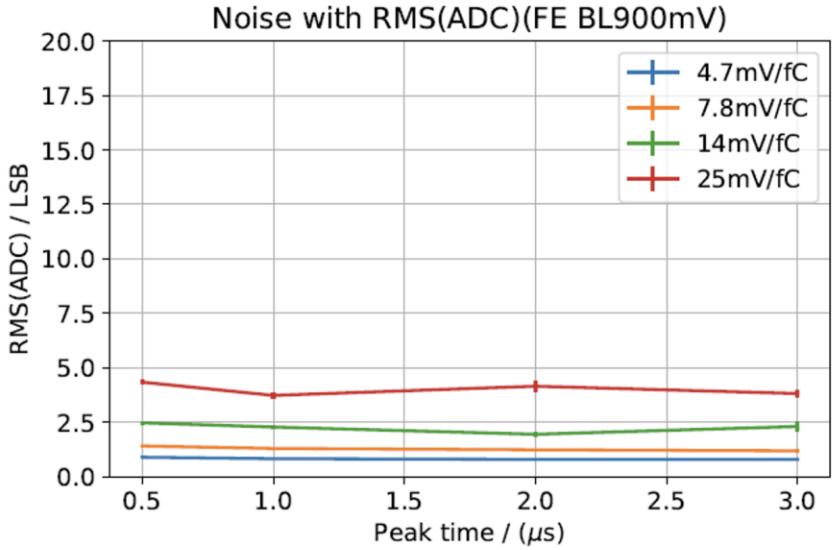
Toy TPC (Cd = 120pF)

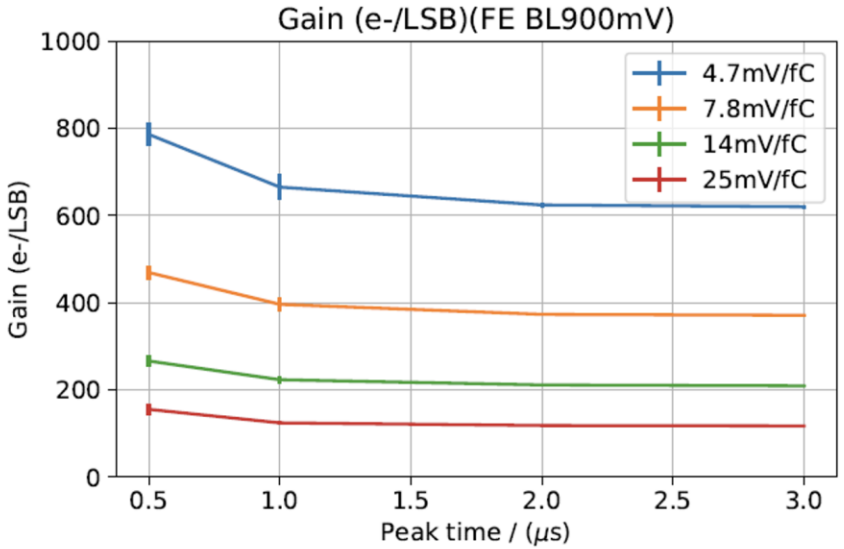


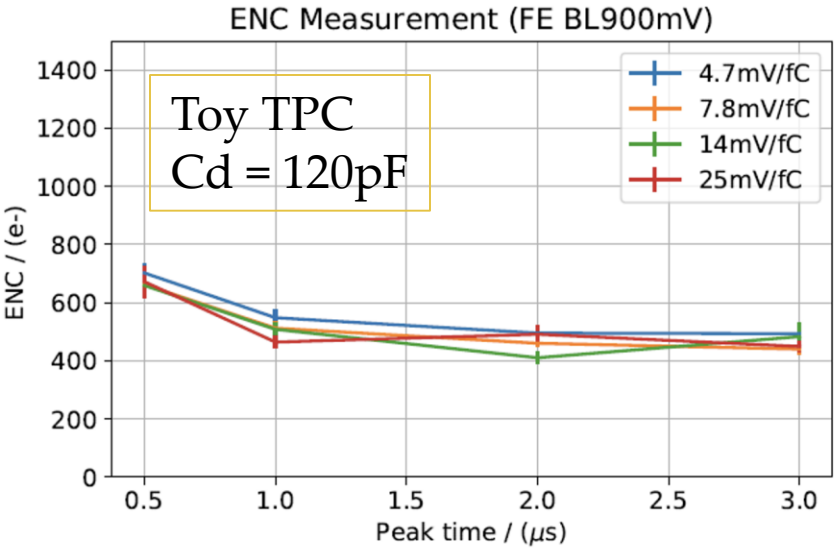


FEMB Performance Characterization at LN2 (5)

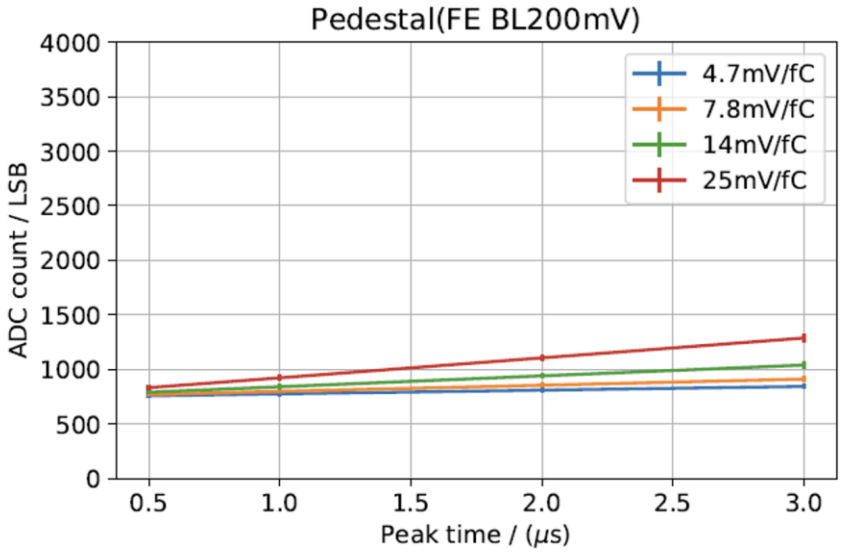


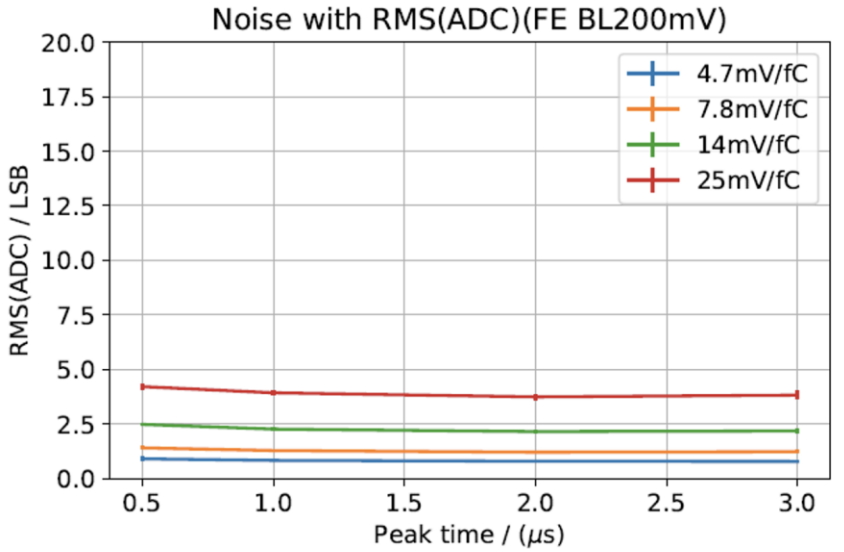


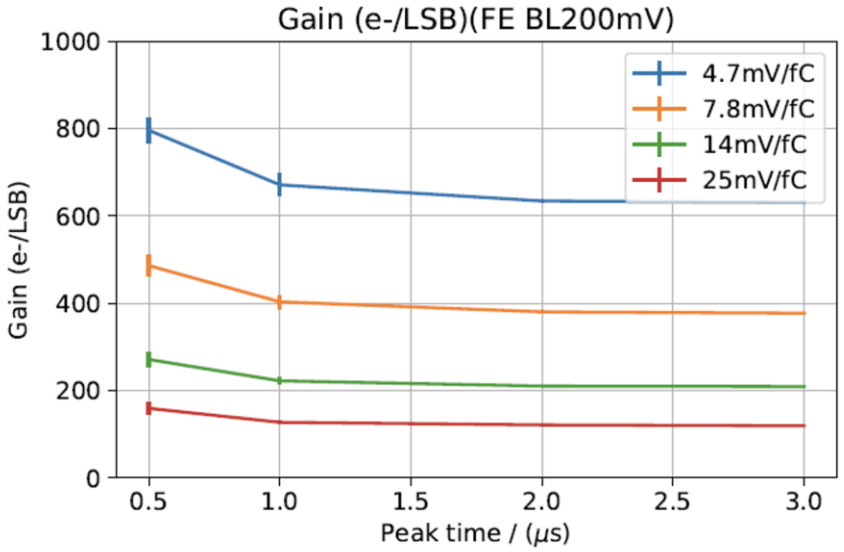


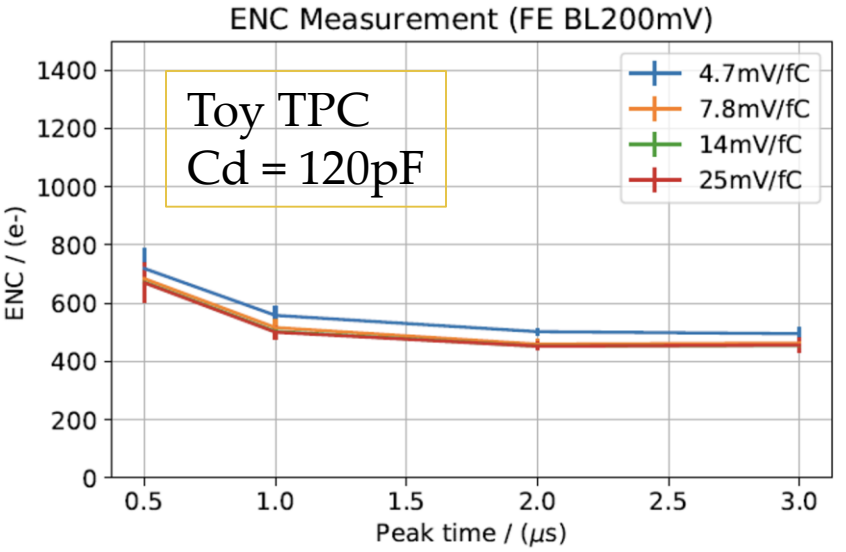


FEMB Performance Characterization at LN2 (6)

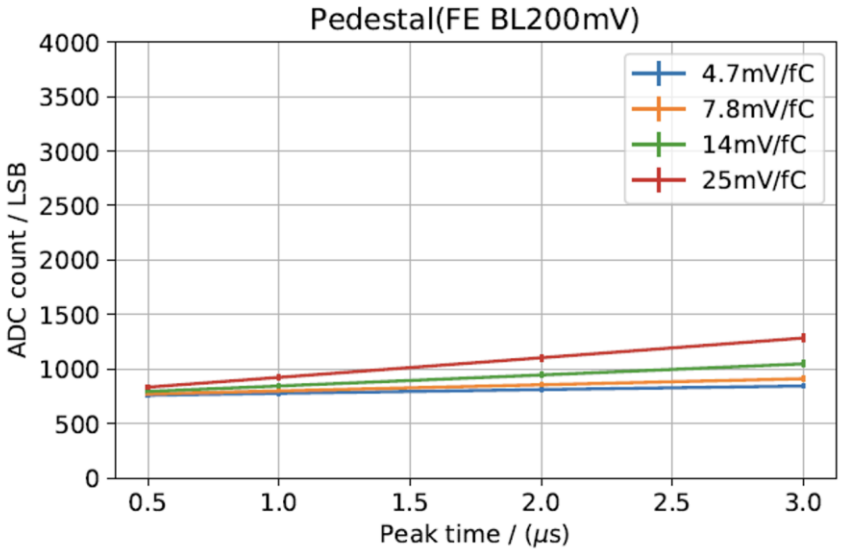


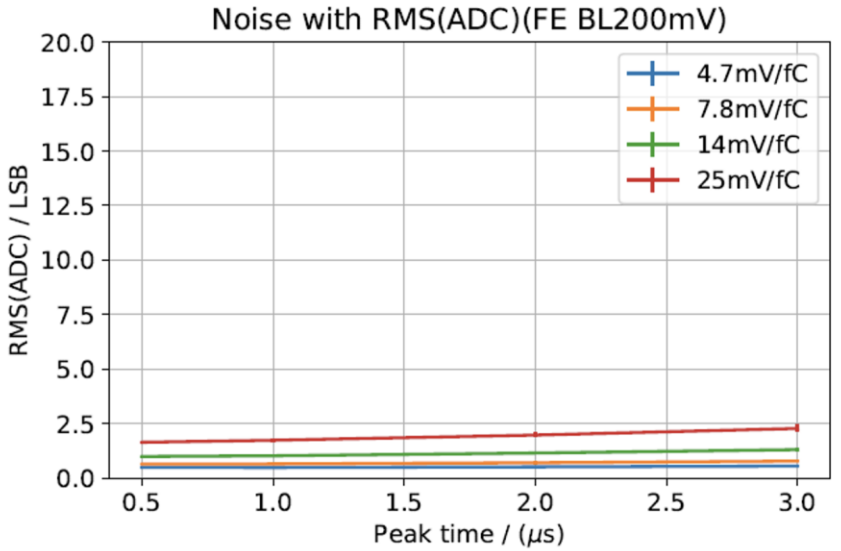


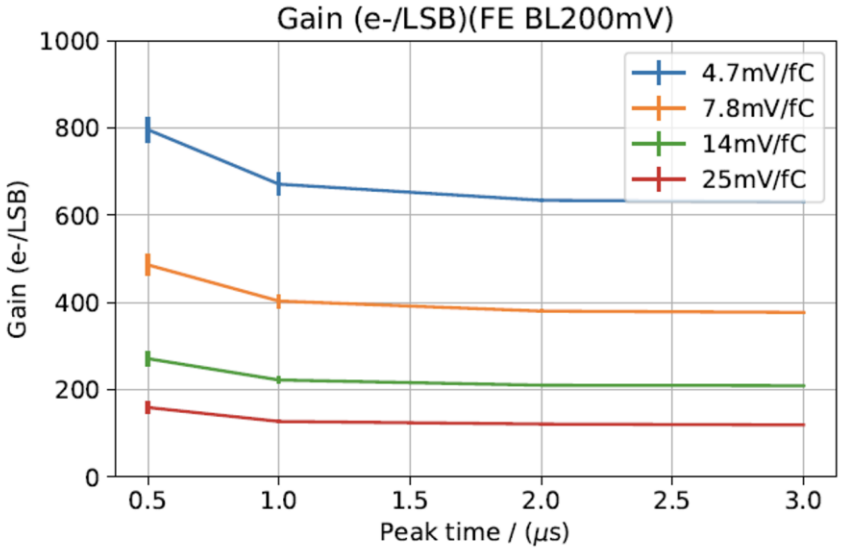


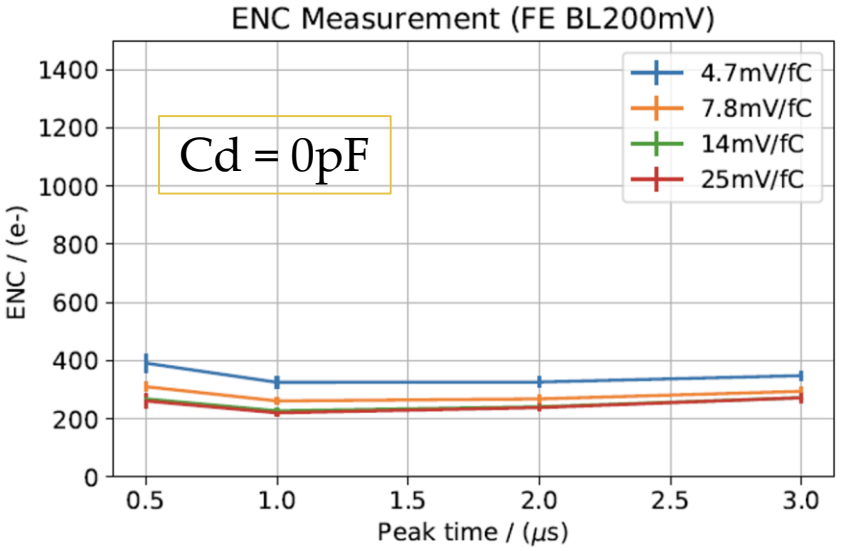


FEMB Performance Characterization at LN2 (7)



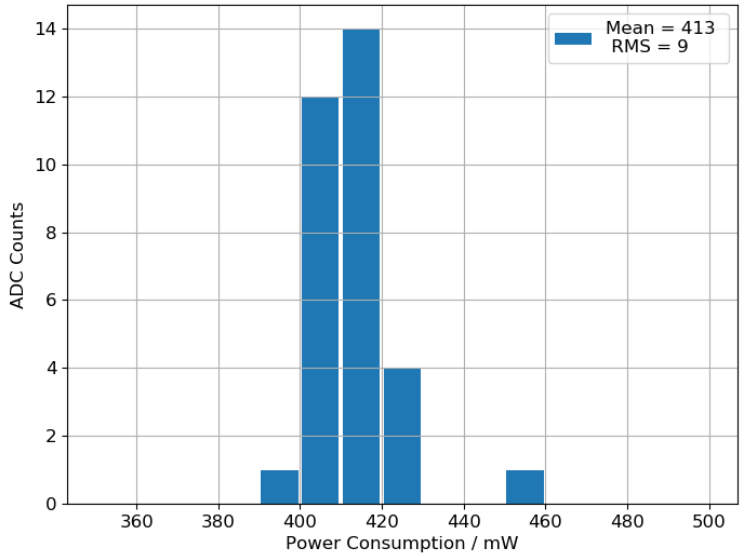


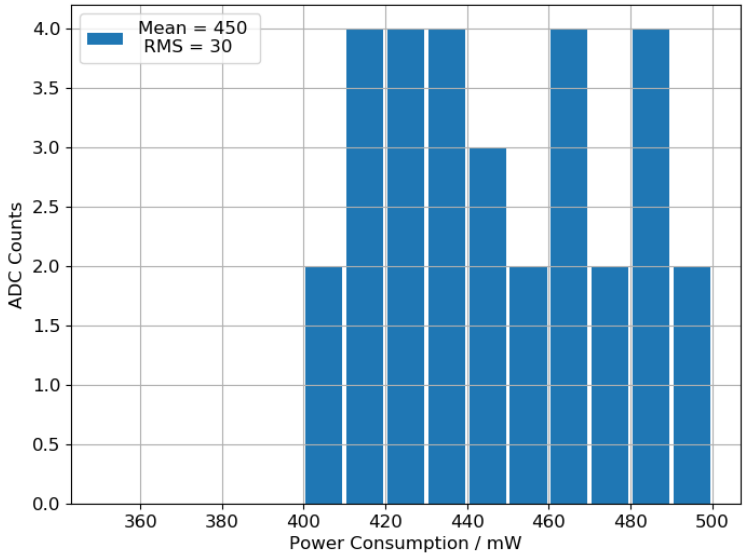




ColdADC QC Statistics (Preliminary)

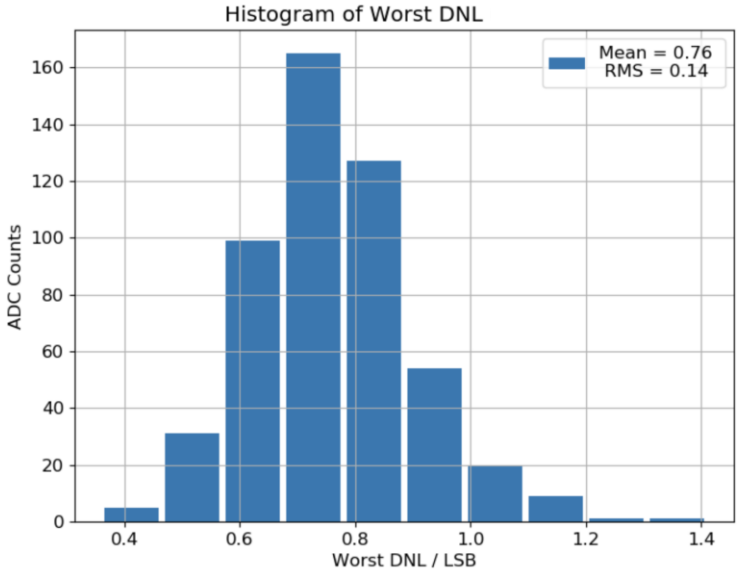
- 33 pcs of ColdADC chips have gone through QC test
  - 31 pcs passed QC
  - 1 pcs (Chip#00096) draws high current (>1A) both at RT and LN2
    - Low resistance between VDDA2P5 and GND
  - 1 pcs (CHIP#00069) requires a re-test at LN2
    - Poor connection between a pin of ColdADC and ASIC socket for CH8

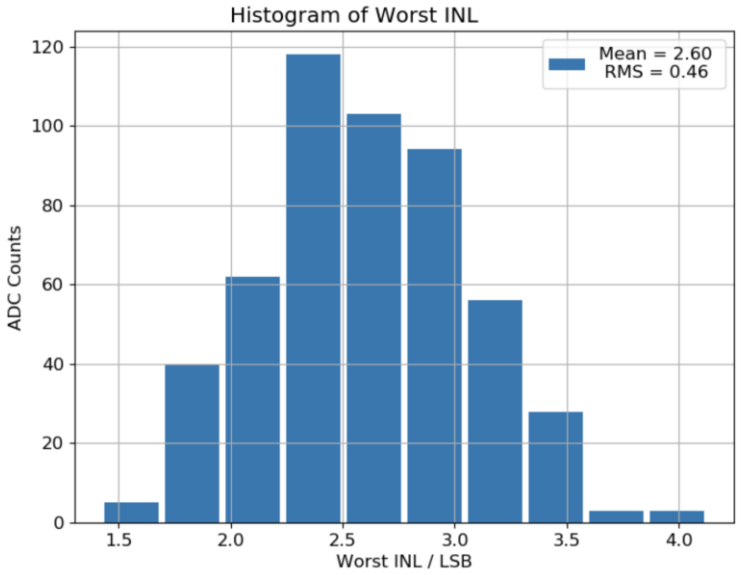


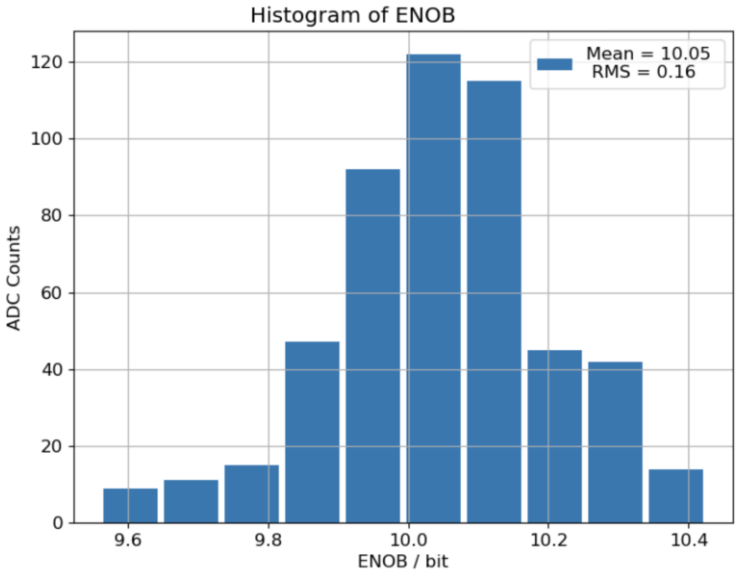


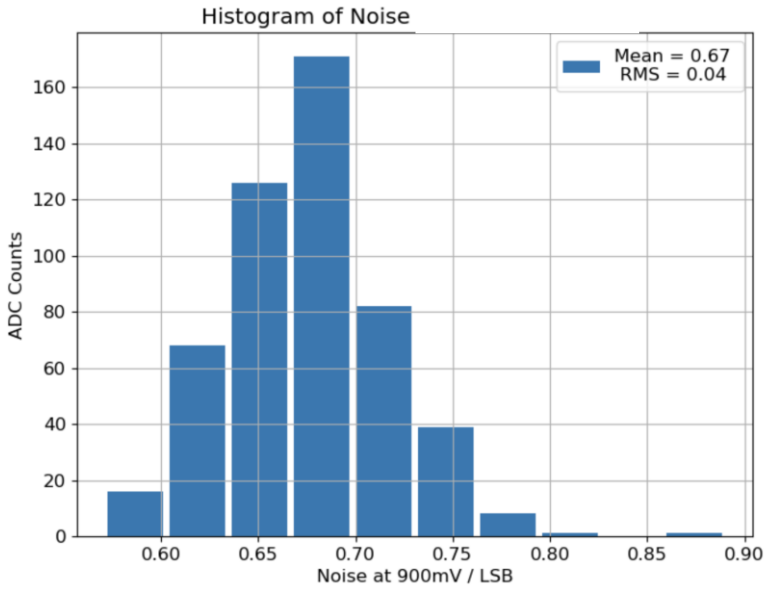
Power consumption at cold is ~40mW higher than warm in average
(CMOS Reference, SDC&DB bypassed, single-ended inputs)

ColdADC QC Preliminary Status (32pcs, RT, 2MS/s)



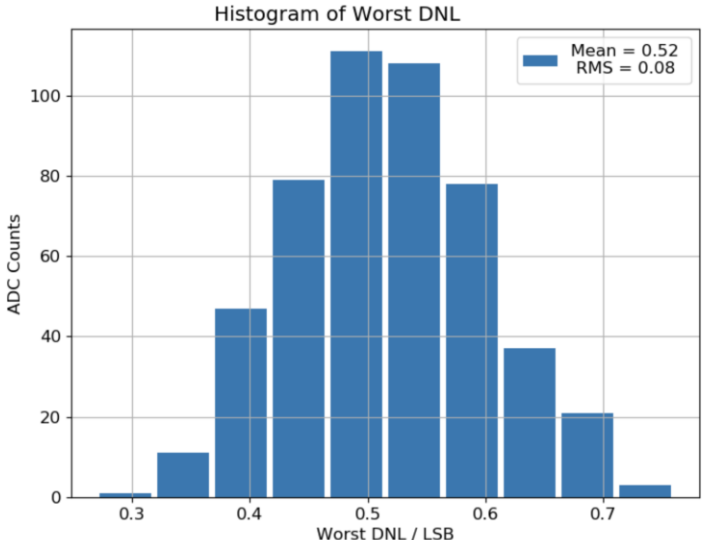


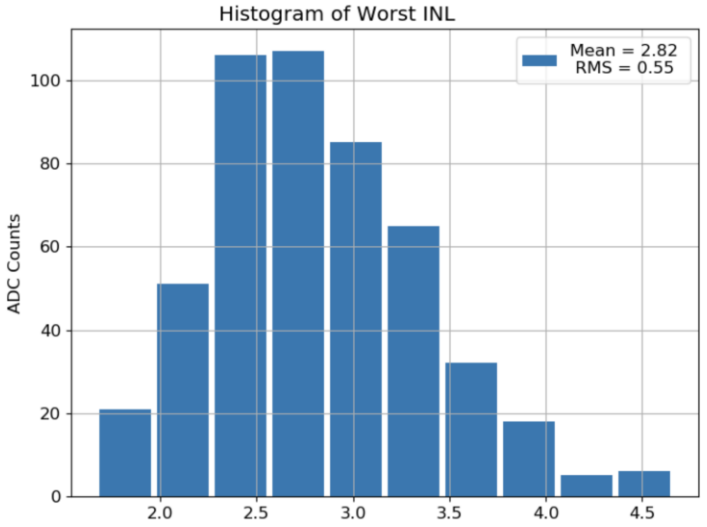


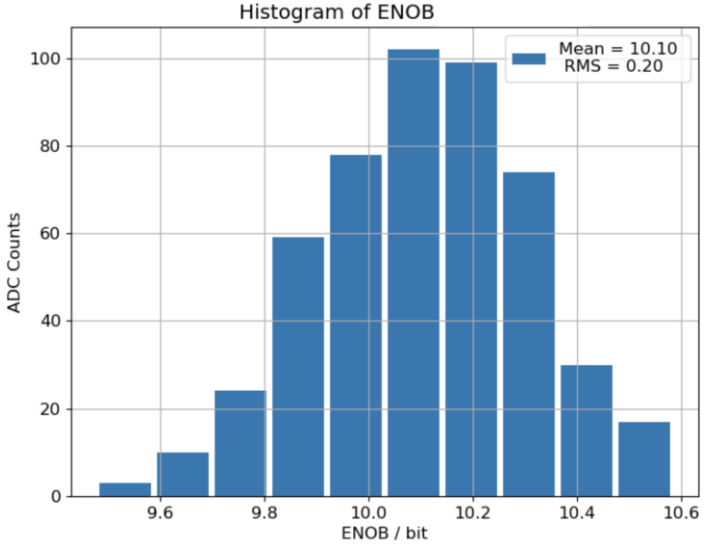


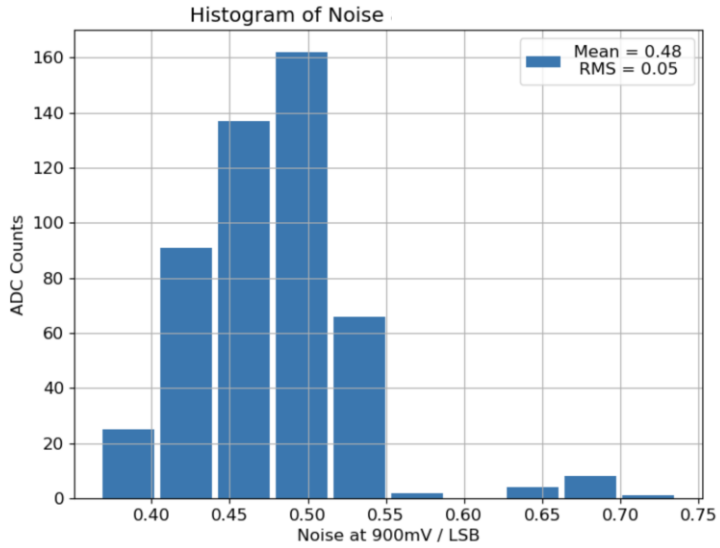
ColdADC QC Preliminary Status (31pcs, LN2, 2MS/s)

CHIP#00069 may have poor connection with socket at LN2









Summary

- "LArASIC + ColdADC + FPGA" FEMB is evaluated at BNL with expected performance
  - 14mV/fC, Tp 2.0us: **ENC = ~450 e- with 120pC at LN2**
  - LArASIC P3 doesn't show baseline distortion caused by packaging
    - ProtoDUNE uses LArASIC P2
  - Performance of ColdADC is comparable with COTS ADC used in SBND
    - Power consumption is higher, but FE buffer can be off
- QC test of ColdADC shows good results
  - Uniform performance, high yield at both RT and LN2

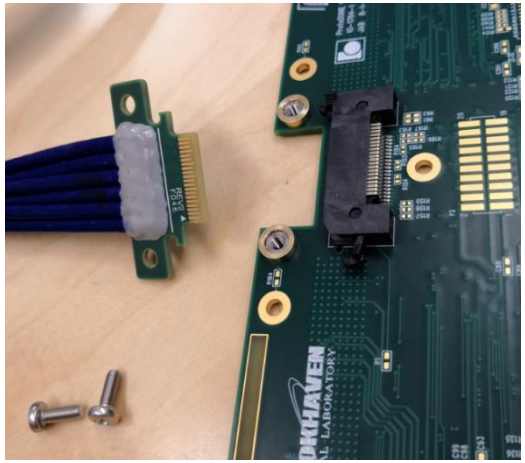
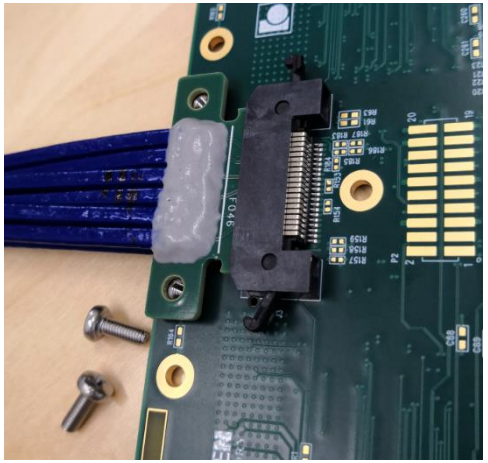
To Do List

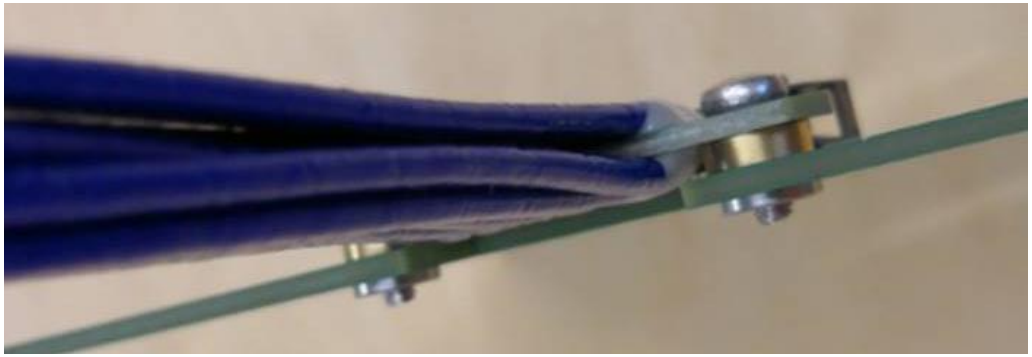
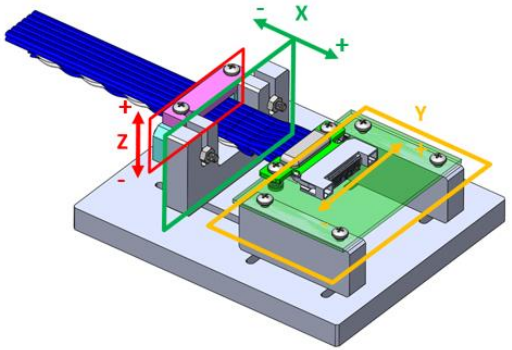
- FEMB optimization and characterization
  - ColdADC manual calibration
    - FW have supported read 8 channels (per ADC core) out simultaneously
  - Implement ASIC-DAC calibration (python script)
  - Implement FE monitoring (python script)
  - Firmware optimization
  - Integration test with 40%APA
- Revision plan
  - Minor updates on AM
    - If single-end inputs of ColdADC is in use, the other unused ends (N) should be terminated to ground through 50 Ohm (currently floating)
    - VDDA2P5, VDDD2P5, VDDD1P2, VDDIO should be powered by different regulators which can be controlled by FPGA independently
      - To allow the power on sequence wrt the ColdADC datasheet to avoid potential unexpected large current
  - Minor updates on FM
    - Layout optimization
      - FPGA-DAC should be repositioned further away from LArASIC

Backup

Cold Data Cable with 2 Tabs

- Improved cold data cable with 2 tabs for reliable mounting

Done by Manhong Zhao at BNL: Redesigned connection between the cold control/data cable and the FPGA mezzanine board has been verified by mechanical fit check and temperature cycling tests and liquid nitrogen immerse tests.