protoDUNE-SP Cold Electronics Calibration

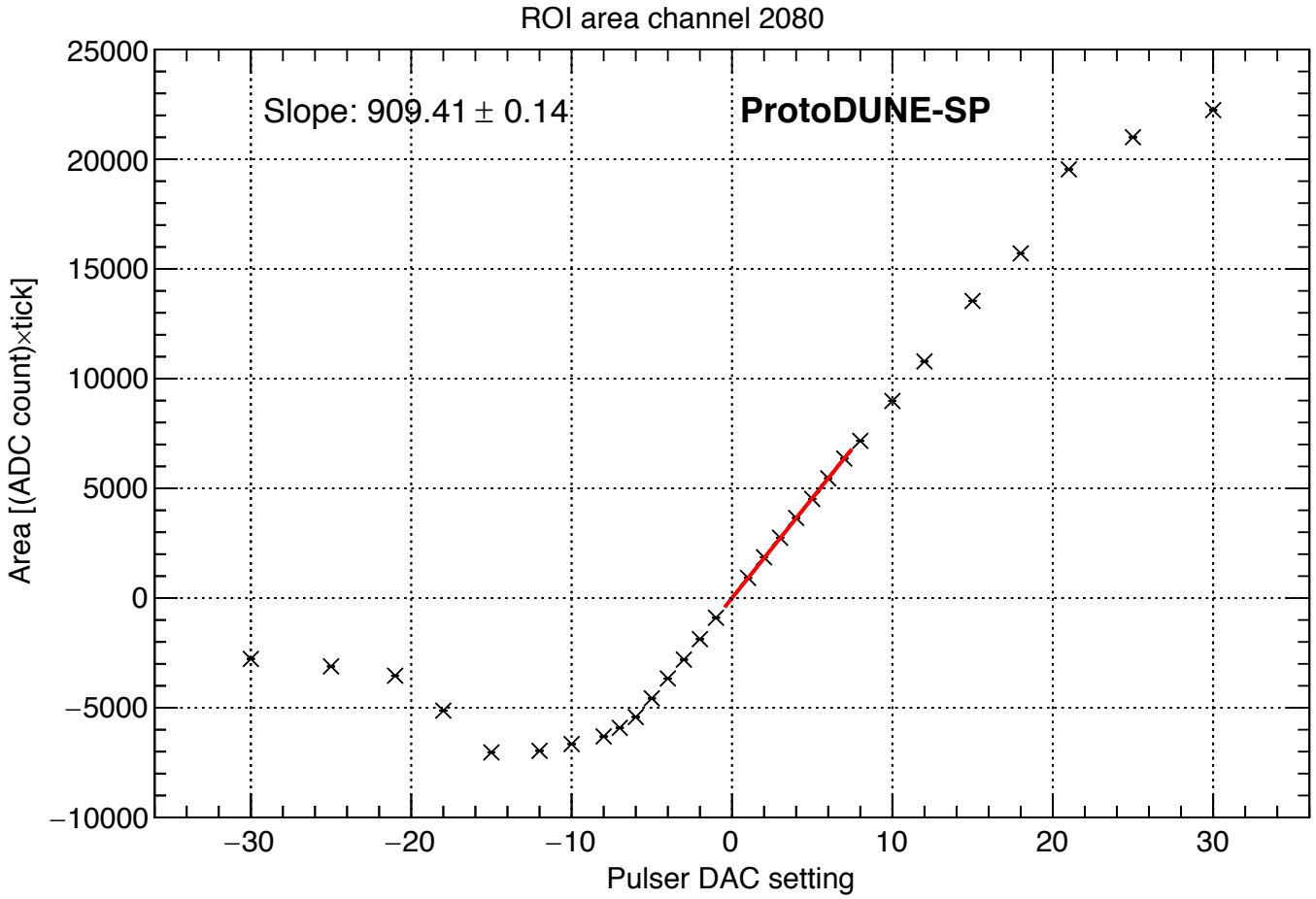
- Two in situ DAC available on the FEMB
  - “external” generated by the FPGA
  - “internal” generated by the FE ASIC
- Configure:
  - FPGA controls clock to generate all pulses:
    - Set FPGA to pulser mode, delay (relative to sampling clock), frequency
  - Decide between INT or EXT on each ASIC
  - Connect test capacitor to each FE channel input (channelwise)
    - Leaves channel input active
- Data-taking: each DAC setting is a unique run
  - All WIBs and FEMBs reconfigured
  - ~5 minutes to configure DAQ
  - 2 minutes/run
    - ~50 events each containing ~12 bipolar pulses

Analysis

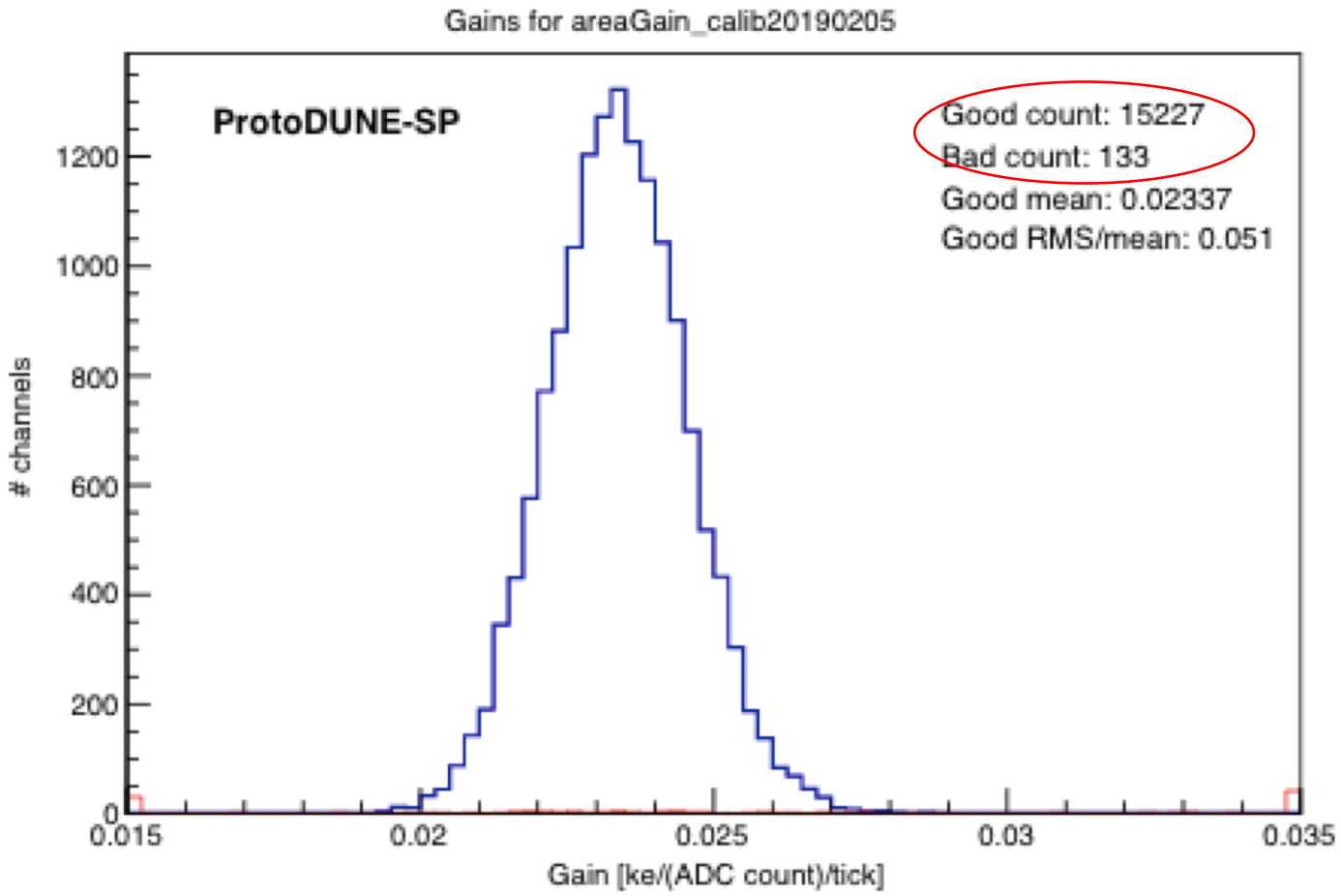
- Area of interest for calibration:
  - DAC 1-7
- At each DAC setting:
  - Average area under the pulse is plotted as a function of DAC value
  - Known DAC step size:

$$Q_s = 3.43 \text{ fC} = 21.4 \text{ ke}^-$$

- From fit and DAC size extract gain in e-/ADC



Gain and Issues



- Every channel was included in every DAC value run
  - Only several times did we take DAC values well into saturation
  - After that only DAC values 1-10 for the default detector gain and shaping time (14 mV/fC, 2 usec) were taken
- Slow and lots of deadtime!
- Solution (*not implemented*):
  - Use EXT pulser, 1 DAQ run
  - Configure all FEMBs 1 time
  - During run, raise the trigger inhibit every 5 minutes, change the DAC setting in the FPGA, lower inhibit, continue taking data