DUNE Single Phase DUNE Warm Electronics and System

Report of the Preliminary Design Review

March – April 2020

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1. Executive Summary

This document is the report of the Preliminary Design Review (60% design maturity) of the Warm Electronics and System which was held remotely in the period March 23rd –April 15th.

No major problems have been detected and the proposed design and program of work in view of being ready for an FDR in Spring 2021 are deemed appropriate.

The documentation (requirements, specifications and interfaces) needs to be completed. It is noted that interfaces to external systems that are not yet specified in DUNE, such as the DDSS, cannot be fully specified. Nevertheless, requirements from the WIB to those systems have to be formalized.

2. Review Committee

Reviewers

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3. Agenda and Documentation

Agenda and documentation are available on the indico site: https://indico.fnal.gov/event/22807/

4. Review Process

The review was initially expected to be a meeting in Brookhaven on March 10th and 11th. Due to the COVID-19 crisis, this meeting was dropped and it was decided to run a remote review. A first meeting was organized between the review committee and Marco Verzocchi during which Marco made an introductory presentation. The review committee had then a week to read the documentation and all the presentations prepared by the design team. After a meeting of the review committee on March 23rd, a list of questions was sent to the design team. The design team answered by email on March 31st. A few clarifications were still requested and a meeting between the design team and the review committee was held on April 7th.

5. Findings and Comments

5.1. Scope of the review

The services (cables and power supplies), the WIEC (Warm Interface Electronics Crate), the WIB (Warm Interface Board), the PTC (Power and Timing Card) and the grounding and shielding scheme were reviewed.

DUNE needs 150 WIEC's each of them housing 5 WIB's and 1 PTC. Each WIB interfaces with:

- 4 FEMB's (Front-End Mother Board) housing either the 3-ASIC front-end chips (LARASIC, COLDADC and COLDATA) or the CRYO front-end chip. Cold cables between the FEMBs and the WIBs carry timing, control, data and power;
- The PTC (through the WIEC backplane) from which it gets power, timing signals and configuration signals;
- The DAQ system through optical fibres to FELIX;
- The DAQ and Slow Control (SC) through one ethernet fiber.
- Possibly the Dune Detector Safety System (DDSS).

5.2. Grounding & Shielding

The presented scheme looks good to the committee and it has mainly been validated in ProtoDUNE. A question arose concerning the move of the DAQ hardware on the cryo mezzanine. Although this equipment is referenced to the facility ground system and should not interfere with the front-end electronics some specific tests should be done. The design team agrees and will perform these tests on ProtoDUNE.

5.3. WIEC

The design is mainly unchanged with respect to the ProtoDUNE design. As a follow-up of a few problems, changes were made to improve it. Following questions from the review committee, a few points were clarified.

The warm flanges are easily accessible on the top of the cryostat, and the maintenance of the air filters (i.e. replacing the old filter with a new one) will not require more than a few minutes of down time for each WIEC. The WIECs are at a height of ~20 cm above the false flooring, which means that the personnel replacing the air filters will have to kneel or bend over during the operation. The area on top of the cryostat will be accessible without any restriction during the operation of the detector (a fence around the TPC electronics cryostat penetrations and the photon detector mini-racks is to be installed to prevent people from running into them). Given the small distance between the WIEC and the false floor the air filter will be above the WIEC and have the air flowing downward. This is still to be included in the CAD models.

For firmware development purposes there will be multiple WIECs operating. These may not be fully populated (i.e. have multiple WIBs), but the goal is to have one of them operating in each institution involved with the WIB/PTC firmware development. Eventually, during operations, one of these test stands could be installed on the surface at SURF, in such a way that the personnel responsible for operation on site will be able to exercise the maintenance tasks there, prior to performing them on the systems used for data taking.

5.4. WIB

The WIB requirements document and the firmware/software document are still too vague and it is not clear how real specifications will be defined/derived from it. For instance, the allowed power dissipation, the allowed weight should be clearly defined. The 1% downtime required should translate in allowed data transmission errors, allowed loss of synchronization and time to recover. Detailed comments on these documents have been given to the design team. The design team will try to improve both the hardware and the firmware/software requirement documents but mentions that many of the comments of the committee on the WIB requirements document highlight the fact that these documents are preliminary and need to go through a joint review by the TPC electronics and DAQ consortia. The firmware/software document in particular is a planned extension of the interface document between the two consortia. The design team will continue updating the WIB requirement documents as the design of the DAQ Control, Configuration and Monitoring (CCM) sub-system and SC evolves, to ensure that the systems are fully compatible. In the meantime, the design of the WIB can start. Concerning the total power dissipation, preliminary numbers based on ProtoDUNE have been used to define the overall air-cooling requirements in the cavern. The allowed weight has an impact on the thickness of the tubing used for the TPC electronics spool pieces. This has been studied for ProtoDUNE and needs to be documented in the requirement document.

The presented changes with respect to the WIB design used in ProtoDUNE and the development plan are fully justified and consider all the lessons learnt in ProtoDUNE.

The firmware is to be designed by several institutes and the way this will be efficiently done is not yet fully defined. How will the different blocks be defined (including detailed interfaces between blocks), what will be the design follow, what will be the verification flow, are being worked out. The committee is pleased to see that an engineer in charge of the firmware/software development has been nominated and acknowledges the fact that defining and putting in place this process will still take 2 to 3 months. It is recommended to fully document this process and to have a light follow-up review when this is done.

The qualification of the high-speed links has been clarified and it has been shown that even with a BER at the level of 10^{-12} the down time of the detector is very minimal. The design team will nevertheless make BER tests up to a lower level during QC tests.

There are two options for the front-end (3-ASIC or CRYO) and the interfaces to the WIB are not the same for the 2 solutions. The requirement documents should reflect these differences and there should be a detailed description of the interfaces for the two solutions (data format, protocol, control of synchronization, resynchronization process). These documents are planned to be completed during the Fall of 2020 and it is assumed there will be enough time to have an implementation for the two front-end solutions in time for ProtoDUNE run 2.

The WIB should be compatible from the hardware point of view with FEMBs housing the 3 ASIC solution (i.e. communication via COLDATA) and FEMBs with the CRYO solution. The powering scheme of the current intermediate WIB prototype is compatible with both types of FEMBs. From the firmware point of view, two different versions of firmware re needed and the firmware is divided in blocks in a way that minimizes the amount of firmware that differs between the two solutions. The differences between the two versions will be limited to the block that communicates with the FEMB. This block controls both the communication from the WIB to the FEMB, which uses I2C in the case of COLDATA and SACI in the case of CRYO, and the decoding of the data from the FEMB, which can be asynchronous data with 8b/10b encoding (COLDATA) or synchronous data with 12b/14b encoding (CRYO). The FEMB block also needs to handle the different synchronization mechanism for the two types of FEMBs. However, as there is a single design team for both solutions the priority is put on the 3-ASIC solution (communication with COLDATA). When developing the CRYO version of the firmware it is planned to reuse blocks of firmware library (communication with SACI, 12b/14b decoder) that have already been developed by the SLAC group.

5.5. PTC

It is proposed to modify the PTC in order to increase the monitoring and control on the power distribution from the LV power supplies to the WIBs and to provide an interface to the DCS and to the DUNE detector safety system (DDSS). The proposed modifications of the PTC make sense. The design team also clarified that the intermediate WIB design can easily be adapted (change of firmware) and that no design change is required for the WIEC backplane. However, the implementation is still to be done and the documentation to be updated.

The role of the PTC with respect to SC and DDSS requires some clarifications. Some of them have been given and a diagram showing the interactions have been produced. However, the interaction with DDSS is not just a simple interlock implementation and to be effective it still requires the firmware/software of both the WIB's and PTC to be fully functional. The interface to DDSS and the interlocks needs additional analysis. All the failure modes should be identified and the interlocks generation defined after this analysis.

Requirement and specifications documents for the PTC are still in preparation. It should be ready in June 2020.

5.6. Power Supplies

The proposed scheme makes sense. The statement "Both the WIENER PL506 and the ISEG HV modules that are in use in ProtoDUNE have ripple voltages that exceed the requirements for DUNE" should be and will be documented with measurements. It is said that the last LDO reduces the input ripple at the level of 10^-4 which should be enough to reach the few µV ripple needed at the input of the front-end chips.

The way the interlock is implemented on the power supplies should be documented.

It is clarified that the power dissipated in the warm cable trays does not require a special cooling.

All the power lines (Bias, HV, LV to the front-end) are potential single point failures but some redundancy can be implemented. On the top of the cryostat it is possible to replace power supplies and cables if needed. It is assumed that a failure on the power supplies or on the bias voltage supplies will result in a downtime of up to 2-3 days, until a spare unit (available at SURF) can be installed. Components inside the cryostat cannot be accessed or replaced and there is not sufficient room to increase the redundancy of the power or bias voltage distribution system. For the bias voltage lines, it could be conceivable to add some redundancy, but for all other cables inside the liquid argon this is not possible. This stresses the importance of having reliable connections on the FEMBs and on the flange (this has been a sour point in ProtoDUNE, in particular for the signal cables, and the reliability of the connector on the FEMB has been improved in the new design). The final scheme for the power distribution between the WIB and the FEMBs is not yet fully defined, but it is likely that some redundancy could be built in the system. The design presented in the TDR has a single LV sent from the WIB to each FEMB over multiple AWG20 wires. If a single wire is disconnected, this would lead to having the same current being transferred over a smaller number of wires, resulting in larger ohmic losses between the WIB and the FEMB. This could be compensated by increasing the voltage on the WIB, such that the final input voltage on the FEMB is unchanged.

For the field cage termination bias voltages, there are failsafe terminations inside the cryostat such that in case of a bias cable connection failure, the field cage module is terminated to a voltage not too different from the optimal bias value to maintain near normal operation.

5.7. Interfaces to DCS, DDSS and Interlocks

The committee requested some clarifications concerning this aspect and a diagram of the different interactions has been presented.

In general, an interlock only involves a very few hardware signals and should always be working as the last line of defense if something is dangerous. When the system is fully working the DCS has all the needed information to take appropriate actions. The presented scheme shows communication between the WIBs the PTC and DDSS and requires that some firmware/software is working. The team is encouraged to make an analysis of all possible failure modes and to define the interlocks only after this analysis is done. It seems unrealistic to have a very high level of granularity for the DDSS instead of having interlocks cutting complete crates (i.e. only have connections to power supplies), when needed (i.e. when everything is going wrong).

A list of all the quantities that are going to be monitored and controlled, or simply monitored from the SC as well as a list of all the channels that provide inputs to the DDSS have been provided.

In the case WIBs are used both for SC and DAQ traffic, probably different levels of reset are needed, in order to keep the SC communication up and running at all times.

The fans control, is currently based on the current drawn to decide whether they are in rotation or not. For ProtoDUNE there is a design (not implemented yet) that actually checks the fans speed. The design of DUNE will be an evolution of that design, and it could also include feedback from the temperature sensors on the WIBs and on the PTC (which would be transmitted via the DDSS).

5.8. Timeline and production

The idea of having a PTC with an FPGA dates from February, when prototypes of the intermediate WIBs were already in hand. It turns out that the communication between the PTC and the WIB can be implemented on a bus that was already available on the backplane of the warm interface electronics crate (the PTB). This bus was originally meant only to assign an address for each WIB (and therefore there is already a connection on the printed circuit board of the WIB between that bus and the FPGA), but it can be repurposed for the I2C communication between the WIBs and the PTC. Therefore, it will be possible to test the communication between the new PTC and the current WIB as soon as a new PTC prototype is available.

For ProtoDUNE run 2 a total of 20 WIBs (five per APA, with 4 APA total), and 4 PTCs (one per APA), plus spares are needed. It is too early to decide that the current WIB prototype will be the one used for the ProtoDUNE run 2. It is possible that an updated version will be produced (with a simpler power distribution and a reduced number of voltage regulators). A complete test of these modules will be available in Spring 2021. In addition, the current WIB prototype will be used with prototype FEMBs with the current version of the ASICs in Summer 2020. It will be used in system tests at the Fermilab ICEBERG test stand and in the cold box at CERN using the first prototype DUNE APA. The FDRs for all the TPC electronics components are planned for Spring of 2021, before the fabrication of the components for the ProtoDUNE run 2 is launched. This schedule for the WIB/TPC is reasonable

The PRR for the WIB/PTC will be held early 2023 after additional WIB/PTC prototypes will have been tested in ProtoDUNE in 2022.

6. Recommendations

The requirements, specifications and interfaces documents should be completed. The time scale is June 2020 for the PTC and Fall 2020 for the WIB. Although the requirements documents can be completed right away, the final specifications will be completed when the DAQ, DCS and DDSS are fully defined.

The interface to DDSS and the interlocks needs additional analysis. All the failure modes should be identified and the interlocks generation defined after this analysis.

The sharing of the tasks between the firmware and the software as well as their developments within several institutions must be fully defined and documented. This is expected within the next 3 months.

When the above-mentioned documents are completed, a light follow-up review is to be held.

The proposed prioritization of the developments for the two possible front-end solutions (3-ASIC first priority and CRYO second priority) is to be maintained and the amount of resources available to complete these two versions before Spring 2021 is to be monitored.

7. Answers to the Review Charge

1. *Are the full specifications of the detector components, designs and complete documentations for users available in EDMS?*

There are documents available but some of them are still incomplete and some changes are still being considered and hence not yet fully documented (e.g. PTC). The design team has a clear plan for completing them within a few months.

2. *Does the system design address detector requirements: performance, installation, grounding, testing, calibration, commissioning, operation and maintenance? Are the impacts of detector capabilities and goals on physics performance well documented? Have design choices been fully identified and do they meet detector requirements?*

Even though some details are not yet fully defined, the overall system design addresses the detector requirements and meets the detector requirements. Some part of the design (e.g. grounding) has already been fully validated in ProtoDUNE.

3. *Have lessons learned from ProtoDUNE been implemented both for the overall system design and for the individual design of components?*

Yes. The solutions validated in ProtoDUNE have been integrated in the designs and those presenting weaknesses have been modified and improved (for example the need for including debug tools in the WIB firmware).

4. *Have interfaces with other detector components (including interfaces with TPC electronics systems that have already been reviewed) been addressed and documented? Do risks of design changes in other systems have appropriate mitigation strategies?*

Yes. The interfaces with other detector components have been addressed. In particular the interface with the two possible front-end designs (3-ASIC or CRYO solutions) have been worked out and the firmware blocks dealing with them identified (data readout protocol and format and synchronization). However, this is not yet fully spelled out in the documentation (only the 3-ASIC case is documented).

Some interfaces with parts no yet fully defined (DAQ, DCS and DDSS) are still to be completed and the design team has a clear plan for this.

5. *Are engineering analyses sufficient to ensure the design is safe during all phases, and have applicable design codes and standards been satisfied?*

In general, the answer is yes although the work will be fully completed in a few months only.

An engineer in charge of coordinating the firmware/software is nominated. The sharing of work and the development process are being worked out and should be finalized within 2–3 months. A light (email based) follow up review is to be organized when this is fully documented

The interface to DDSS and the interlocks needs additional analysis. All the failure modes should be identified and the interlocks generation defined after this analysis. A follow-up review should be organized at a later stage and after DDSS is defined.

6. *What is the status of the procurement strategy and of the manufacturing and testing plan? Are they compatible with the current design and with meeting the detector requirements?*

A fully defined and detailed procurement strategy is not required at the level of a PDR. The design is based on available and non-obsolete components and the presented plans for spare procurements is sensible.

The testing plan is satisfactory. The manufacturing of the prototype WIBs and PTCs has needed a quite high level of reworking; the testing procedure has easily identified the problems.

7. *Are quality assurance and testing plans sufficiently developed to proceed to final design?*

Yes, QA and testing was presented, but this should be documented in a QA-QC plan. See following question.

8. *Are plans for additional prototyping reasonable and sufficient?*

The prototyping plans as well as their testing and validation are sufficient and appropriate. The ProtoDUNE run 2 version will be extensively used before the final DUNE version is finalized.

9. *Have appropriate cost estimates and schedule been determined? Are plans for required technical resources consistent with scope of remaining work?*

There were few discussions about cost estimates and long-term schedule. The only point of concern is the fact that a single (not that large) design team has to work on the current intermediate design, the two versions needed (3-ASIC and CRYZO) for ProtoDUNE run 2 and the final version.