

# Replies to committee's questions

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# Questions from the committee

- 11 questions received on Saturday 4 April
- Answers in the following slides

# Question 1

- Q. We understand that the intermediate WIB can work with the new PTC. This requires a change of firmware to have the WIB driving the I2C lines. Has this modification already been implemented ?
- A. No, this is a new requirement, and it will be implemented on the timescale of end 2020, when the prototype of the new PTC is available

# Question 2

- Q. The interface PTC/SC has still a lot of options opened. When and how the decisions will be made ? Will it be during the Fall with the new requirement document ?
- A. The design of the SC system is not defined at this point. The DAQ/SC consortium is testing (in ProtoDUNE) the extension of the OPC UA protocol to the WIENER power supplies. The DAQ/SC consortium is also testing the Ignition software platform. We need input from the DAQ/SC consortium on the scalability of this system
- TPC electronics has  $O(1000)$  nodes,  $O(30,000)$  quantities to be monitored. How many SC control computers are needed for this ? Would it be easier to reduce the number of nodes to  $\sim 200-250$  ?
  - Decision on whether SC talks to each WIB or just to the PTCs should be taken jointly by DAQ/SC and TPC electronics consortia
  - A timescale of Fall 2020 would allow the DAQ/SC consortium to perform more tests, get better understanding of scalability issues

# Question 3 (i)

- Q. We understand there is an engineer in charge of coordinating the firmware/software work. Could we have details about the process to be put in place ? Will there be a mechanism to remotely update PL firmware ( “Gateware” ) and PS firmware ? Will there be a mechanism to remotely recover the WIB if the firmware becomes corrupted and renders the board inoperable ?
- A. We are setting up the team for the firmware development right now, and it is too early to discuss how the team will be organized and how we will do the firmware development. We plan to have test stands at all the sites involved in the development.

## Question 3 (ii)

- Q. We understand there is an engineer in charge of coordinating the firmware/software work. Could we have details about the process to be put in place ? Will there be a mechanism to remotely update PL firmware ( “Gateware” ) and PS firmware ? Will there be a mechanism to remotely recover the WIB if the firmware becomes corrupted and renders the board inoperable ?
- A. We plan on having the capability of remotely updating both the PL and PS firmware independently. We also plan to store in flash multiple copies of firmware, which would allow us to revert to a golden image in case of firmware corruption, using the Zynq+ multiboot capability

# Question 4

- Q. The DUNE-SP timing system periodically interrogates the status of every timing endpoint in the system. The endpoint must be able to turn on and off its return signal to the timing master when commanded by the timing master. Is it envisaged that in normal operation all five WIBs in a WIEC will function as timing endpoints? Or will the PTC be the single endpoint in the WIEC ?
- A. Each WIB will be a timing endpoint, like in the current system. In the current system a clock fanout on the PTC broadcasts the timing signal to the 5 WIBs via the backplane of the WIEC. On the return path the timing signals from the 5 WIBs go through a multiplexer that is controlled by a priority encoder which selects which WIB is transmitting information back to the timing system. The input to the priority encoder is provided by the FPGA on the WIB interrogated by the timing system (8 lines are used for this purpose on the backplane)

# Question 5

Q. Lines in the WIEC will be configured as an I2C “backplane” . If the WIBs are timing endpoints will they be able to be I2C masters and control the single optical transmitter if they are interrogated by the timing master? How long will it take for these I2C transactions to complete and the transmitter to be activated ?

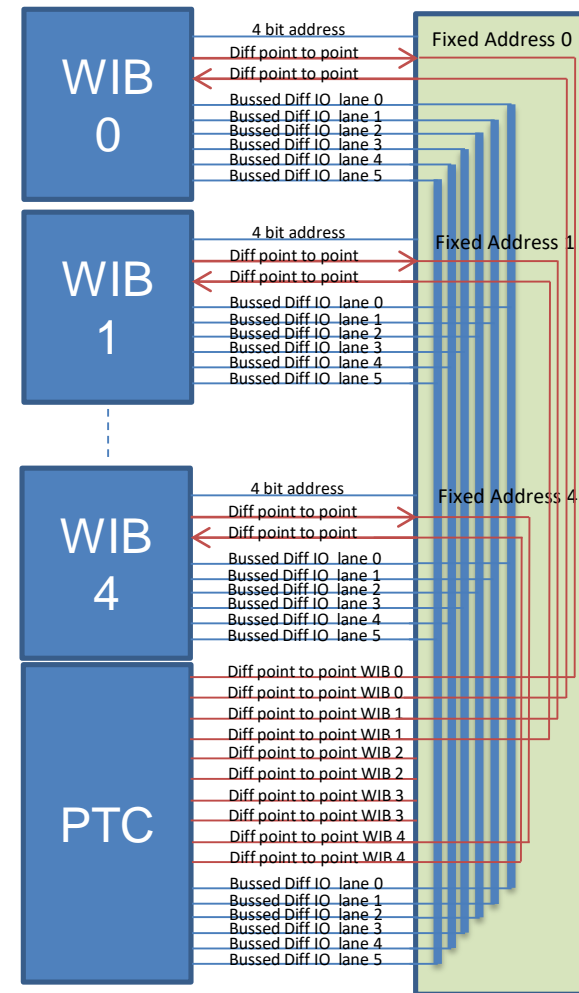
A. This should work as follows:

- Timing system tells the WIB in slot x to configure for the delay measurement
  - The FPGA in the PTC sets appropriate bit in the priority encoder in such a way that the reply sent to the timing system from the WIB in slot x is selected
- Timing system sends signal to WIB in slot x, received by the FPGA there
- FPGA in WIB in slot x sends alarm to the FPGA in the PTC, then replies to the timing system with a fixed delay
- That reply is sent back to the timing system
- Further checks are performed and finally the timing system downloads the delay information on the timing endpoint
- Exact sequence needs to be discussed with the DAQ consortium



# WIEC backplane

- Each WIB connection to the PTB Include
  - Fixed 4 bit slot address
    - Used for geographical addressing
  - Two differential point to point connections to the PTC
    - Used to pass timing system signals
  - Six differential bussed signals OR 12 single ended signals.
    - For ProtoDUNE they were used as single ended signals
      - 4 lines used as a crate address for geographical address
      - 8 lines used as a priority encoder to select which WIB is selected to use the PTC SFP TX link
    - For DUNE they can be used as I2C links so that the smart PTC can communicate with the WIB
      - Slot address will be used for WIB I2C address
      - 2 lines used as I2C (PTC master)
      - 5 lines can be used as alarms from WIB to PTC where the slot address will either tri-state the line or use it for the alarm
      - Crate address will be delivered over I2C
      - Priority encoder function now controlled by smart PTC/I2C
      - 5 spare lines TBD



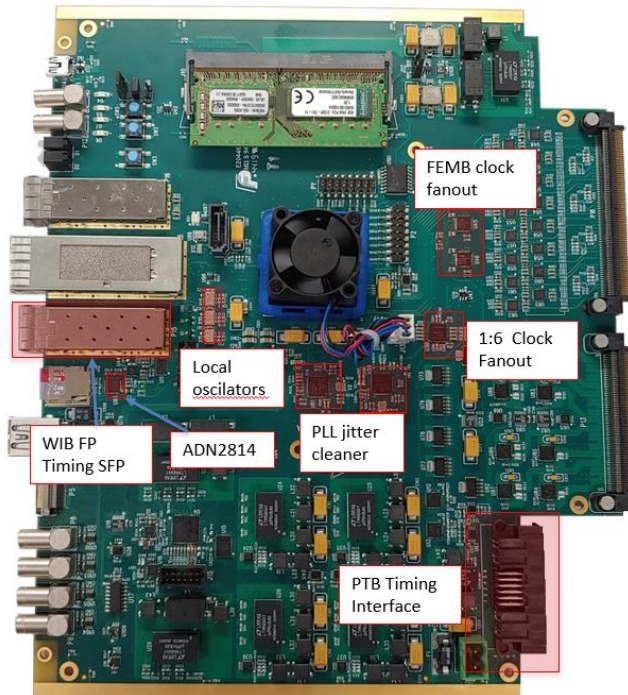
# Question 6

- Q. A minor question: Every timing endpoint in the system must have unique identifier. Is it anticipated that this will be the unique hardware identifier associated with the PCB ( if I understand correctly from response (14) each board will have ROM with a unique ID ) or will it be associated with geography ( slot, crate number )?
- A. To be decided: we can have either a unique address based on the combination of a unique address for the PTC plus a slot number for the WIB. For example if in the crate for APA 122NU (detector 1, row 22, north array, upper APA) we have a PTC with identifier 0x2f, the 5 WIBs could be called 0x12f to 0x52f (we have allocated 8 bits to the WIEC address and 3 to the WIB address in the [data format for the TPC electronics](#), this is consistent with having unique addresses for 1 detector, assumes that the timing system does not talk to 2 detectors at once).

# Question 7

Q. It looks like p17 of [Jack's presentation on the WIB](#) has the wrong text. What text was intended to be there?

## WIB Clock Distribution



– WIB discrete timing components

- The WIB is capable of multiple timing configurations including an option only to use discrete components without the need to run clock signals through the FPGA .
  - Benefits include
    - » Deterministic Timing
    - » Reduced timing jitter
- The option to use the FPGA is available which does allow for more system flexibility

03/10/2020

2020 DUNE WIB PDR

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# Question 8

- Q. Concerning the BER, in your answer you mention that a BER of  $10^{-12}$  leads to 0.44% down time. How do you get this number when at most you lose  $10^6$  samples per day i.e. 0.5 second per day ?
- A. This number is obtained assuming that a corrupted frame in any of the 750 WIBs leads to the loss of the information for the entire detector, which is clearly a pessimistic assumption (and by the way this is wrong by a factor of 2 because the data transmission is over 2 links, which are independent). Given the nature of the data transmission between the WIBs and FELIX, with idle patterns being sent after frame, a simple non-repeated bit error in the WIB to FELIX data transmission (which is detected using the checksum at the end of a frame) introduces a negligible dead time.

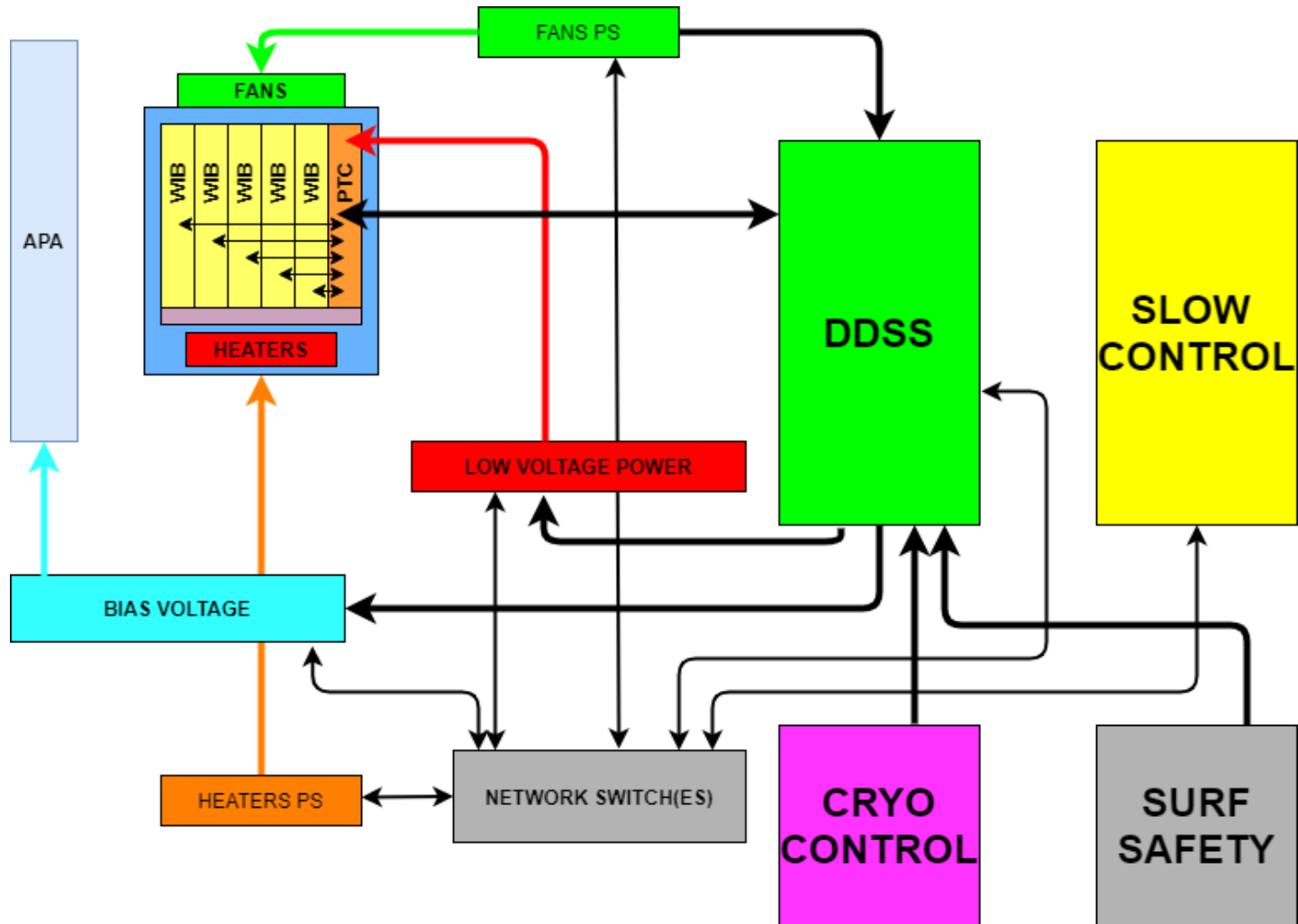
# Question 9 (i)

Q. The question of the interlock is still a bit unclear. For instance, disabling the power of a FEMB could be locally decided without requiring communication with DDSS etc. Would it be possible to have a diagram showing the interlock generation ?

A. See picture on the next page

- Arrows indicate direction of power/bias/control/information
- Thick black lines indicate connections that provide inputs to the DUNE detector safety system and that provide interlocks to the PTC, bias voltage supplies and low voltage power supplies
- Colored thick lines indicate bias voltage supply lines or power supply lines
- Thick black lines ARE NOT part of the Slow Control network, form independent network (ProfiNet, ProfiBus, or EtherCAT) that is entirely under DDSS
- Thin black lines indicate slow control commands and status information (all slow control communications go through network switches)
- Similarly expect to have dedicated inputs to DDSS from Cryo Controls (is the LAr boiling ?) and from the SURF safety system (is the cavern on fire ?)
- Other detectors have their inputs in the DDSS, receive their inhibit signals from the DDSS (not shown in picture)

# Question 9 (ii)



## Question 9 (iii)

- The DDSS receives inputs from the PTC, the fans, the CRYO controls, the SURF safety system
- The DDSS can receive the status of the bias voltage supplies, the low voltage power supplies, and the heaters power supply via the Slow Control
- The DDSS provides its status and alarms to the Slow Controls for monitoring
- The PTC provides to the DDSS the status of the WIBs and the FEMBs, the PTC receives inhibit from DDSS signals that can be used to turn off the power to the FEMBs with higher granularity compared to the inhibit signal sent to the low voltage power supplies
  - Inhibit to the WIB: turn off individual FEMBs
  - Inhibit to the PTC: turn off individual WIBs
  - Inhibit to the low voltage power supply: turn off entire WIEC
- Communication between PTC and DDSS is via optical fiber, requires optical to electrical conversion at the DDSS I/O

# Question 9 (iv)

- The DDSS can turn off the low voltage power (individually, APA by APA) by sending inhibit signal to the LV supplies
  - Additional layer on top of sending signals to FEMBs, WIBs, PTC
  - Communication between DDSS and LV supply is electrical (requires conversion of digital output from DDSS 0-24 V logic to TTL signals)
- The DDSS can turn off individual bias voltage channels by sending inhibit signals to the bias voltage supplies
  - Communication between DDSS and bias voltage supply is electrical (requires conversion of digital output from DDSS 0-24 V logic to TTL signals)
- Decided that fans power supplies provide status to DDSS, but have no interlock (requires conversion of TTL signal to digital input in 0-24 V logic of DDSS)
- Heaters power supplies TBD (shown only under slow controls in diagram)
- Interaction with other detector components to be understood
  - Example: may want to have inhibit on field cage termination electrodes bias depending on status of cathode power supply



# Question 9 (v)

- Examples:
  - FEMB draws very large current
    - Suspect failure on FEMB
    - If power turned off on FEMB, may not have protection on amplifiers
    - It is better to turn off the bias voltage for that APA
    - Need to tell bias voltage supply to turn off three specific channels
  - PTC not being powered on
    - Missing signal at input of DDSS that FEMBs are in the correct state
    - Prevent bias voltage from being turned on for that APA, send inhibit signal to three specific channels on the bias voltage supply

# Question 9 (vi)

- PTC does not take interlock decisions, the action matrix is in the DDSS
  - The question is all the action matrix is entirely in the DDSS or whethersome fraction of the action matrix (are all the FEMBs OK for this APA) is in the firmware of the FPGA
  - Decision between the two solutions depends on the PTC to DDSS communication protocol (send 1 bit or send more information in the PTC to DDSS direction)
  - Similarly in the opposite direction the decision whether to turn off 1 FEMB / 1 WIB / entire crate depends on how much data is transmitted
  - Communication between PTC and DDSS is optical, whether a single bit of information or whether multiple bits are sent depends on DDSS architecture

# Question 10

Q. Could you clarify the schedule for getting all the interface and requirements documents finalised ?

A. We will try to get all the interface between firmware/software blocks and all the requirements documents in place by the end of July

- This partially depends on the level of detail, in some cases we may also profit from starting the FW/SW development to better understand the interfaces between blocks and hence the requirements
- In some cases we need communication with DAQ/SC consortium to understand interactions between two systems

# Question 11

- Q. Finally a remark concerning Grounding: it may be more valuable to use a signal generator that can produce radiated and conducted noise at the maximum possible level permitted by 150 PCs for the tests with ProtoDUNE.
- A. This is a good suggestion. We will try to perform the measurement in this way.