ProtoDUNE-SP Warm Interface Electronics

Research, Development, Production, Installation and Commissioning

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Brookhaven National Laboratory

DUNE Cold Electronics WIB and System Review
March 10, 2020

Outline

- ProtoDUNE-SP Cold Electronics
- Warm Interface Electronics
  - Power, Timing and Control Distribution
  - Warm Interface Board (WIB)
  - PTC, PTB and Flange Board
  - WIEC and Feedthrough Assembly
- WIB Standalone Read-out for FEMB Testing
- Warm Interface Electronics Electrical QC tests
- Firmware and Software
- Summary

ProtoDUNE-SP Cold Electronics System

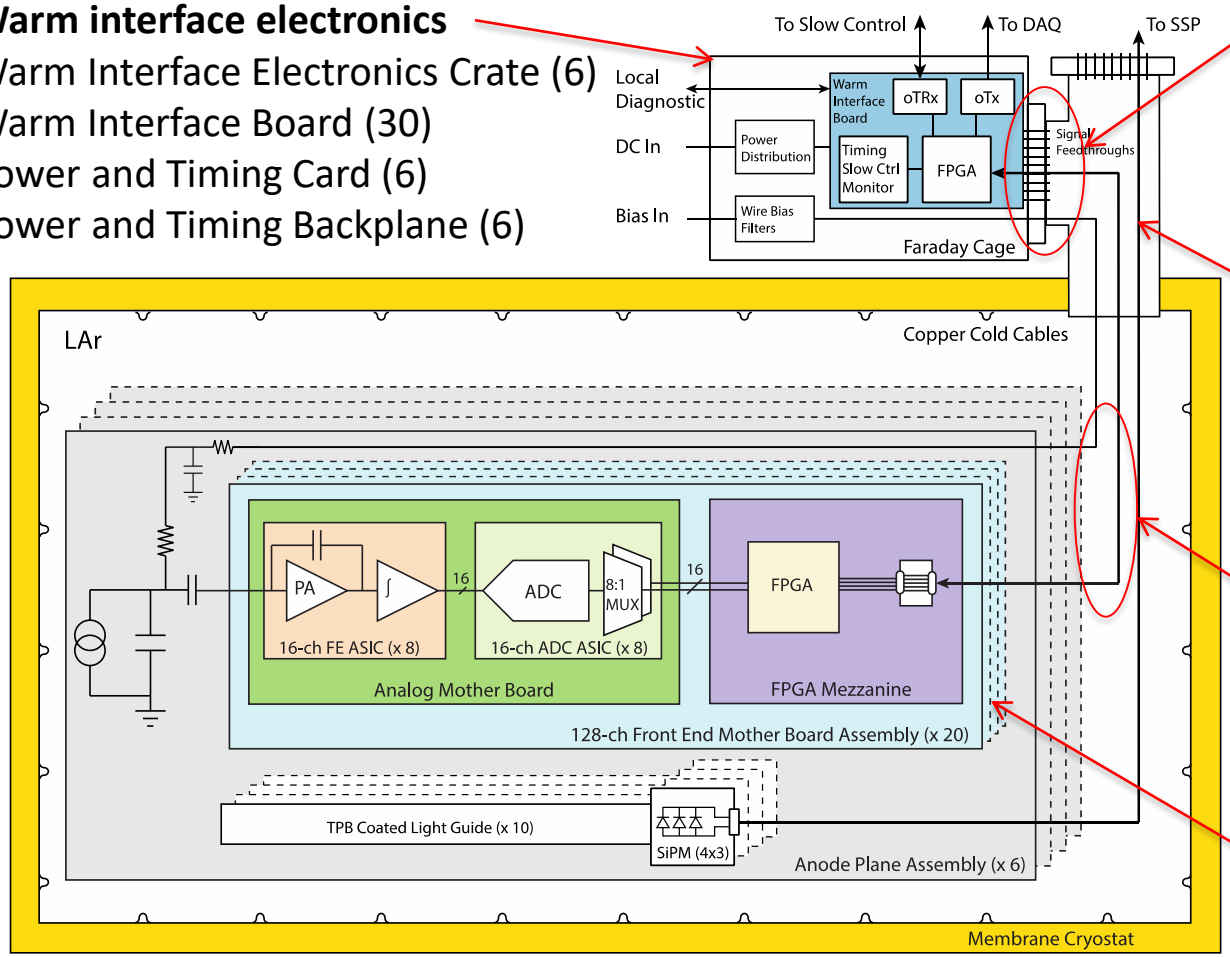
Warm interface electronics

Warm Interface Electronics Crate (6)

Warm Interface Board (30)

Power and Timing Card (6)

Power and Timing Backplane (6)



CE flange

Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

Signal feed-through

Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

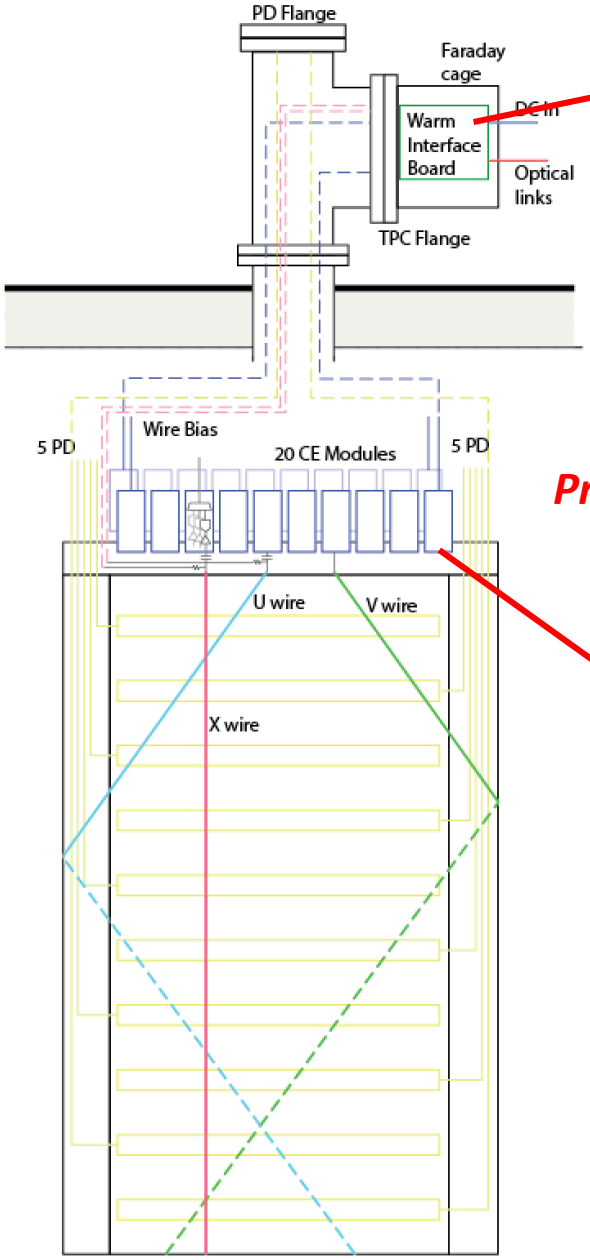
Cold cable

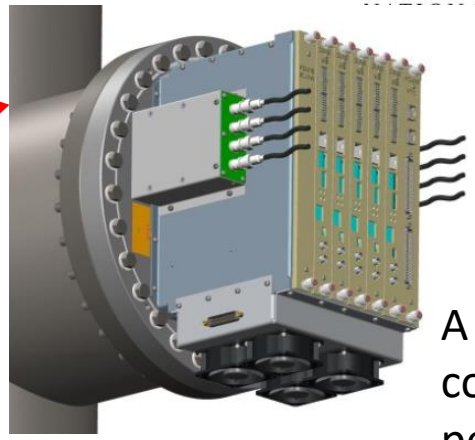
LV and data cable (120+120) to FEMB and APA wire-bias SHV cable (48)

Front End Motherboard

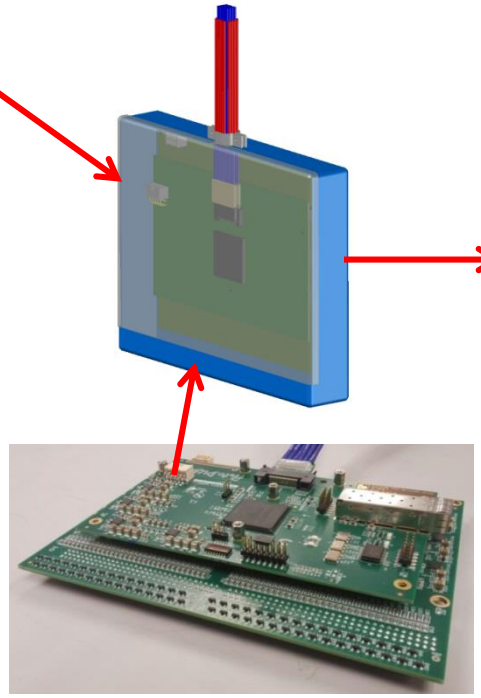
(FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

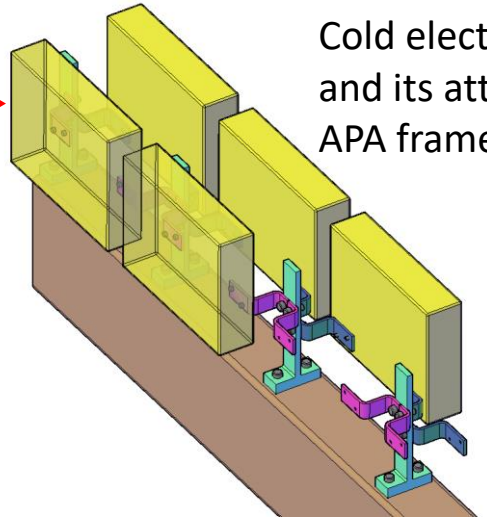
Integral System Design Concept





ProtoDUNE-SP



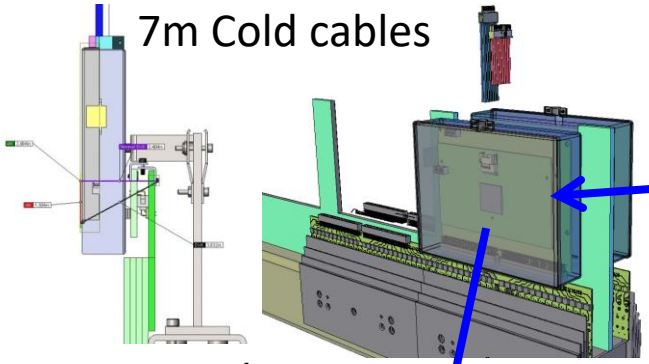


A necessary (but not sufficient!) condition to achieve a good performance, **the integral design concept** of APA + CE + Feed-through, plus Warm Interface Electronics with **local diagnostics** and strict isolation and **grounding rules** will have to be followed

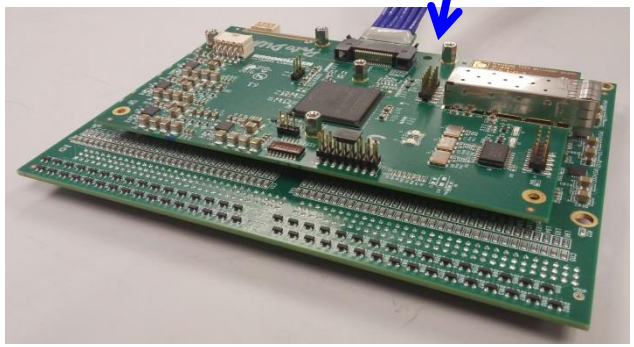
Cold electronics module and its attachment to the APA frame

One WIEC for One APA Readout

7m Cold cables

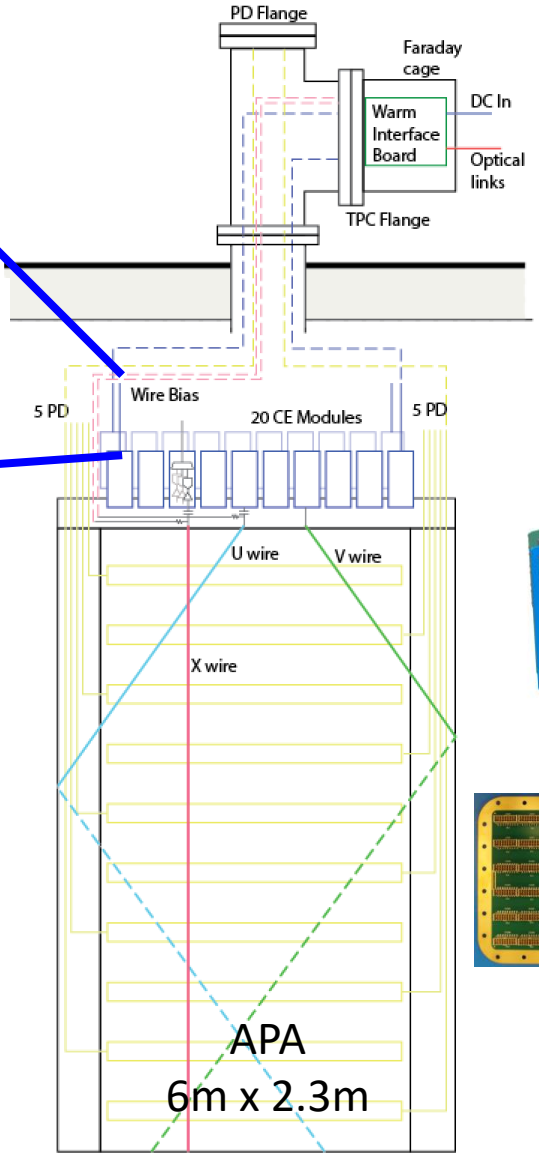


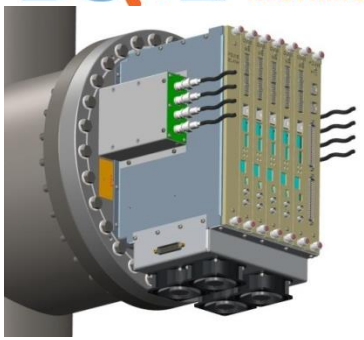
20 CE boxes on APA



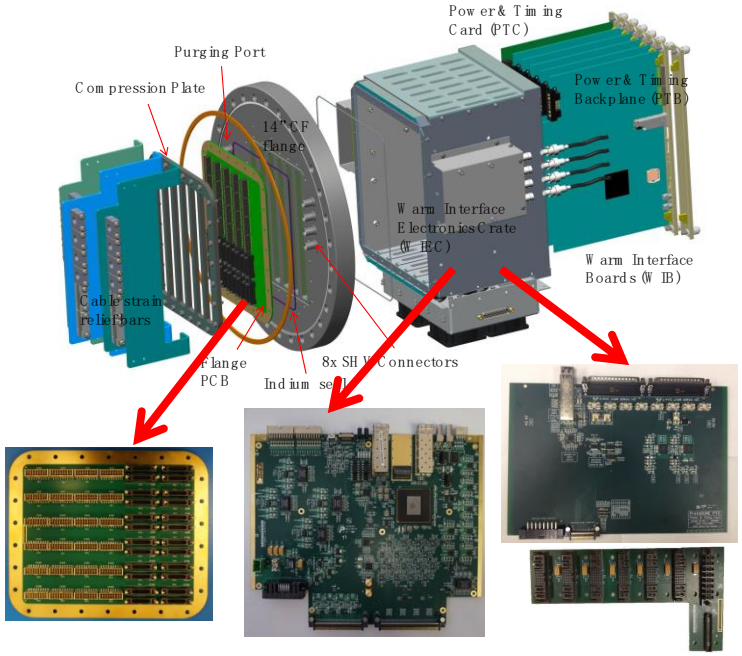
FEMB (inside CE box)

Cold Side





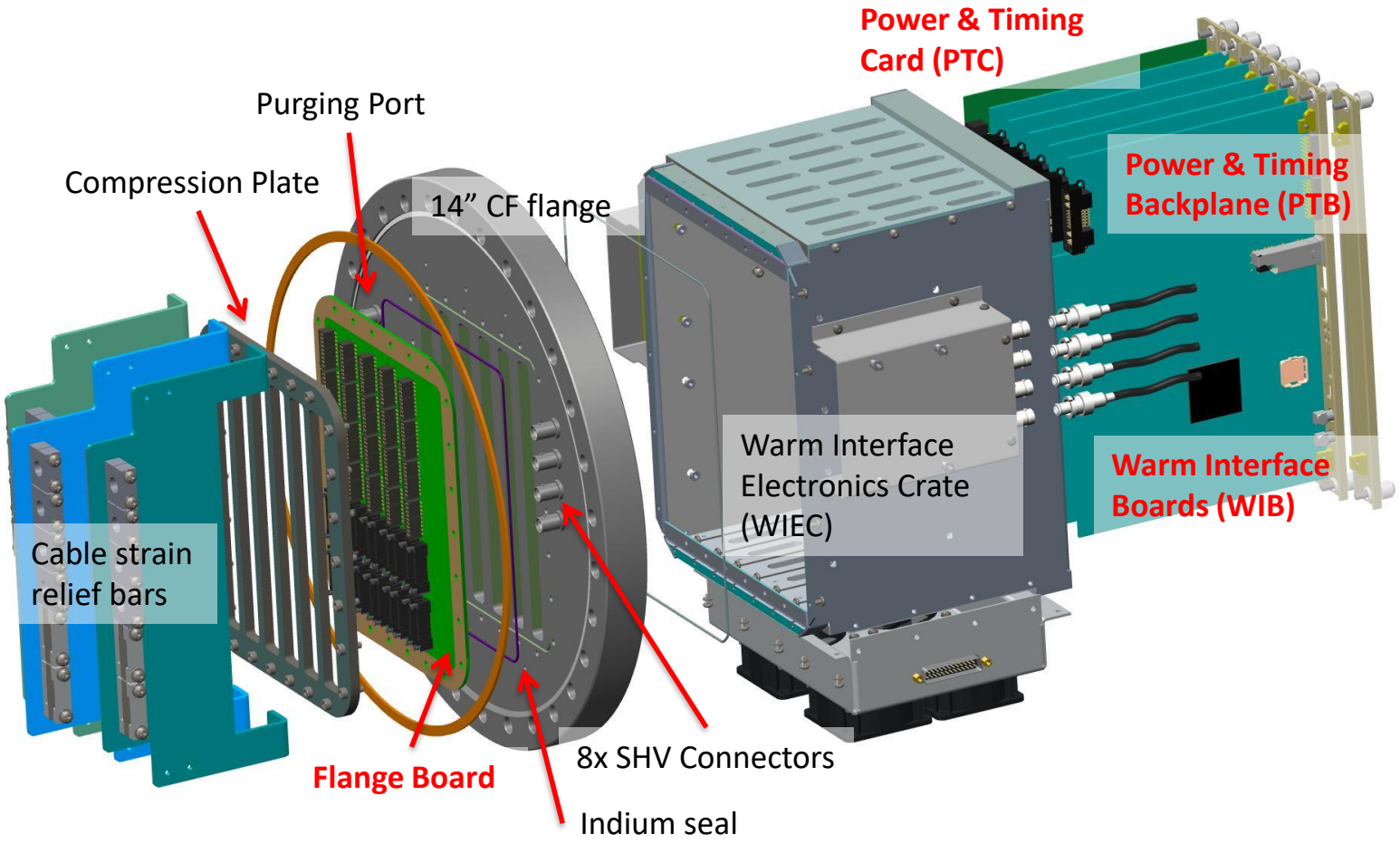
Signal Feed-through Assembly



Flange Board, WIB, PTC, PTB

Warm Side

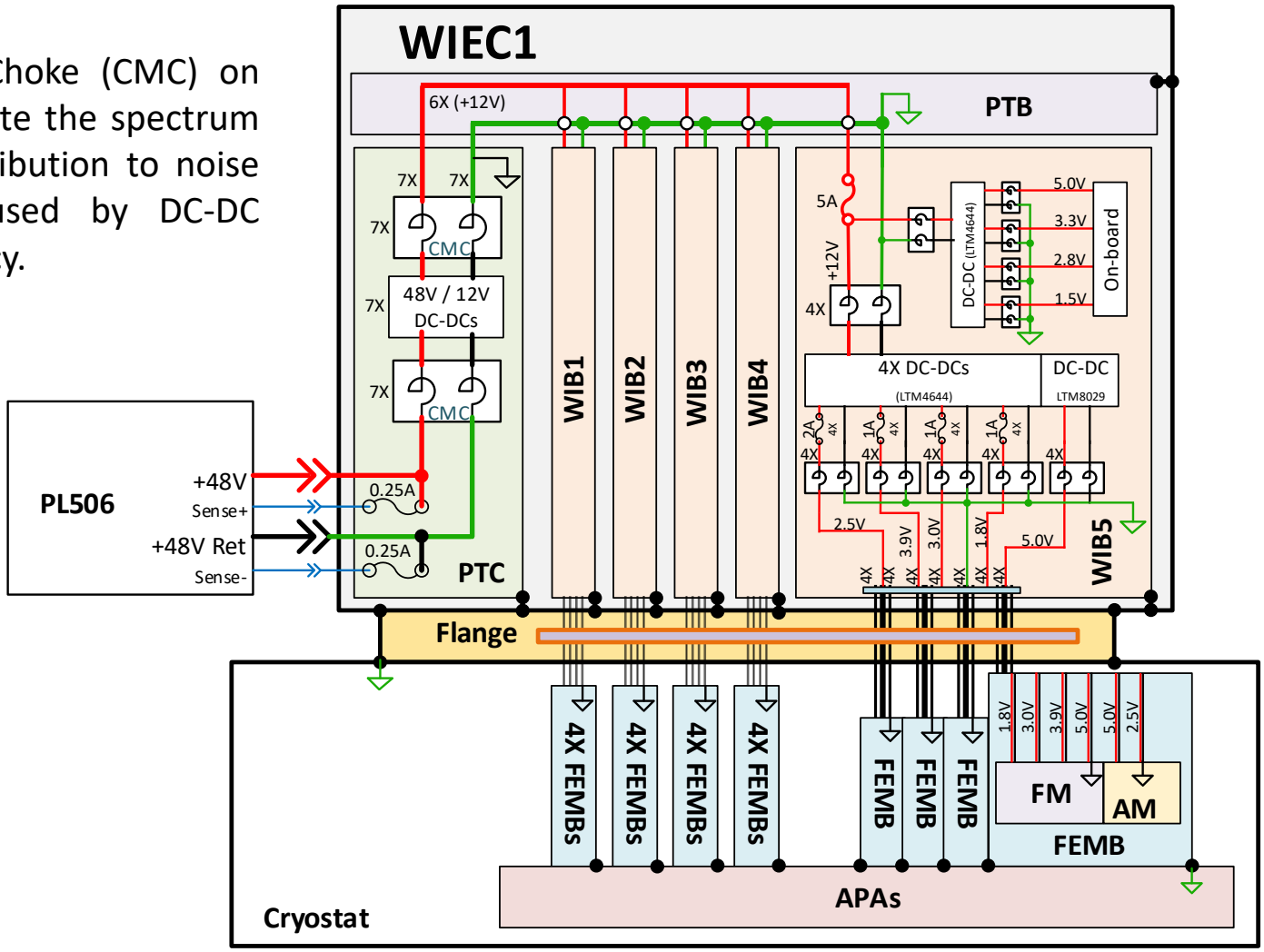
WIEC and Feed-through Assembly



CE flange and WIEC are a single assembled unit

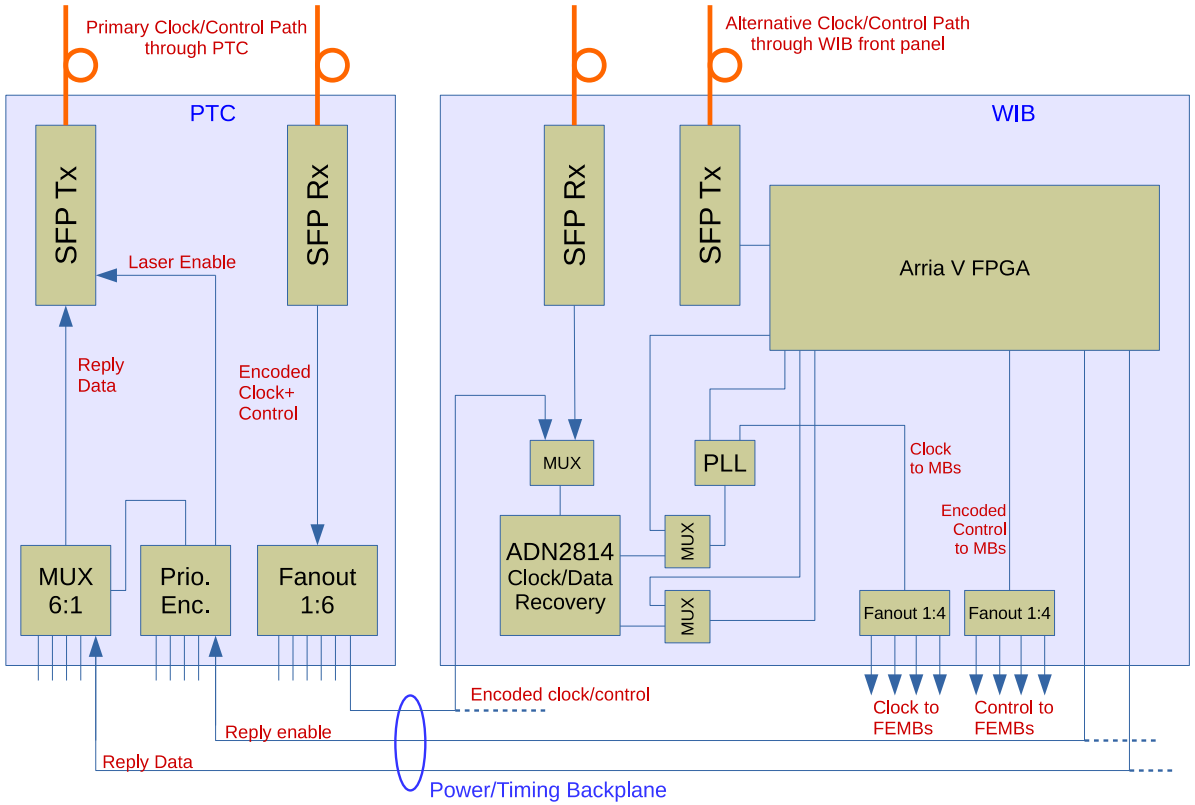
WIEC LV Power Distribution

Common Mode Choke (CMC) on PTC or WIB mitigate the spectrum spikes (little contribution to noise performance) caused by DC-DC switching frequency.



Cold cables is the only return path from Cold Electronics to Feedthrough + WIEC

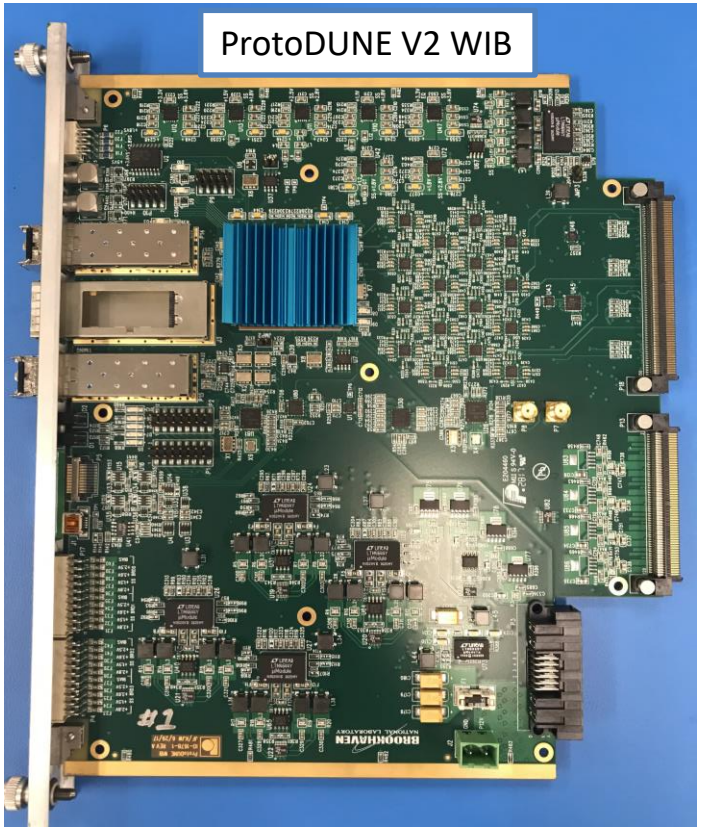
WIEC Timing and Command Distribution



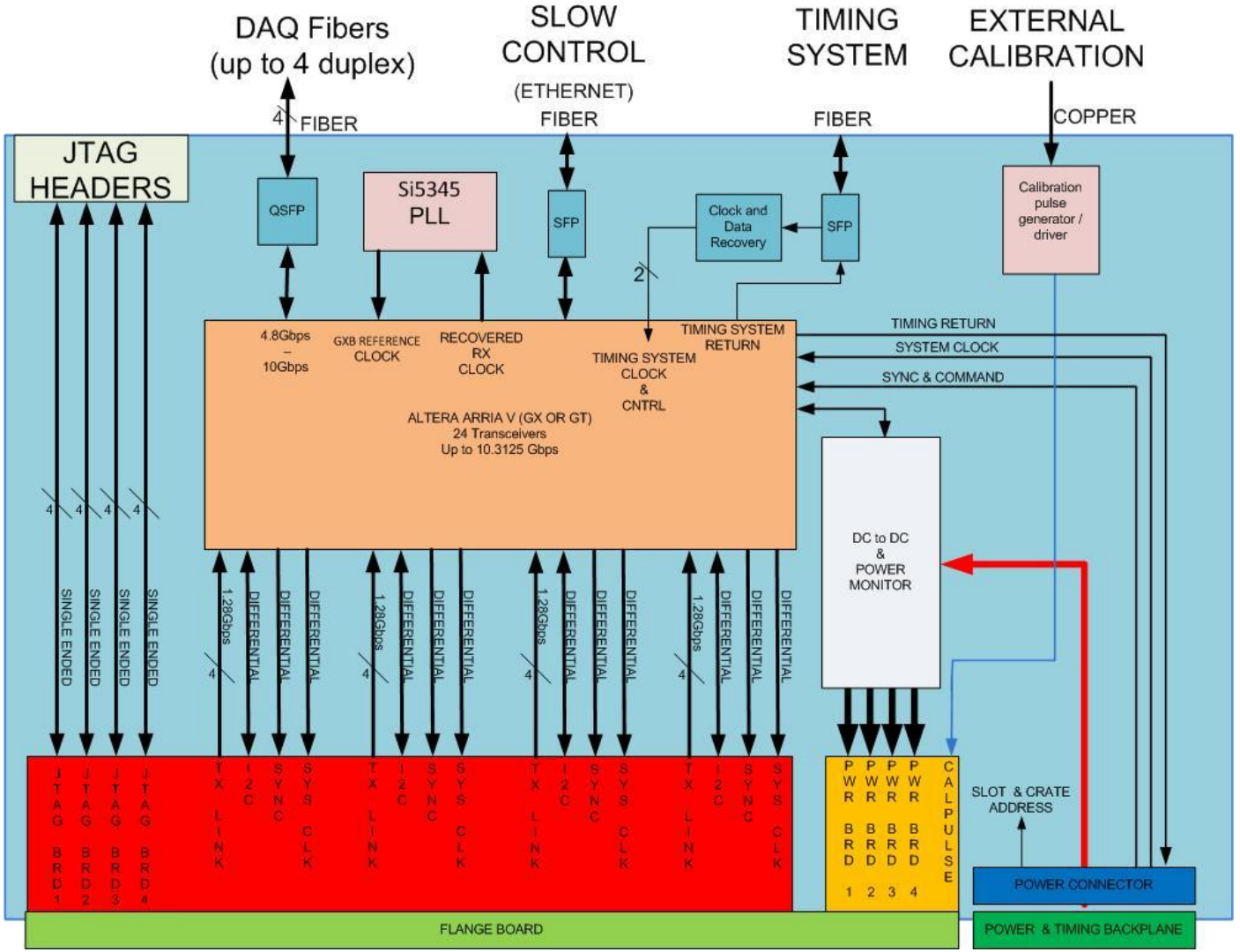
- Receives the timing and control from the 50 MHz encoded system clock
- Sends timing and control to FEMBs and receives high-speed TPC data over cold data cable and transmits it to the DAQ systems over fiber optical links

ProtoDUNE WIB

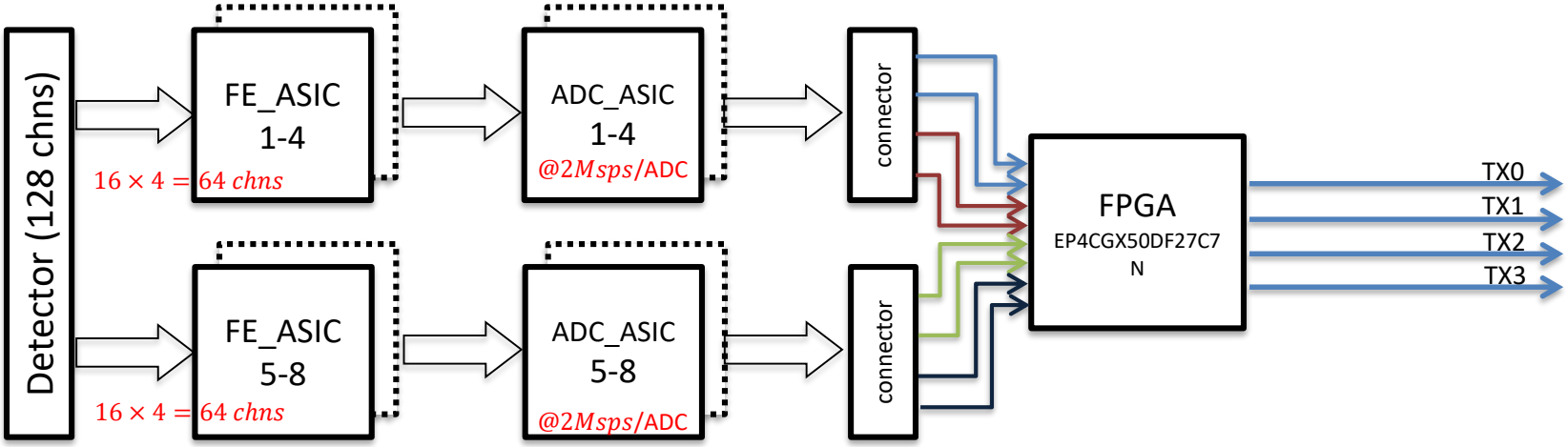
- Collaboration between BNL (hardware) and Boston University (firmware)
  - WIB schematics, layout, and BOM
    - DUNE-doc-3327-v3
  - WIB BU firmware repository
    - BU DUNE WIB
- Onboard power and control for up to 4 FEMBs
- Altera Arria V GT FPGA
- Inputs
  - 12V power and timing signal via passive PTB in WIEC
  - Alternate timing input also via front panel
  - High speed data links from FEMBs (16 x 1.28 Gbps)
  - JTAG for FEMB FPGAs
- Outputs
  - Clock / control to FEMBs
  - DAQ links (QSFP) up to 10 Gbps
  - Ethernet for configuration/slow control and real-time diagnostic readout
  - Analog monitoring for FE output if enabled

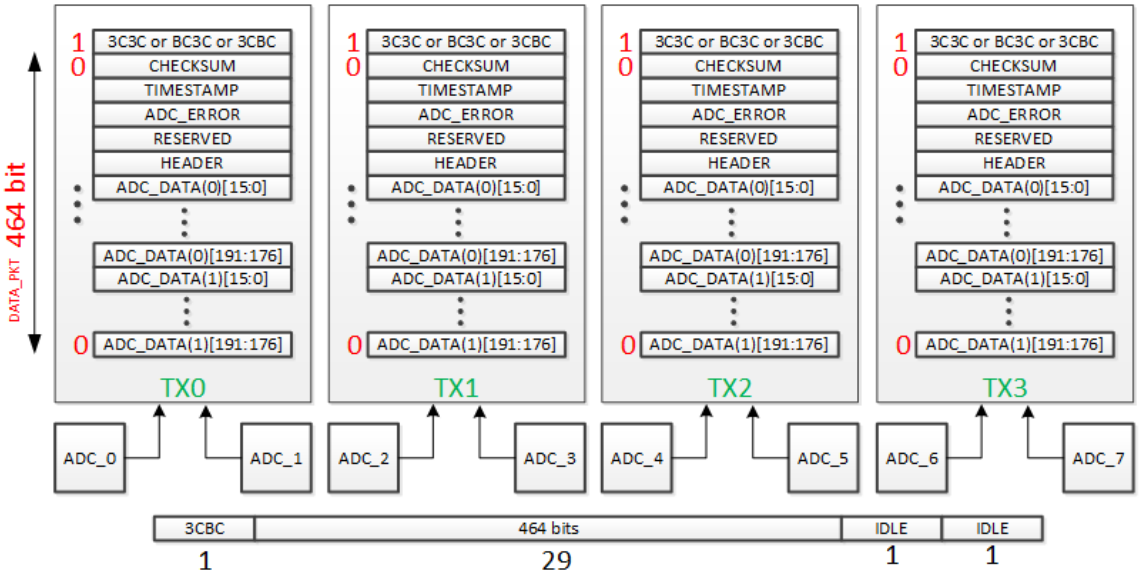


ProtoDUNE WIB



Data Flow from FEMB to WIB



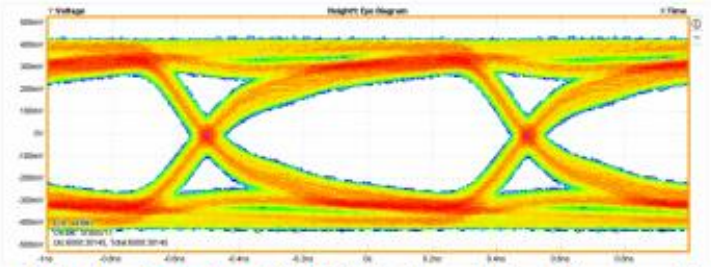


For each Tx lane

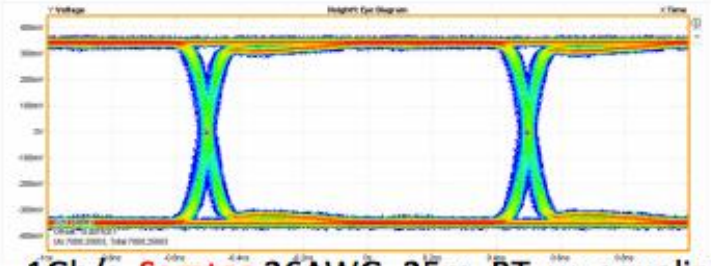
- Data rate of payload
  $29 \times 16bit \times 2MHz \times 1.25(8B/10B) = \mathbf{1.16Gbps}$
- Data rate of physical link
  $32 \times 16bit \times 2MHz \times 1.25(8B/10B) = \mathbf{1.28Gbps}$

Eye Diagrams with/without Equalizer

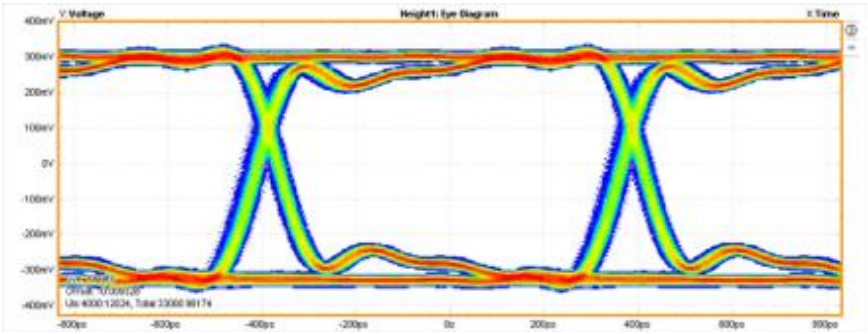
50 MHz encoded system clock for configuration and control



1Gb/s, Samtec 26AWG, 7m, RT, w/o equalizer
Height = 429mV, Tj = 152ps



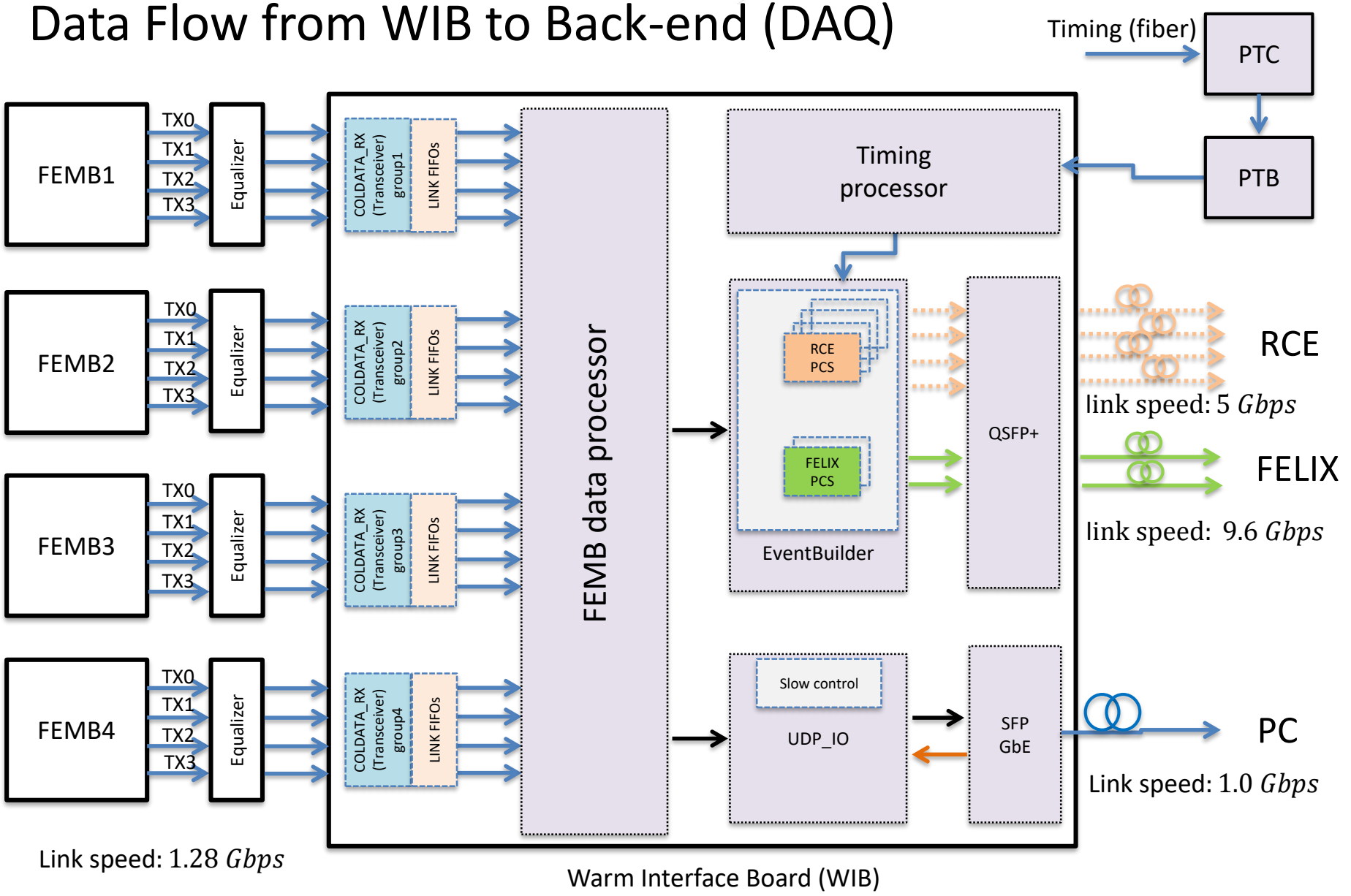
1Gb/s, Samtec 26AWG, 25m, RT, w. equalizer
Height = 628mV, Tj = 113ps



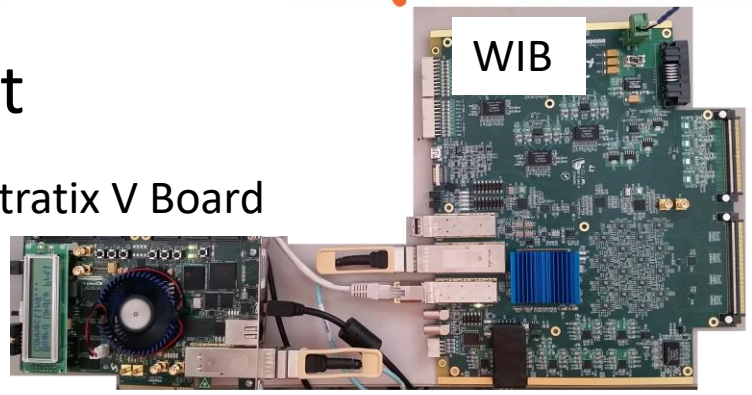
Eye diagram after 25m of ProtoDUNE-SP twinax at LN2 temperature

- BER test passed at 10^{-13} with and without active equalizer

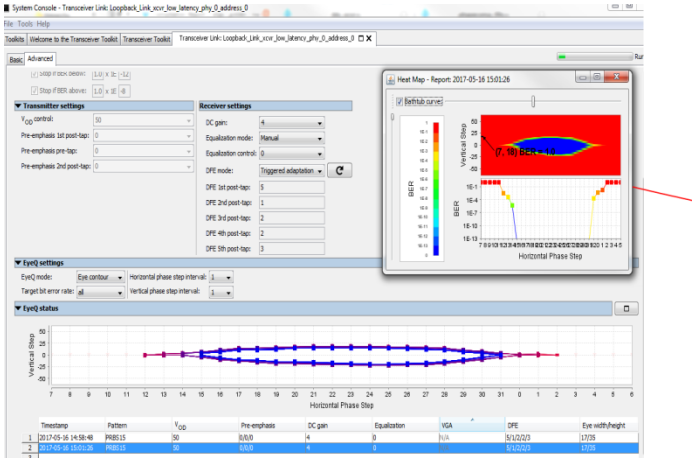
Data Flow from WIB to Back-end (DAQ)



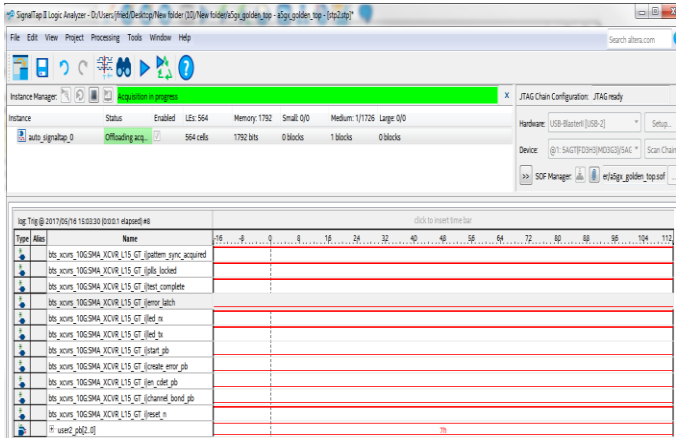
ProtoDUNE WIB 10 Gb/s Link Test



- Test setup
  - ProtoDUNE WIB V1
  - Altera Stratix V Development Board
- Test method
  - WIB transmitters verified by using Stratix V receivers + Altera transceiver tool kit.
  - WIB receivers verified by using Stratix V transmitter + PRBS checker running on WIB with the result displayed using Signal Tap.
- All links have been tested with BER < 10^{-13}

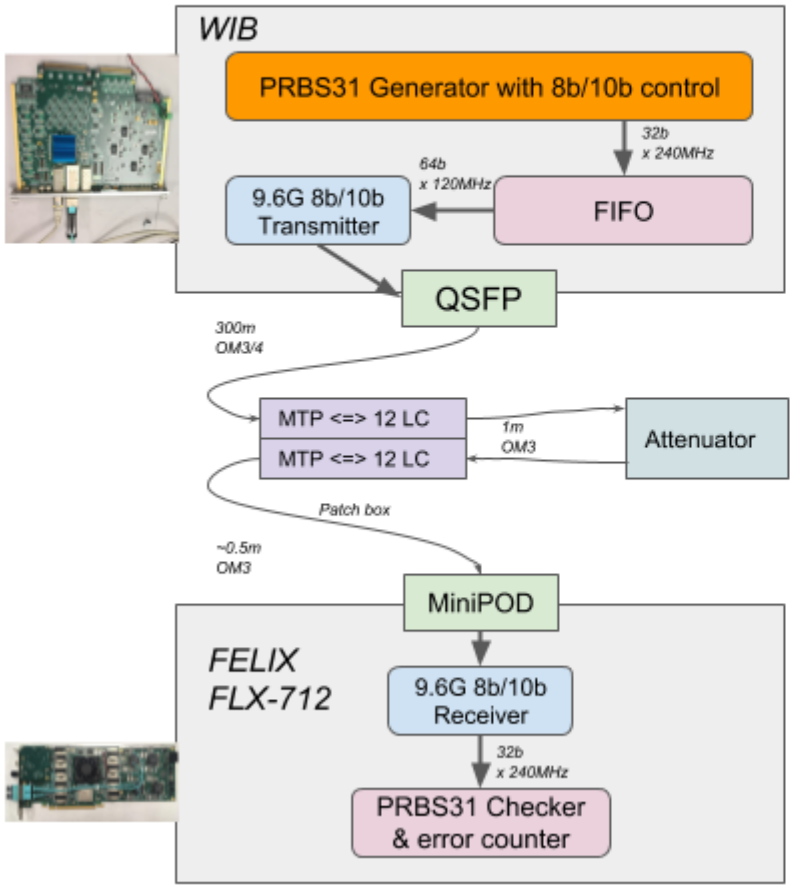


Altera transceiver tool kit



Signal Tap

Test Setup for the 300 meter fiber



- ***Motivation is to test whether 300m fibers work for 9.6 Gb/s from current WIB to FELIX, and to measure the margin of optical power.***
  - WIB FPGA: Altera Arria V GT 5AGTFD3H3F35I3
  - QSFP+: AFBR-79EIPZ
  - FELIX FPGA: Kintex Ultrascale XCKU115-2
  - MiniPOD: Avago AFBR-824Vxyz
- ***OM3 fiber is under testing. OM4 fiber to be tested.***
- ***Attenuator is used to measure margin.***
- ***Test data stream:***
  - 8b10b input is 32-bit PRBS31 with SOP, EOP and several IDLEs.

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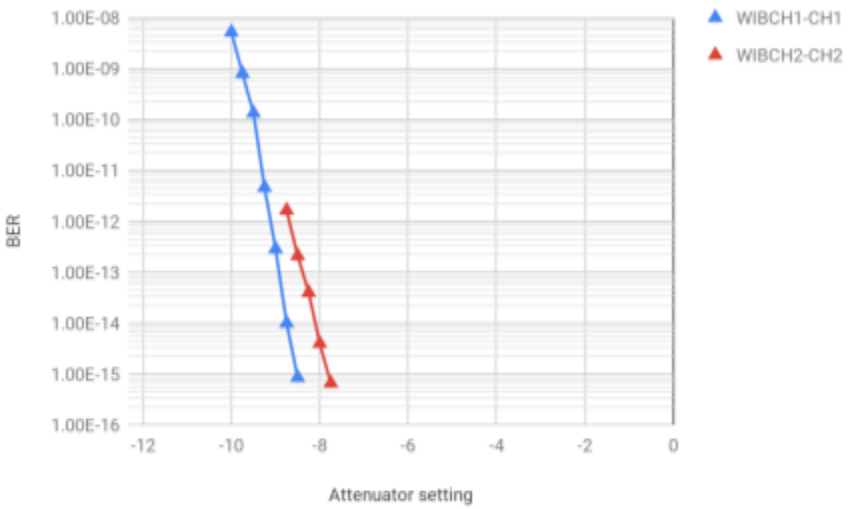
BER (Bit Error Rate) test



- ***Two links are measured:***
  - WIB CH1 -> FELIX CH1
  - WIB CH2 -> FELIX CH2
- ***Similar trend for the two curves.***
- ***The margin for BER<10^{-15} is about 8.5 dB and 7.75 dB.***
  - Note: compared to connect the two LC connectors on patch box directly, the insertion of attenuator will introduce about 0.7~0.8 dB attenuation even setting is 0 dB.
  - If without attenuator, margin will be about 9.25 dB and 8.5 dB.
- ***To do: test OM3 300m, OM4 300m and compare results with OM3 20m.***
- ***Conclusion (preliminary): WIB to FELIX link can run stably with 300 meter OM3 fiber at 9.6Gb/s with good margin***

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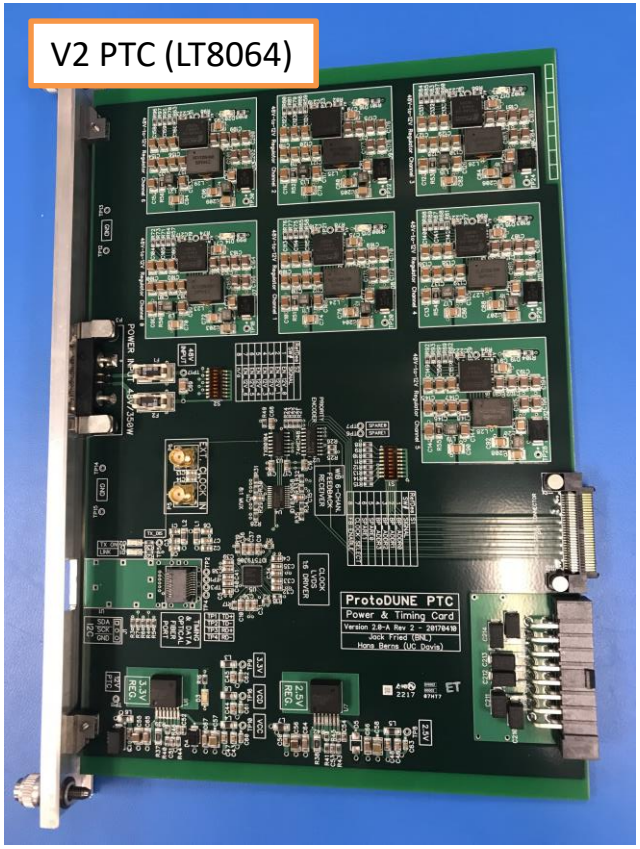
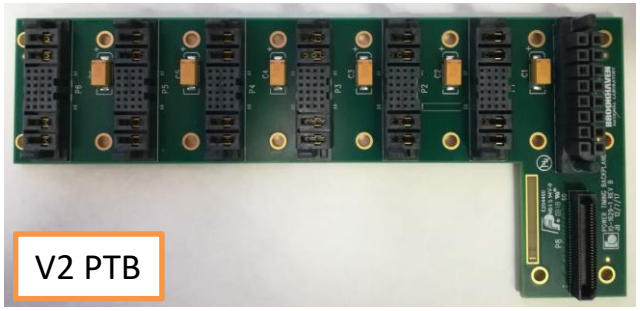
PTC/PTB

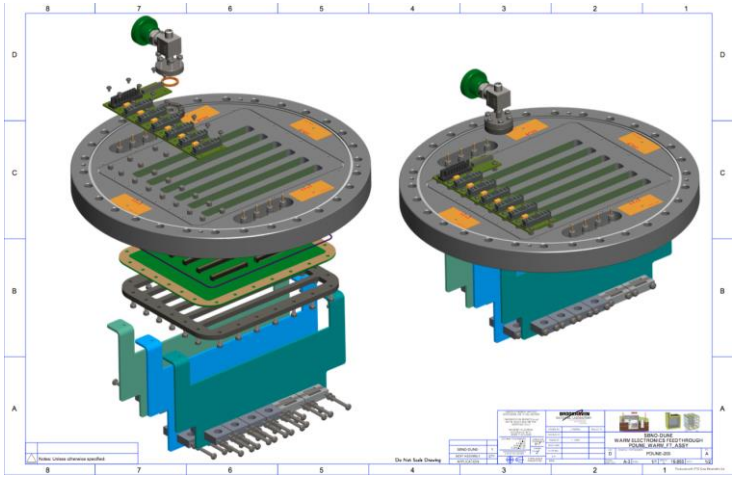
- Power and Timing Card (PTC)
  - Schematics, layout, and BOM
    - DUNE-doc-3327-v3
  - Design collaboration between BNL and UC Davis
    - PTC with Vicor PI3456 DC-DC module
    - PTC with Linear LTM8064 DC-DC module
    - LTM8064 PTC shows slightly less noise than PI3456 PTC
  - Inputs
    - 48V power from DC supply
    - Timing signal (including return path from individual WIBs)
  - Outputs
    - 12 V and timing signal fanout over passive backplane
    - Crate location for WIB IP address
- Power and Timing Backplane (PTB)
  - Schematics, layout, and BOM
    - DUNE-doc-3327-v3
  - Passive components

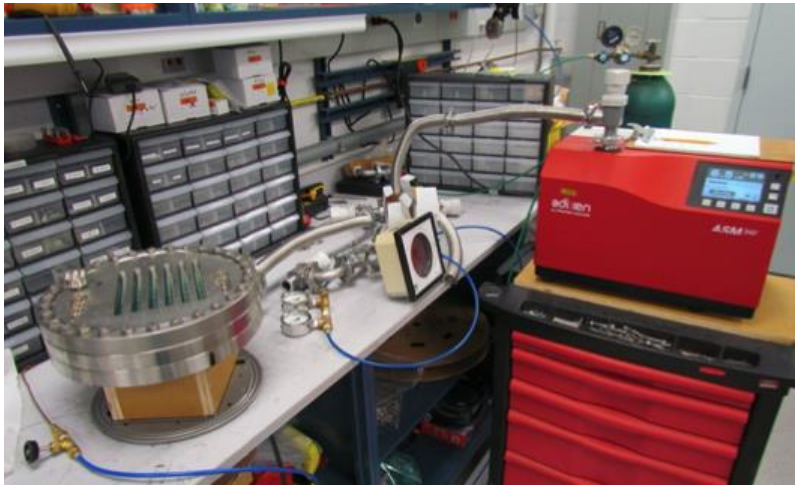




Flange Board

- Flange Board
  - Schematics, layout, and BOM
    - DUNE-doc-2777
  - Low impedance connection to cryostat ground at flange
  - All cable connectors are surface mount components
  - Blind vias
  - Indium wire seal is used between the PCB board and flange to ensure good electrical contact (grounding)

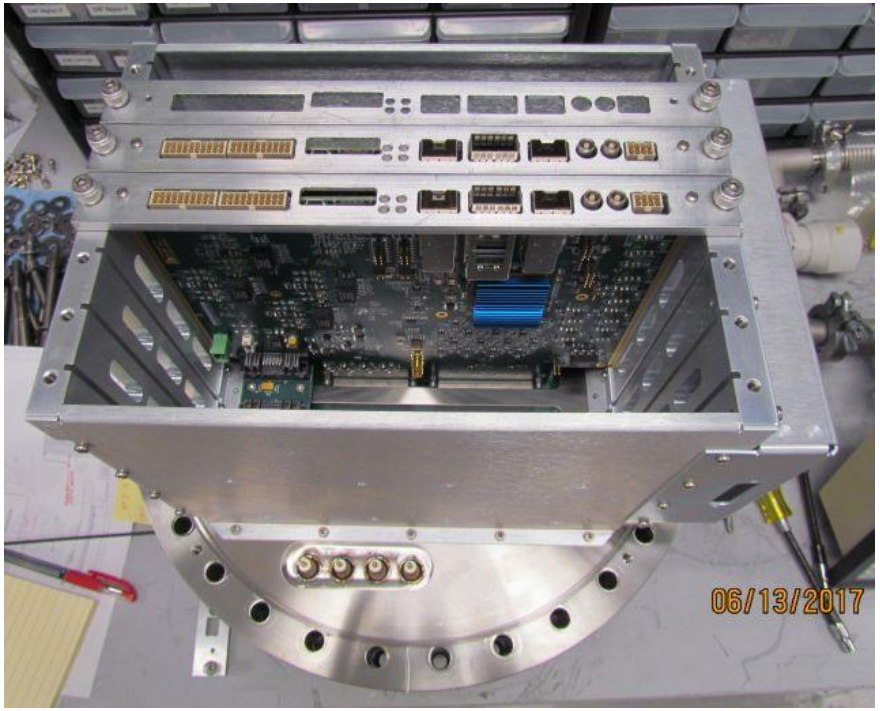




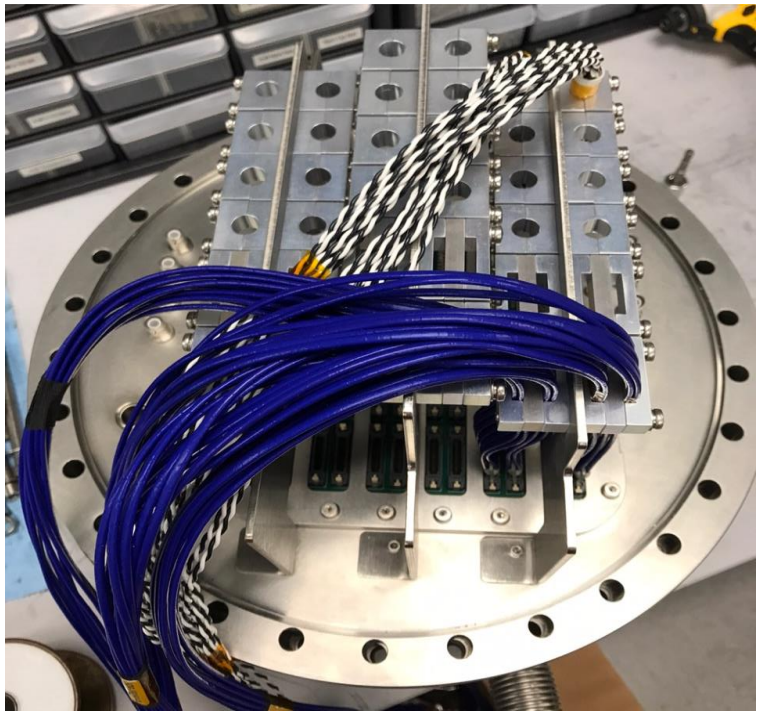
- Withstands > 20 PSI pressure differential on cold side
- Leakage rate < 10^{-9} mbar L/sec with 5 PSI differential pressure applied to cold side

CE Flange and WIEC

- CE flange: provides electrical connection from cold cable to warm electronics via flange PCB and cold-side cable strain relief
- Warm Interface Electronics Crate: RF shielding for warm electronics, only connections outside of crate are via fiber optical links

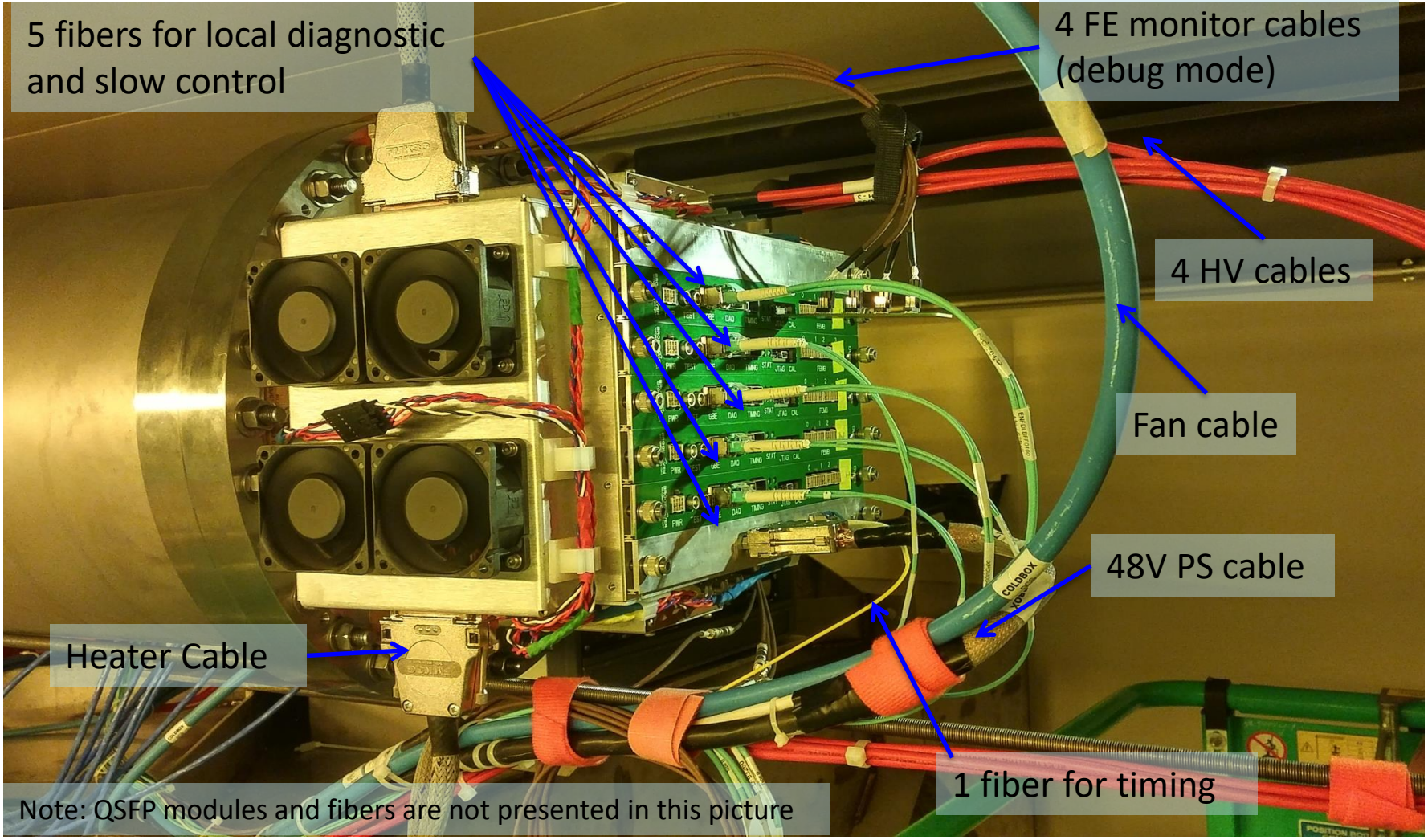


Crate with 2 WIBs on warm flange side



Cables + strain relief on cold flange side

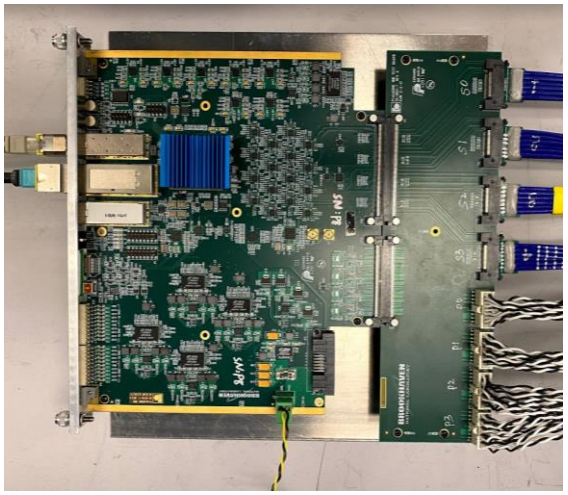
Configuration of WIEC for Cold Box

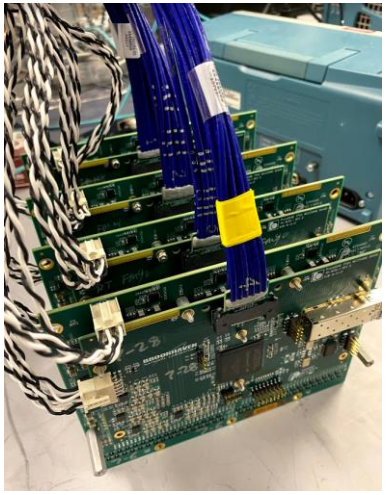


ProtoDUNE fibers are ~50m long from cryostat to DAQ barracks

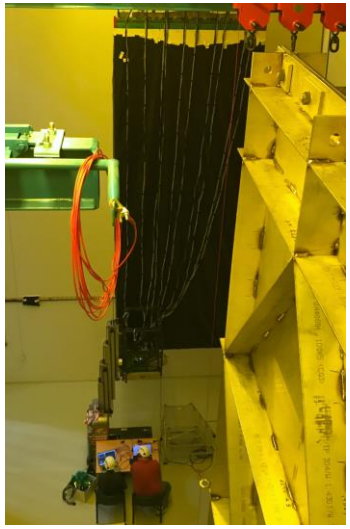
ProtoDUNE-SP CE Testing

- WIB standalone read-out was used to test all production FEMBs at BNL and FEMB installation checkout at CERN
  - WIB + cable adapter connected to DAQ via GbE
  - Laptop DAQ with LabVIEW (real-time monitoring) or Python scripts
  - Can be positioned at anywhere when FEMB are being installed at the top of APA





WIB standalone read-out supports up to 4 FEMBs

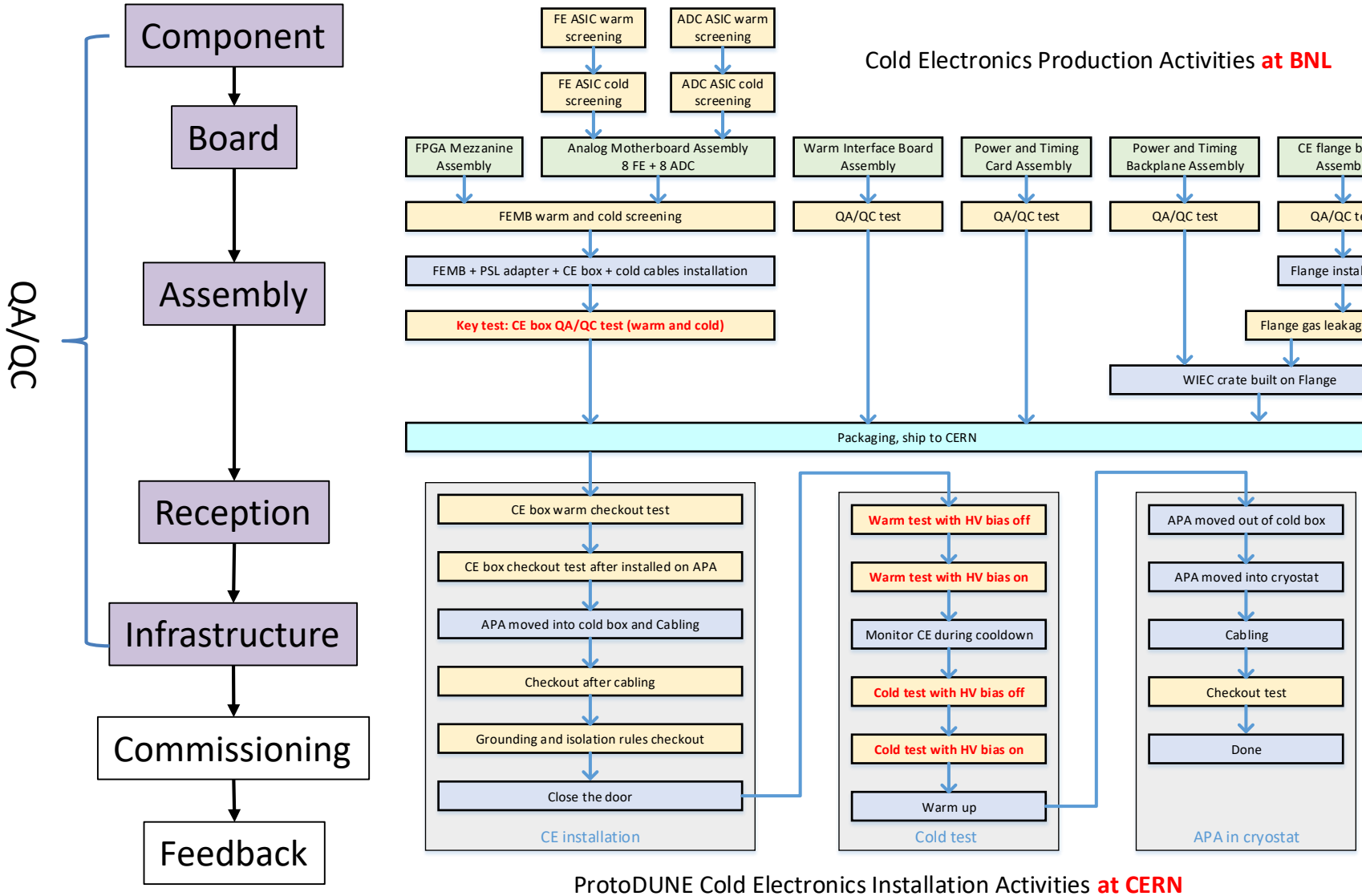


On Floor

On Scissor Lift

FEMB checkout with WIB test stand

Procedure for CE Production and Installation



Cold Electronics Production Activities **at BNL**

ProtoDUNE Cold Electronics Installation Activities **at CERN**

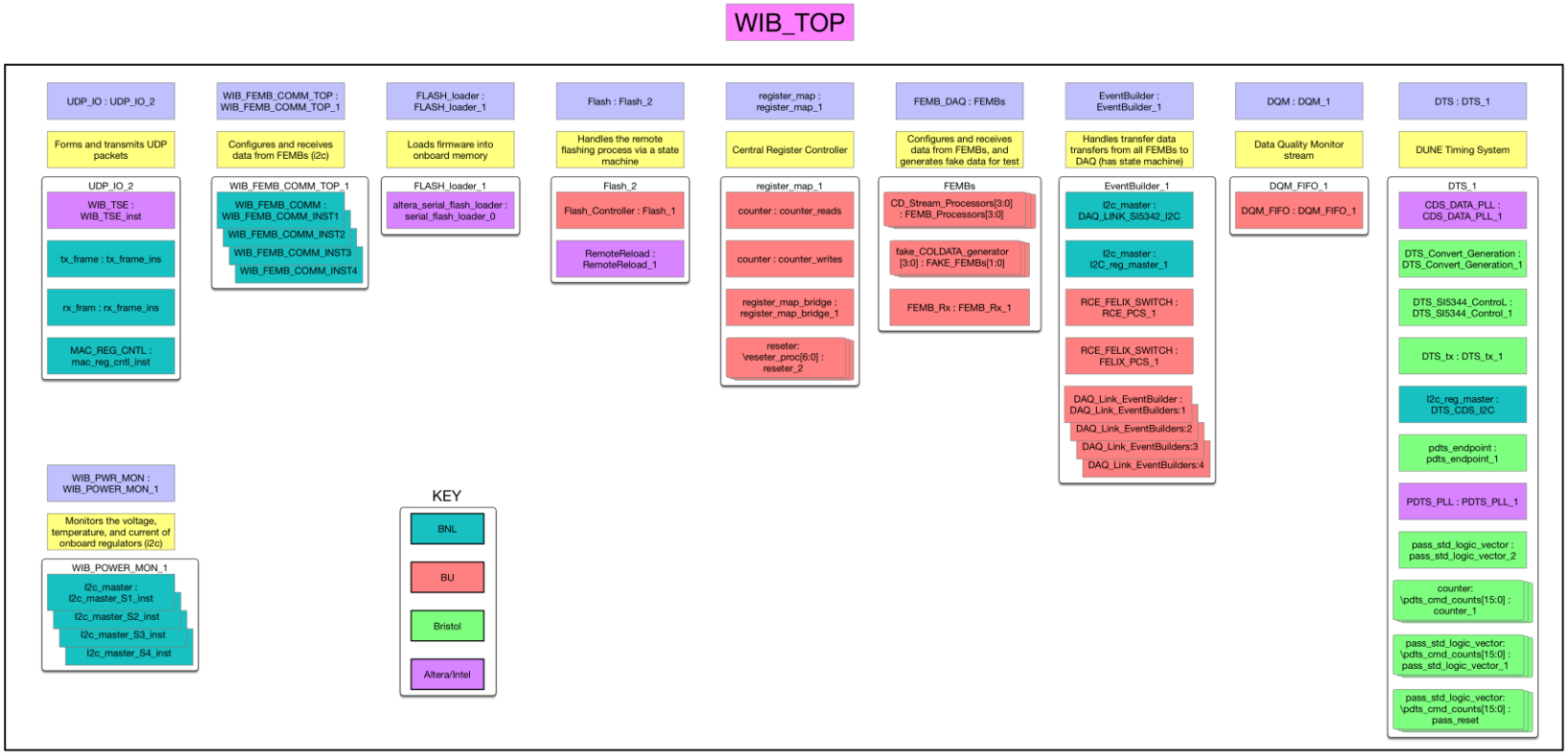
WIB/PTC/PTB/Flange QC Tests

- WIB QC test at BNL
  - Post-assembly visual inspection, FW programming, initialization checkout (voltage, current, connectivity), FEMB operation, etc.
  - 10 Gb/s link test and timing path check
  - All 35 pieces in the production batch passed QC test
    - 3 of 35 WIBs passed QC after rework
      - Failure mode: assembly mistakes, dysfunction QSFP, improper handing
- PTC QC test at BNL
  - Post-assembly visual inspection, power checkout, Timing path checkout
    - PTC with Vicor PI3456 DC-DC modules have yield issue
      - 3 out of 10 pcs are good, 7 pcs with one or more broken PI3456 chips
    - All 10 pieces of PTC with Linear LT8064 DC-DC modules are good
- PTB & Flange board QC test at BNL
  - Connectivity checkout
- Post-installation test at CERN
  - Read out of system via warm interface electronics tests all aspects of chain
  - No failures at 6 feed-through/flange assemblies for ProtoDUNE and 1 for Cold box

BU FW vs. BNL FW

- BU FW
  - Verified and compatible with ProtoDUNE DAQ: required for data-taking since it has the block to interface to the timing system
  - Limited local diagnostic features
    - Can’t peek high speed FEMB data stream through slow control
  - Dedicated software (BUTool) is required to work with BU FW
    - Can peek WIB-DAQ links via BUTool
  - Organized by version control software
- BNL FW
  - Real time streaming over UDP through GbE for data of an ASIC (16 channels)
  - Flexible, easy to use, support any programming language
  - FE for FELIX readout is implemented but never tested with ProtoDUNE DAQ
  - No strict version control is applied
- Drawback of UDP protocol in the complicated DAQ network
  - UDP package loss can cause failure of WIB/FEMB configuration

BU Firmware Top View



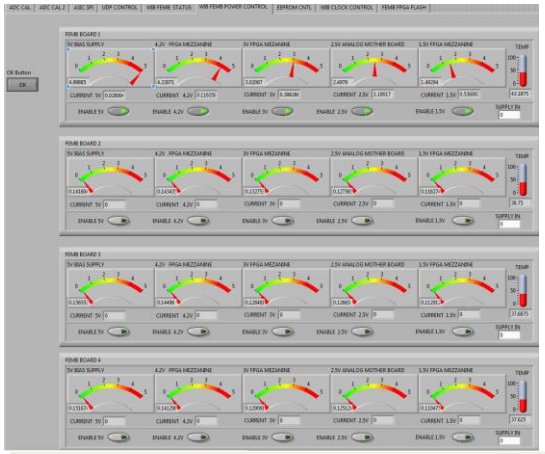
BUTool and Monitoring Software

- BUTool developed by Boston to interface to WIBs
  - Low level UDP over GbE for communication
  - Higher level software for WIB/FEMB configuration
- Real time command line interface to WIBs and FEMBs
  - Primary WIB debugging tool during DAQ configuration and data-taking
- Interface to DAQ
  - Subset of BUTool libraries linked into artDAQ (LSU work)
  - Allows artDAQ Boardreaders to configure WIBs/FEMBs, start CE sending data
- Interface to CERN DIM (monitoring)
  - Allows DIM to read WIB registers for onboard WIB monitoring (MSU work)
- Currently being developed as WIBTool at FNAL for SBND (FNAL, UFlorida, IIT work)

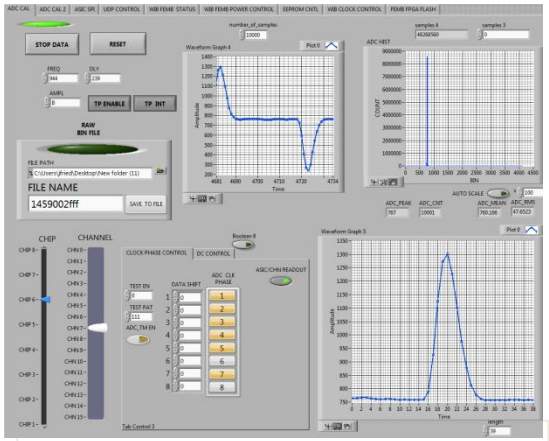
```
[dunecet@protodune-daq02]$ BUTool.exe -X scripts/
config_WIB_FNAL_RCE_default.script
Registered device: WIB
Configuring WIB: FNAL RCE with default FEMB config
SYSTEM.SLOW_CONTROL_DND: 0x00000001
Checking if locked on PDTS
Need to reset for PDTS
Configuring DTS
Using timing group 0x0
Using PDTS for DUNE timing.
Configuring clock and data separator
CDS frequency 241360000.000000
CDS LOL=0 LOS=0
Configuring SI5344.
[================================================]
 ################################################
Setup PDTS.
Try   1.   PDTS state: W_LINK (0x1)
Try   2.   PDTS state: W_ALIGN (0x4)
Try   3.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_PHASE (0x6)
Waiting for phase alignment.   PDTS state: W_RDY (0x7)
PDTS state: RUN (0x8)
Resetting DAQ Links
1
2
3
4
Process done
```

BNL FW with powerful local diagnostics

- **Utilize all engineering development tools used at BNL**
  - Can plug a laptop containing BNL tools into the Ethernet switch or directly into a WIB
  - Can be used simultaneously with DAQ system
  - Will simplify debugging of entire system
- Online monitoring / debugging features
  - Monitor and control FEMB voltages and currents
  - Can monitor FEMB ASIC data sent over high-speed link
  - Read and write FEMB registers
  - Program and verify FEMB FPGA flash memory
  - Can select to use on-board or system clock
  - Peek at high speed data link in real time over slow control
    - **Can monitor one ASIC worth of data**
  - Can generate high speed test data sent to DAQ
    - PRBS test pattern
    - Counter
    - Channel, Crate, Slot address encoded to aid in mapping
  - Can generate calibration pulse for FEMB

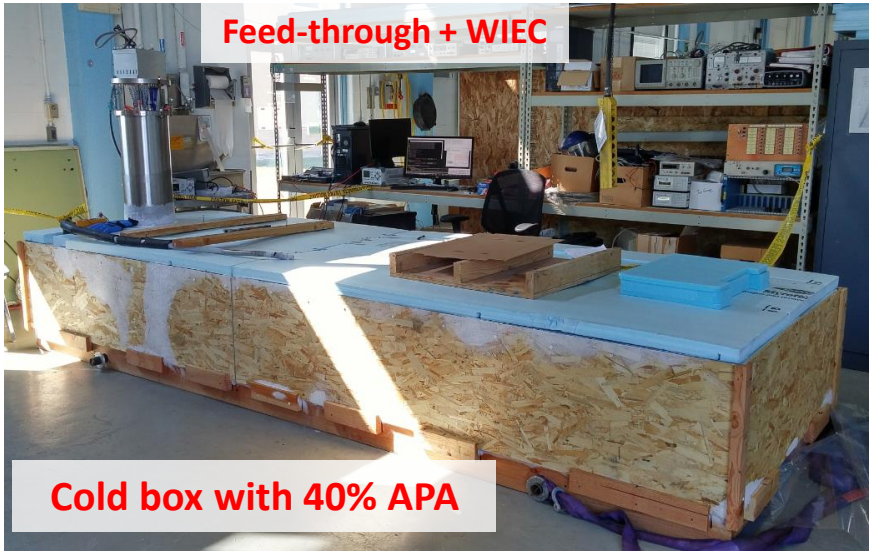


Power Monitor & Control

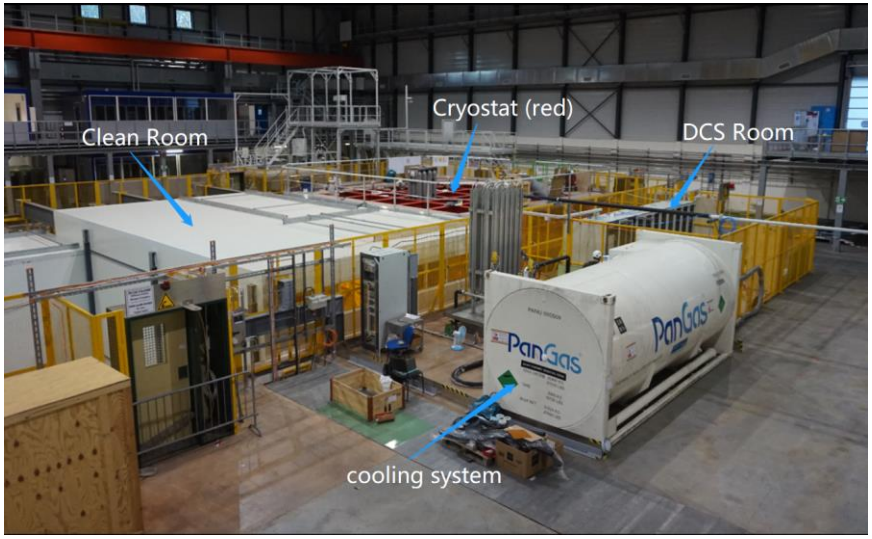


Real-time channel data

Integration Test Stands at BNL and CERN



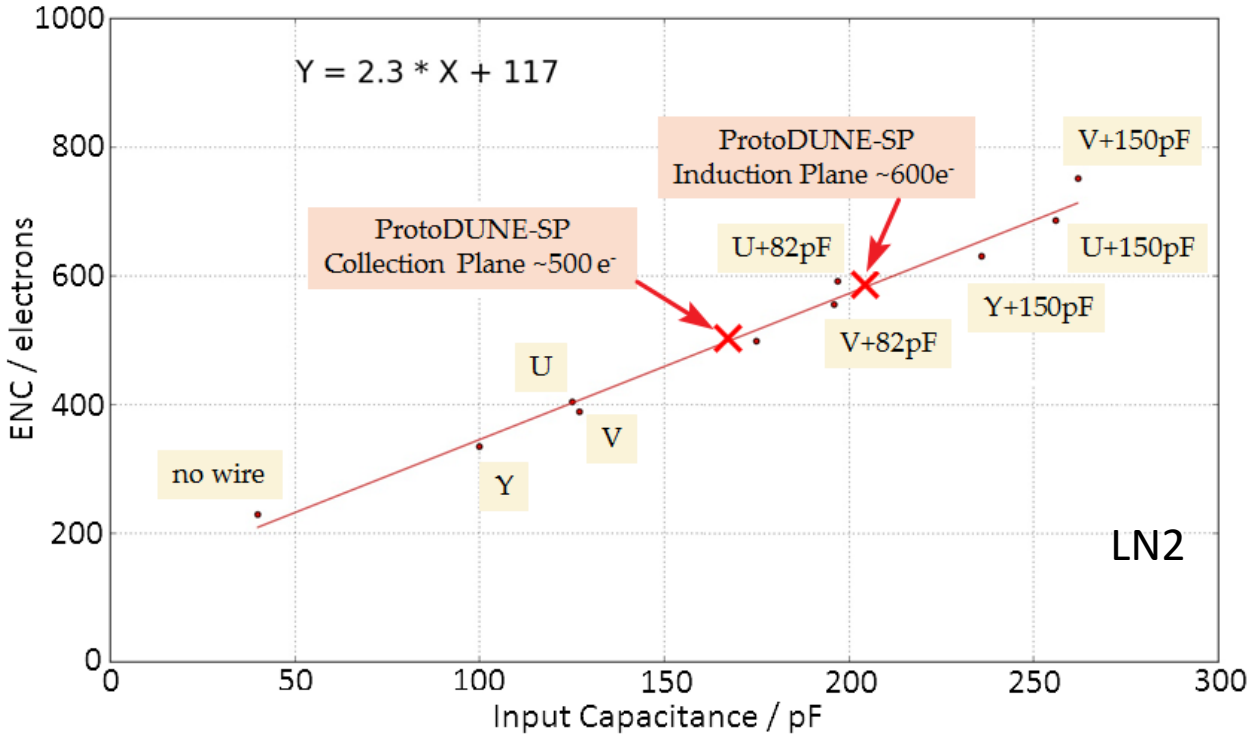
40% APA: 2.8m x 1.0m, 1024 wires



- Warm test
- Cooling down
- Cold test (~150 K)
- Warming up
- Warm test

DUNE APA: 6m x 2.3m, 2560 wires

ENC Projection Based on 40% APA



- 40% APA
  - U/V wire: 4.0 m
  - Y wire: 2.8m

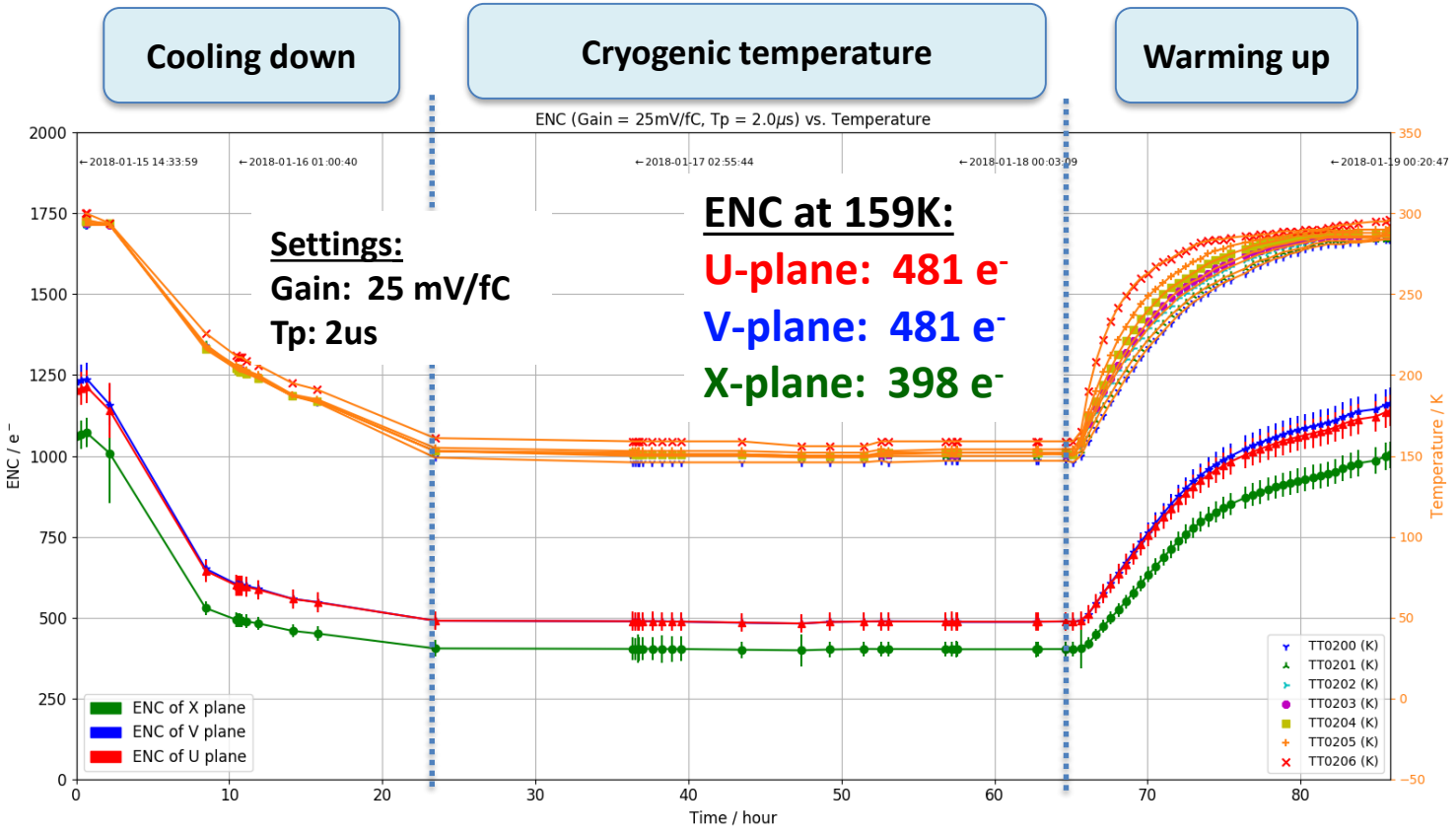
Note: 82pF and 150pF mica capacitors are added on some wires

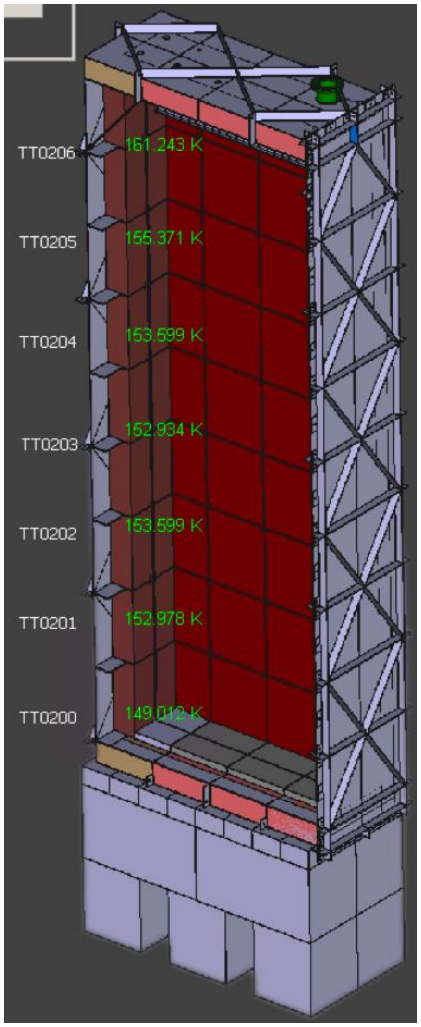
- ProtoDUNE APA
  - U/V wire: 7.39m
  - Y wire: 6.0m

- DUNE Far Detector
  - Same APA as ProtoDUNE-SP
  - Threshold: 1,000 e^-
  - Goal: as low as possible

CERN Cold Box Integration Test

APA2 (2018-01) Cold nitrogen gas with lowest temperature reached ~ 159K





1. Uniform gain (77 e-/bin) is applied for calculating noise of all channels
2. HV Bias voltages were off
3. Data are read out chip by chip over local diagnostic GbE port.

Lessons Learned

- System design and testing
  - A multiple phase QA/QC process, from component through system level, was necessary for excellent system performance
- WIB firmware and software development
  - Unavailabillity of firmware design engineers, especially at the detector site, caused some delays in WIB integration
    - BNL firmware was used for initial APA testing at CERN while WIB-DAQ interface was under development
  - Detailed understanding of software tools by multiple collaborators (LSU, MSU, BU, BNL) was necessary for successful integration
- A better and faster way to upgrade WIB FW remotely
  - Due to lack of alternate data path in BU firmware, BNL FW is required from time to time to cross-check the cold electronics performance during the commissioning
    - FW update speed half an hour BU -> BNL, 3 minutes BNL -> BU
- Periodically unstable data communication with UDP
  - A reliable data communication (such as TCP/IP) should be required for DUNE WIB
    - New study to use Xilinx Zynq+ FPGA for WIB, see Jack's talk.

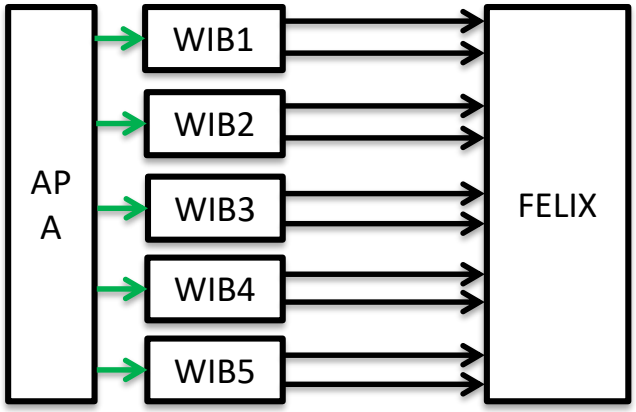
Summary

- The APA + CE + Faraday Cage/Feedthrough with Warm Interface Electronics should be treated as an integrated whole and installed as such
- Warm interface electronics is also playing a key role in excellent detector performance along with cold electronics inside cryostat
  - Low contribution to detector noise
  - Superior data throughput
  - Local diagnostics to easy access cold front-end electronics
  - Controllable isolation and grounding rules
- A multiple phase QA/QC process, from component through system level, was necessary for excellent system performance

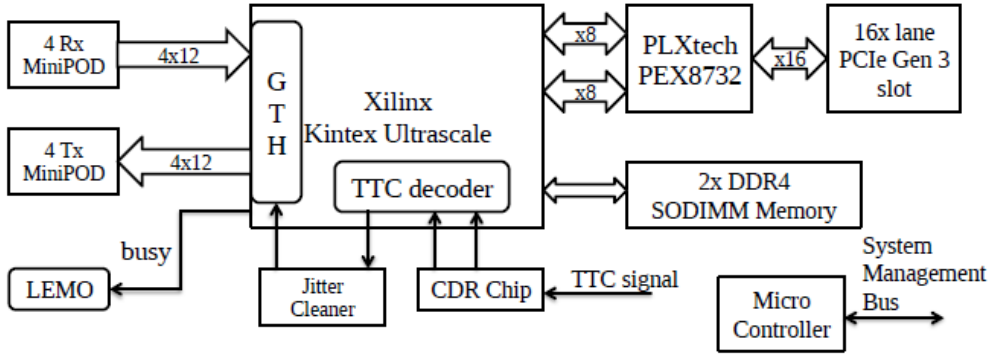
BACK UP

ProtoDUNE-SP WIB-FELIX Readout Test Stand at BNL

Though BNL WIB firmware with FELIX communication capability hasn't been verified in ProtoDUNE, it proves the communication between WIB and BNL-711 PCIe card is stable.



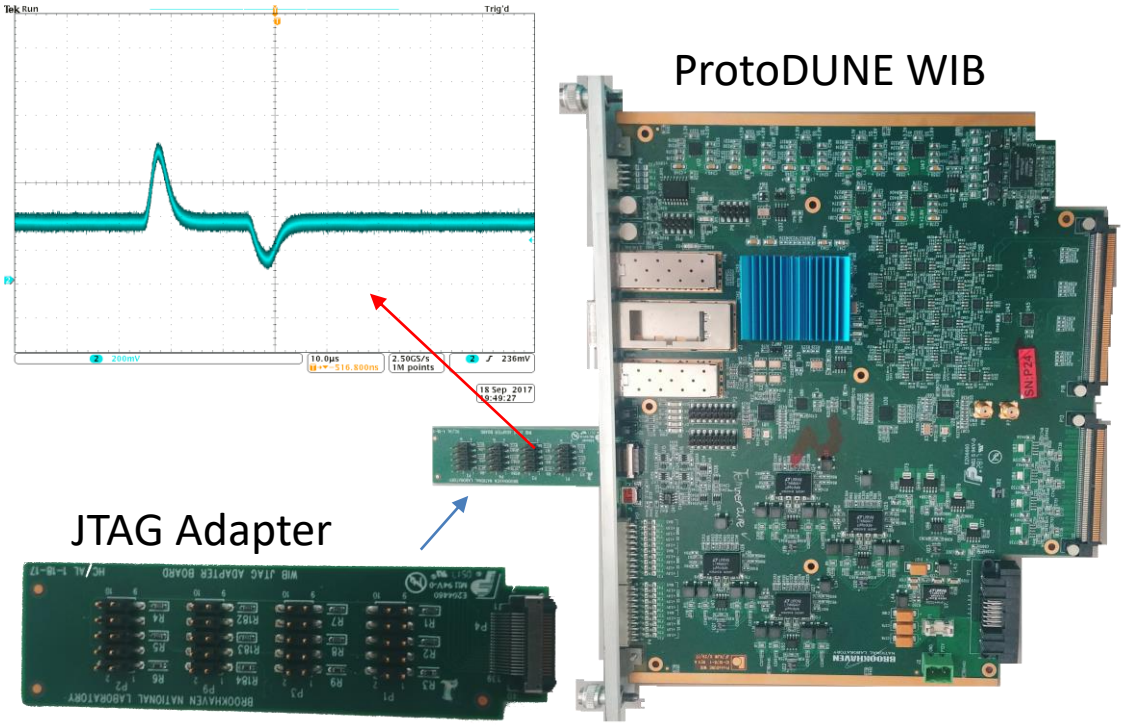
FULL mode: @9.6 Gbps per link



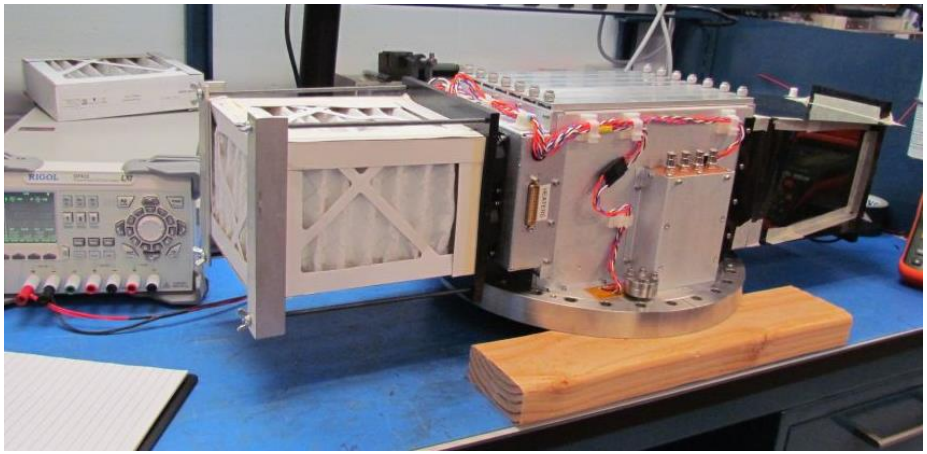
- Xilinx Kintex UltraScale FPGA
- 16-lane PCIe Gen3.0, throughput tested ~101Gb/s
- 48 optical transceivers (MiniPOD)
- On-board timing interface

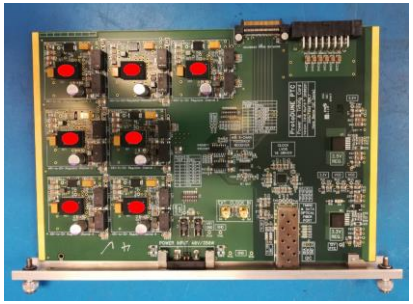
Analog Monitoring

- Can monitor FE output, temperature sensor, and bandgap reference
  - Enable monitoring function attenuates the amplitude of FE output
- Analog monitor over 7m cold + 15m warm of cable
- All 128 Channels on FEMB are accessible



WIEC Air Flow with Air Filters





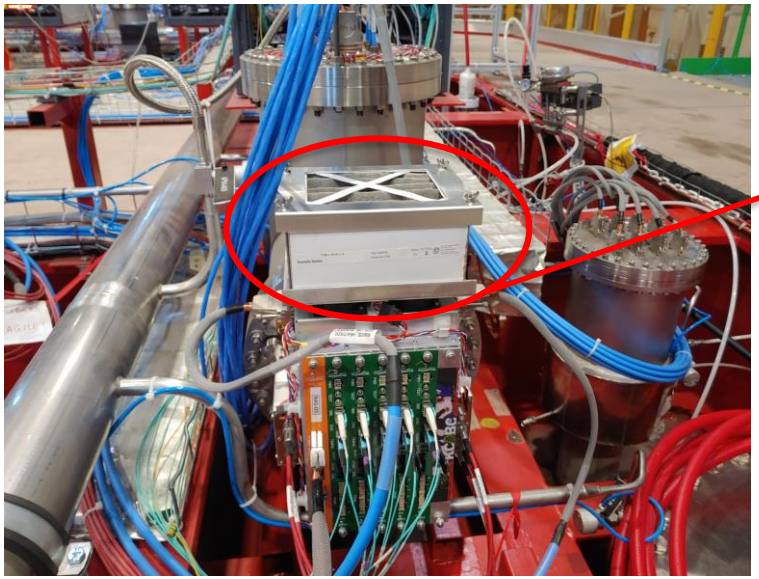
Tests using the actual WIEC, 6 WIBs & 1 PTC, 4 fans					
7.375" x 5.25" x 4" MERV-8 filter		7.375" x 6.25" x 4" MERV-11 filter		7.375" x 6.25" x 4" MERV-13 HEPA filter	
VDC	CFM	VDC	CFM	VDC	CFM
24	30.4	24	30.8	24	24.8
23	30.4	23	30.8	23	24.8
22	30.4	22	30.8	22	24.8
21	30.4	21	30.8	21	24.8
20	30.4	20	30.8	20	24.8
19	29.5	19	30	19	24.4
18	28.1	18	28.7	18	23.3
17	26.8	17	27.4	17	22.2
16	25.4	16	26.1	16	21.1
15	24.2	15	24.8	15	19.9
10	16.9	10	16.9	10	13.8

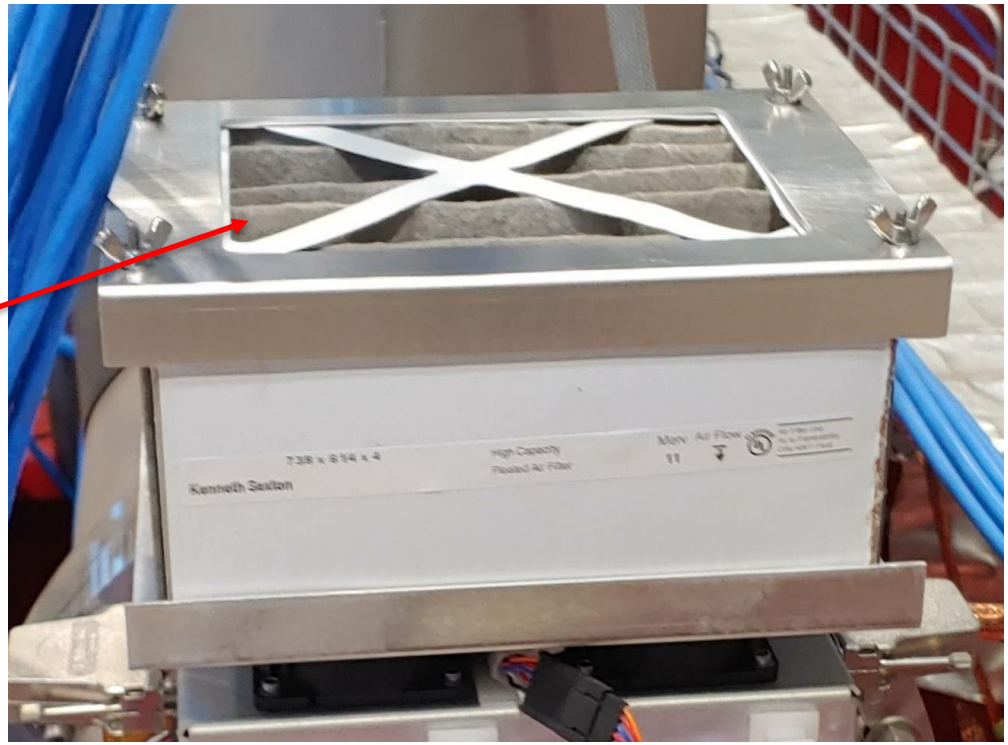
MERV 8 & 11 filters flow virtually the same. The MERV 13 (HEPA) filter restricts airflow about 20% less

Filtration Media (thickness & filter quantity)	Volts (DC)	Flow in CFM	WIB Chip Temp C						PTC Chip Temp						
			1	2	3	4	6	7	5	8	9	10	11	12	13
4" Merv 8	24	31.4	48.2	31.1	46.2	46.8	46.7	47.1	28.6	38	42.9	52.3	44.2	49.4	46.6
4" Merv 8	20	31.4	48.2	31.1	46.2	46.7	46.7	47	28.6	38	42.9	52.4	44.3	49.5	46.6
4" Merv 8	15	25.2	50.4	32.9	48.7	49.4	49.1	49.4	29.8	40.8	45.9	55.9	47.5	53	49.7
4" Merv 8	10	17.7	54.6	36.9	52.7	54.2	53.4	53.8	32.8	46.5	52.1	63.4	54.1	59.6	55.3

Concluded by Kenneth Sexton: the MERV 11 filter is the best choice

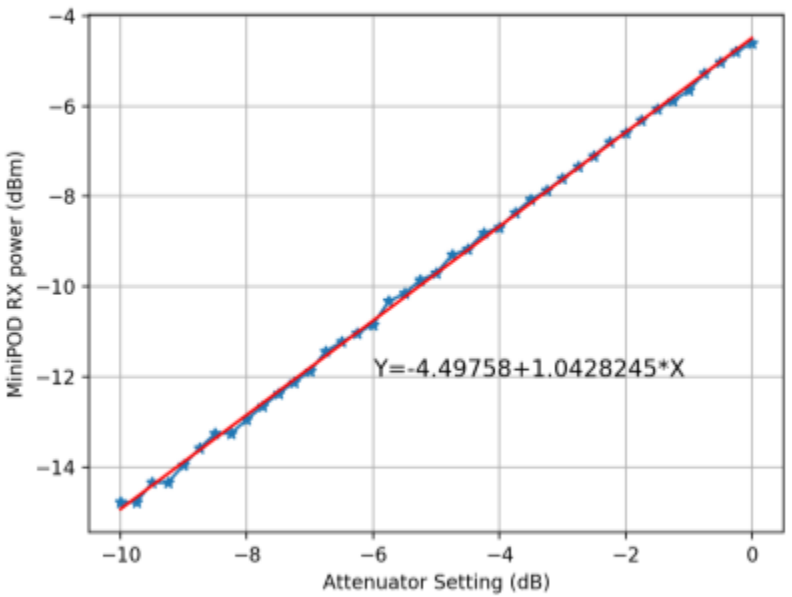
~3 months operation at CERN





Lesson Learned: Air filter is recommended for WIEC during commissioning & operation

Power measurement with MiniPOD

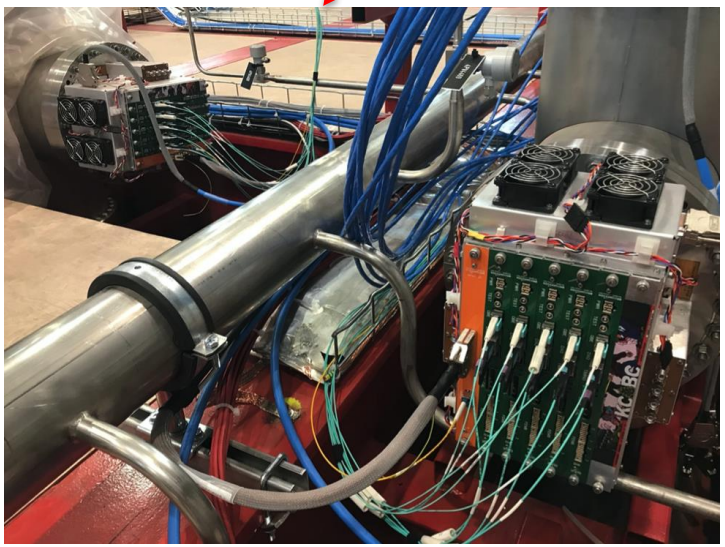


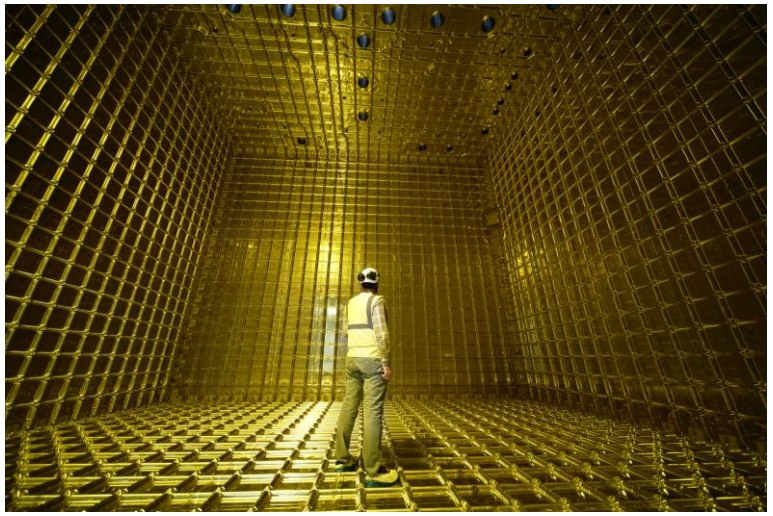
- ***MiniPOD supports to measure the internal received power.***
- ***Scan with different attenuation was performed.***
- ***Test results for RX MiniPOD in 9.6 Gb/s shows:***
  - Though datasheet requires input power be bigger than -10dBm/100uW. Test shows when the internal measured power is bigger than -13dBm/50uW, BER will < 1E-15.
- ***To do: test received power with more WIB channels and more FELIX channels. Compare different fiber types and lengths.***

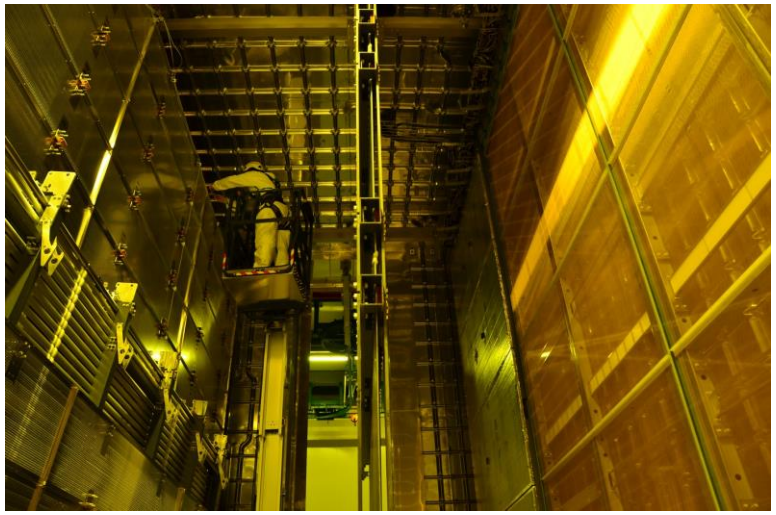
BROOKHAVEN NATIONAL LABORATORY

ProtoDUNE-SP (NP04) at CERN

NP04







6x Feed-through/WIEC assemblies

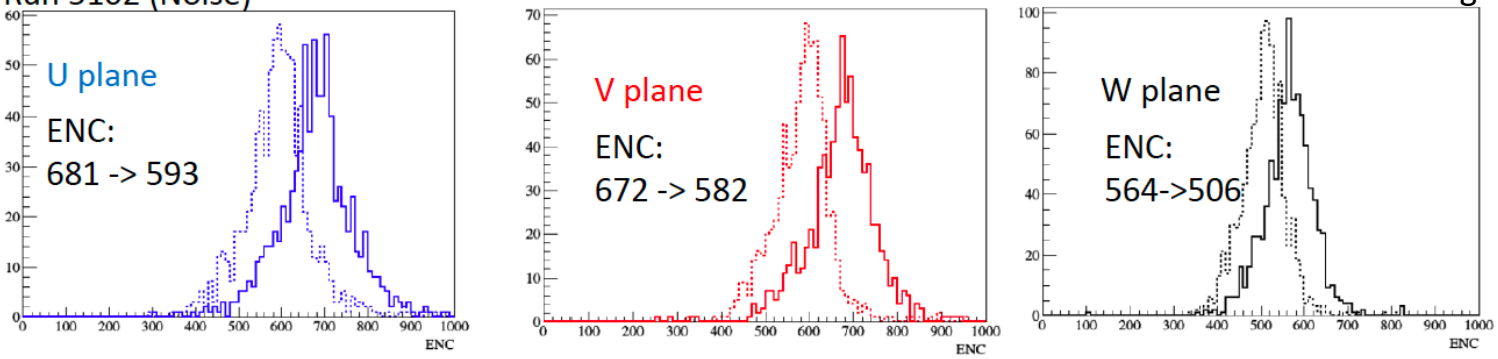
ProtoDUNE-SP CE Status in Detector Operation

- No FE channel got damaged by bias during CERN cold box integration test
  - No cathode but nominal wire bias voltages under strong LN2 air flow
- With 180kV cathode and nominal bias voltages
  - 99.74% (15320 of 15360) of TPC channels are active
    - **Only 4 inactive cold electronics channels**
  - **92.83% TPC channels have excellent noise performance**
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
  - **2 more inactive channels** on APA6 were observed Nov. 27, 2019

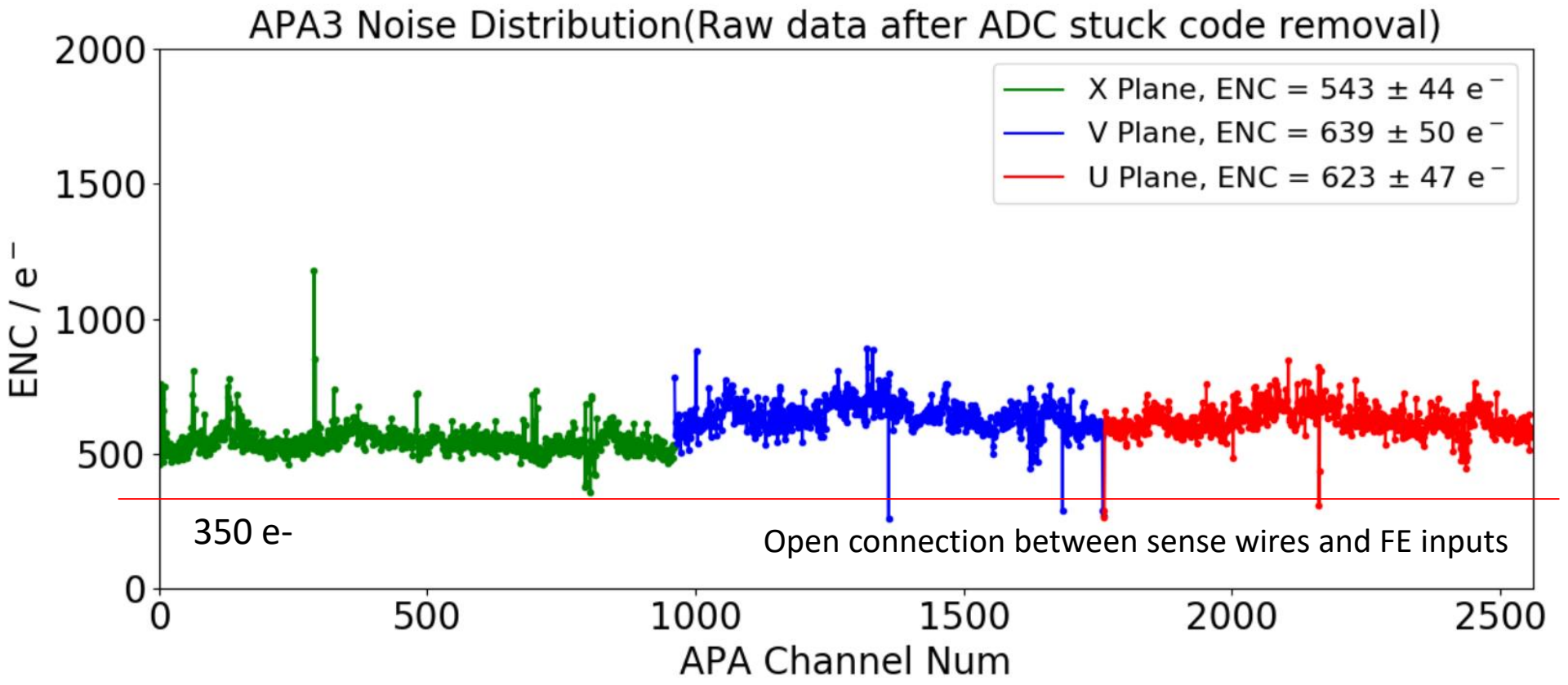
	09/13/2018		09/23/2018		11/27/2019
Item	**test#1**	**test#5**	**test #18**	**test #35**	**DAQ**
Drift	**off**	**120kV%**	**160kV**	**180kV**	**180kV**
Bias	**off**	**on**	**on**	**on**	**on**
FE Inactive	**0**	**2**	**4**	**4**	**6**
Channels (good & <800e-)	**14397**	14297	14179	**14259**	**/**

Run 5102 (Noise)

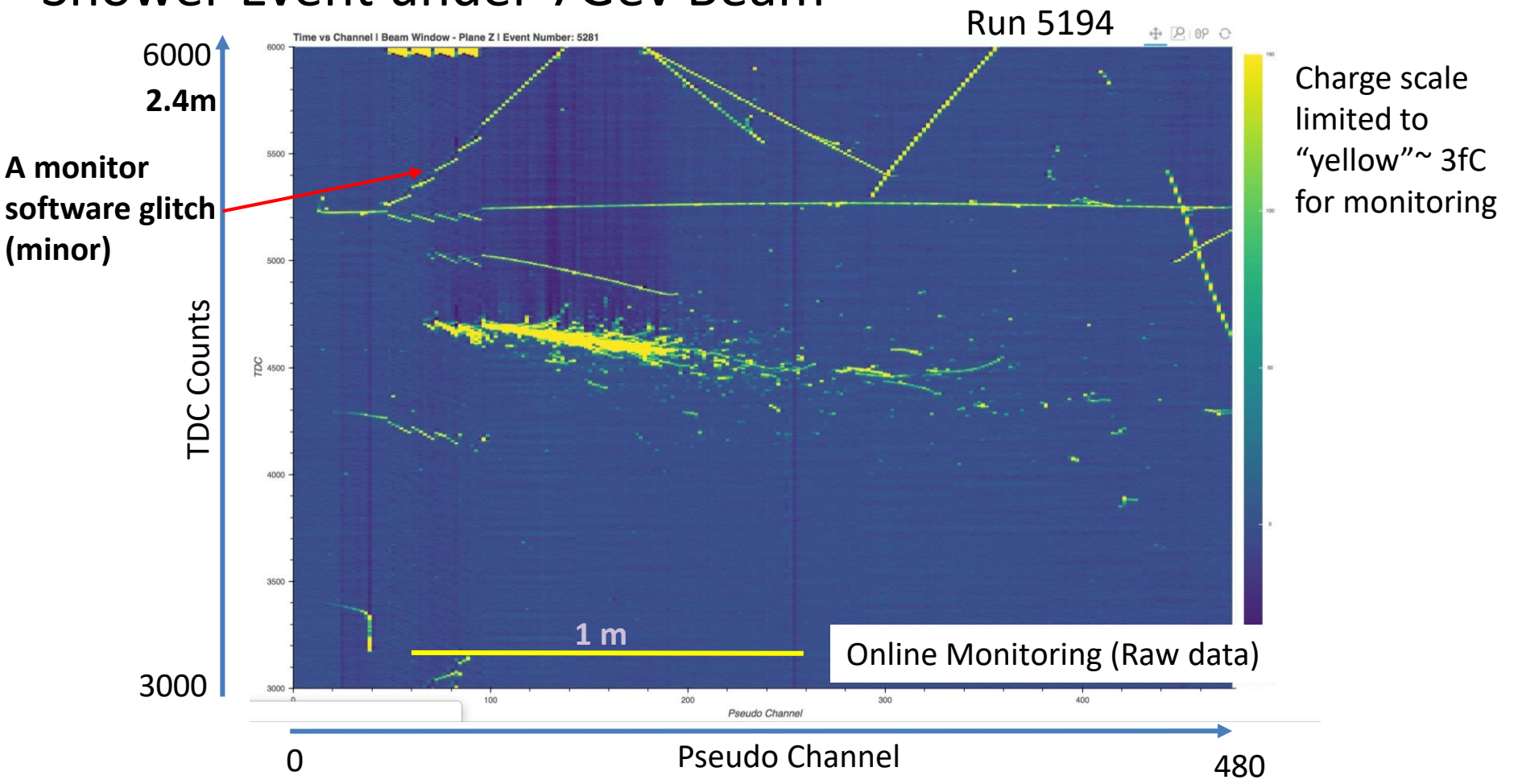
Solid line: raw data. Dotted line: offline filtering



APA3 Noise Distribution in ProtoDUNE-SP Commissioning



Shower Event under 7Gev Beam



T. Yang's talk in the LBNC Review

- High signal-to-noise ratio (Collection Y: 48, induction U: 18, induction V: 21)
- Very few dead/noisy channels (< 0.1% dead)
- Most of the identified issues in raw data are minor and can be mitigated in the offline analysis