Intermediate WIB Prototype Hardware

Xilinx Zynq Ultrascale+

Jack Fried on behalf of the CE group

March 10 , 2020

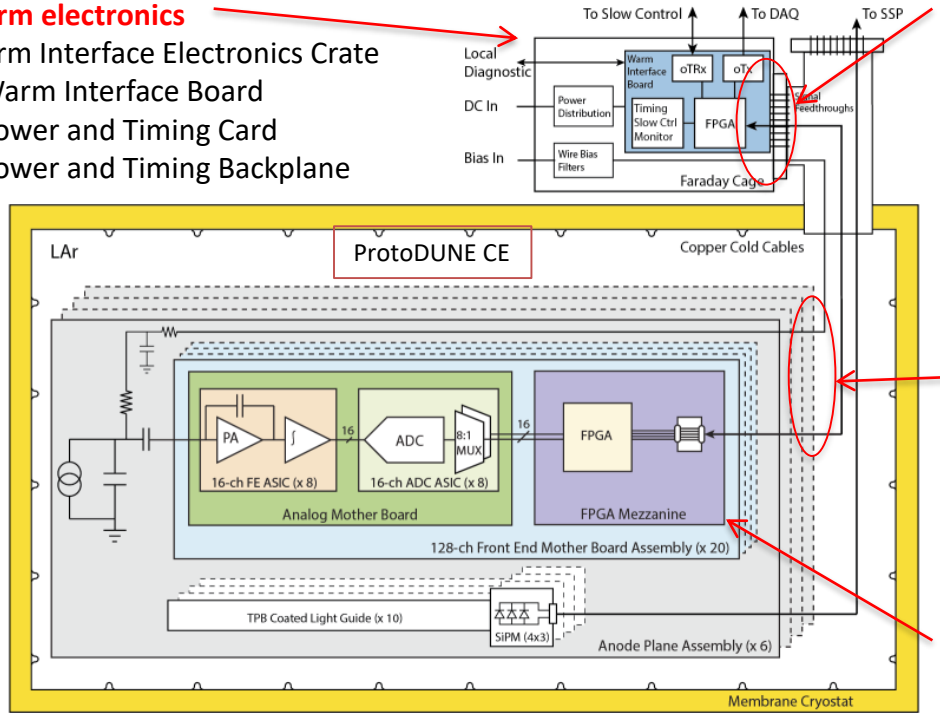
Outline

- WIB Architecture
- WIB Implementation
  - Hardware
- WIB Status
  - Software

Cold Electronics

Warm electronics

Warm Interface Electronics Crate
- Warm Interface Board
- Power and Timing Card
- Power and Timing Backplane



CE flange

Flange assembly with cable strain relief and flange PCB for cable/WIB connection

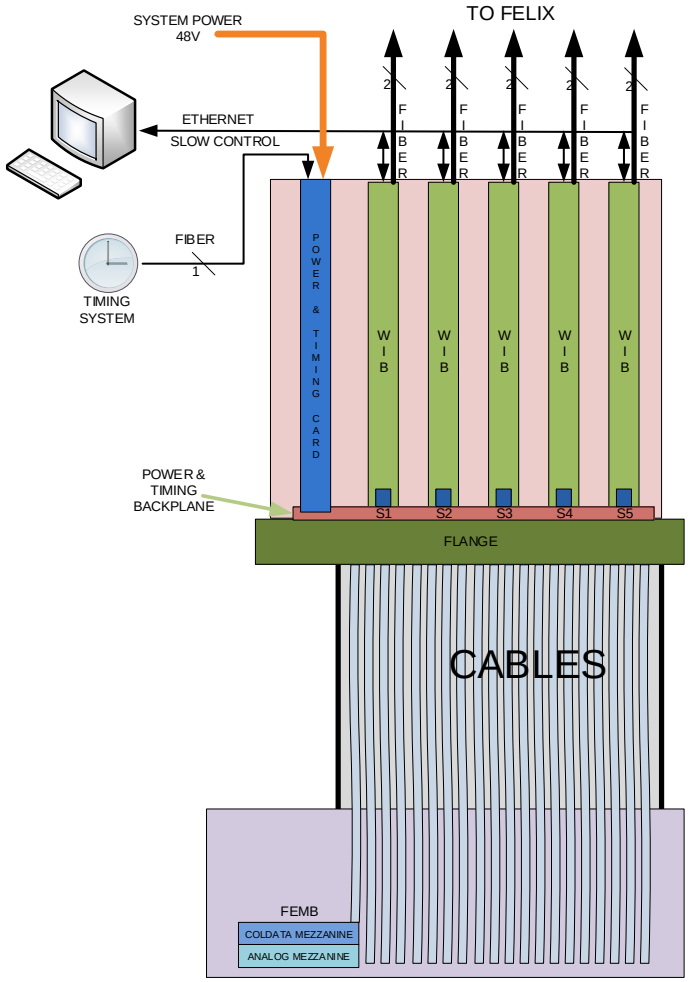
Cold cables

Cables used for low voltage and data/clock transport to FEMB's

Front End Motherboard

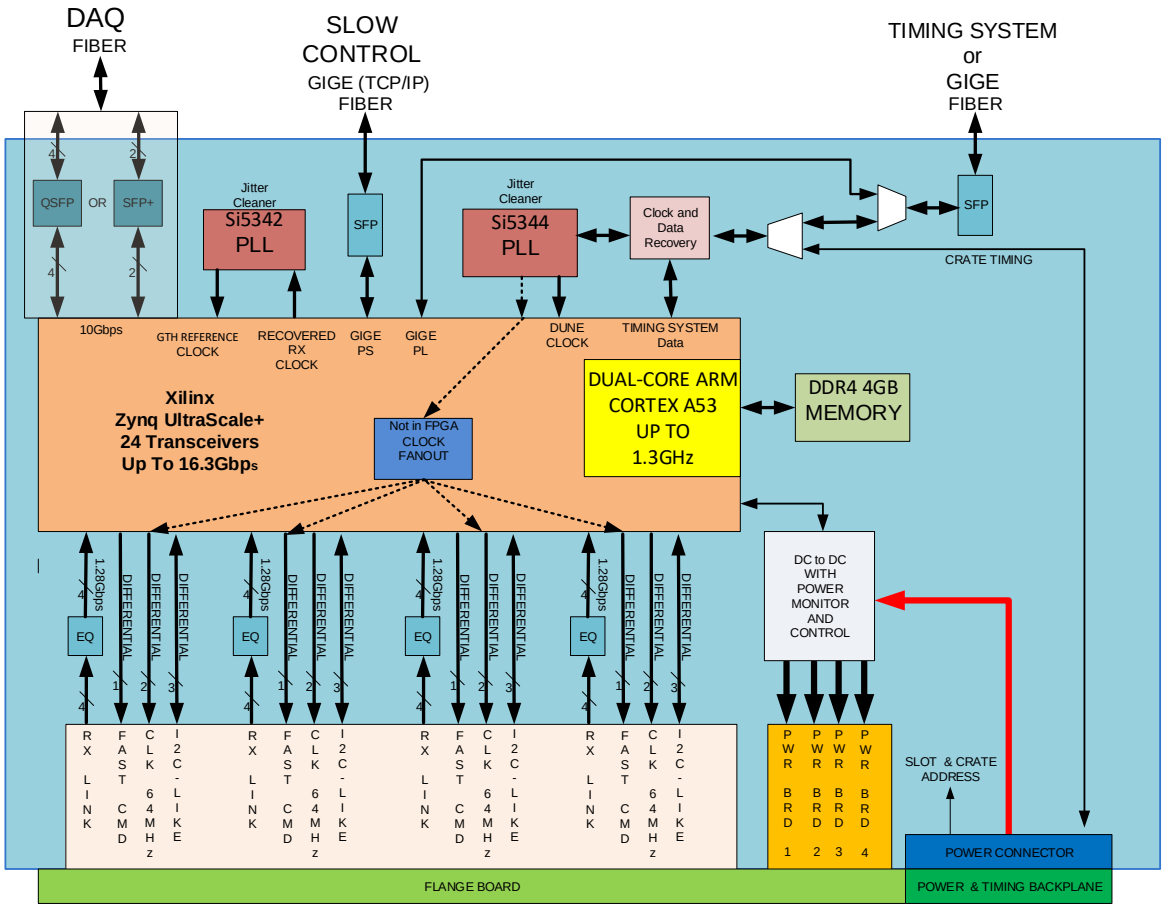
(FEMB) 128 channels of digitized wire readout enclosed in CE Box

Warm Interface Crate (WIEC)



- WIEC Boards
  - 5 Warm Interface Boards (WIB)
    - Interfaces with 20 Front End Motherboards (FEMB)
  - 1 Power and Timing Card (PTC)
  - 1 Power and Timing Backplane (PTB)
  - 1 Flange board
- WIEC connections
  - With Backend electronics
    - 1 48V supply (PTC)
    - 1 LC timing fiber (PTC)
    - 5 duplex LC GbE fibers (WIB)
    - 5 MTP DAQ fibers (WIB)
      - 10 Duplex LC SFP+ (next version)
  - With cold electronics
    - 20 Samtec data cables (flange)
    - 20 Samtec power cables (flange)

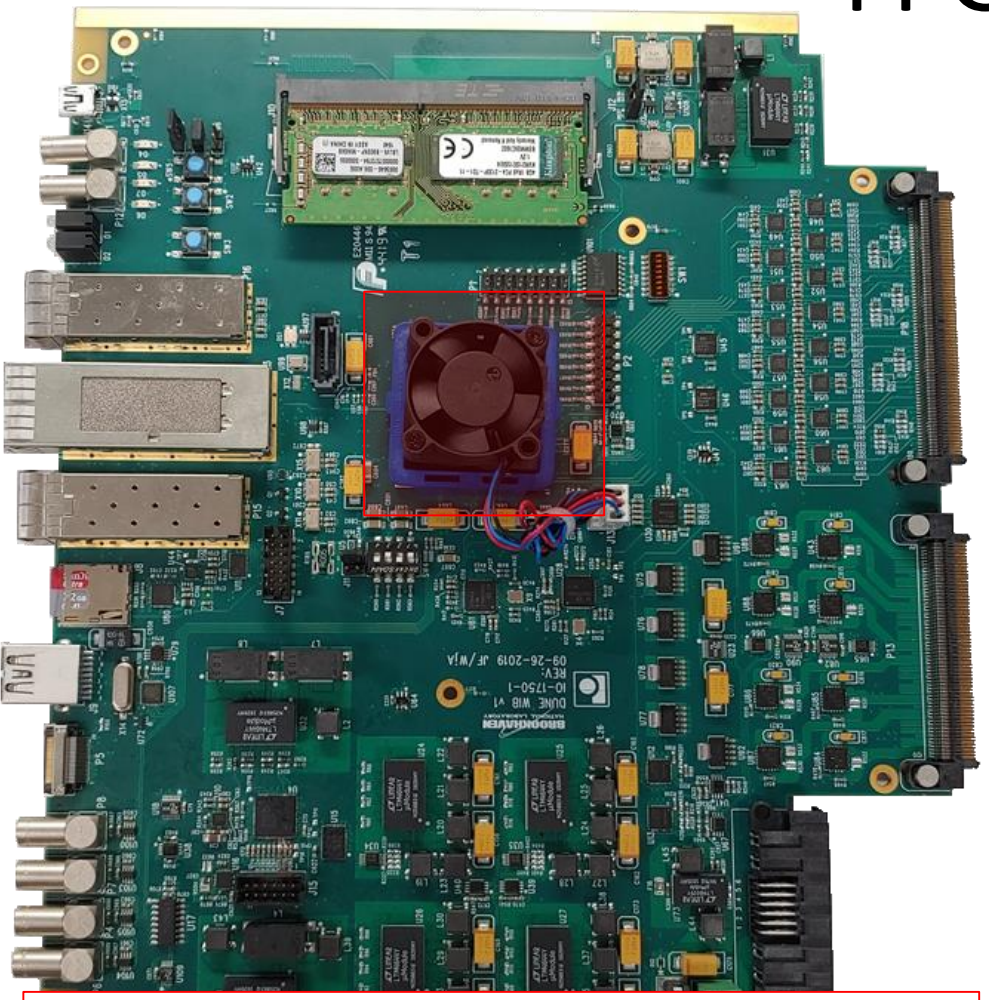
Xilinx Zynq WIB Block Diagram



Basic WIB functions

- Communicate to slow control / CCM
- Communicate / configure up to four FEMBs
- Receive data from FEMBs
- Package FEMB data and send to DAQ
- Receive timing signal to synchronize system
- Control and monitor power for the FEMBs/WIB

Xilinx Zynq Ultrascale+ FPGA



- Xilinx Zynq Ultrascale+ FPGA (ZU6CG)
  - B1156 pin package
  - Dual-core ARM Cortex A53 processor
    - Migratable to Quad-Core
  - Migration path available for larger devices 9CG, 6EG, **9EG** and 15EG.

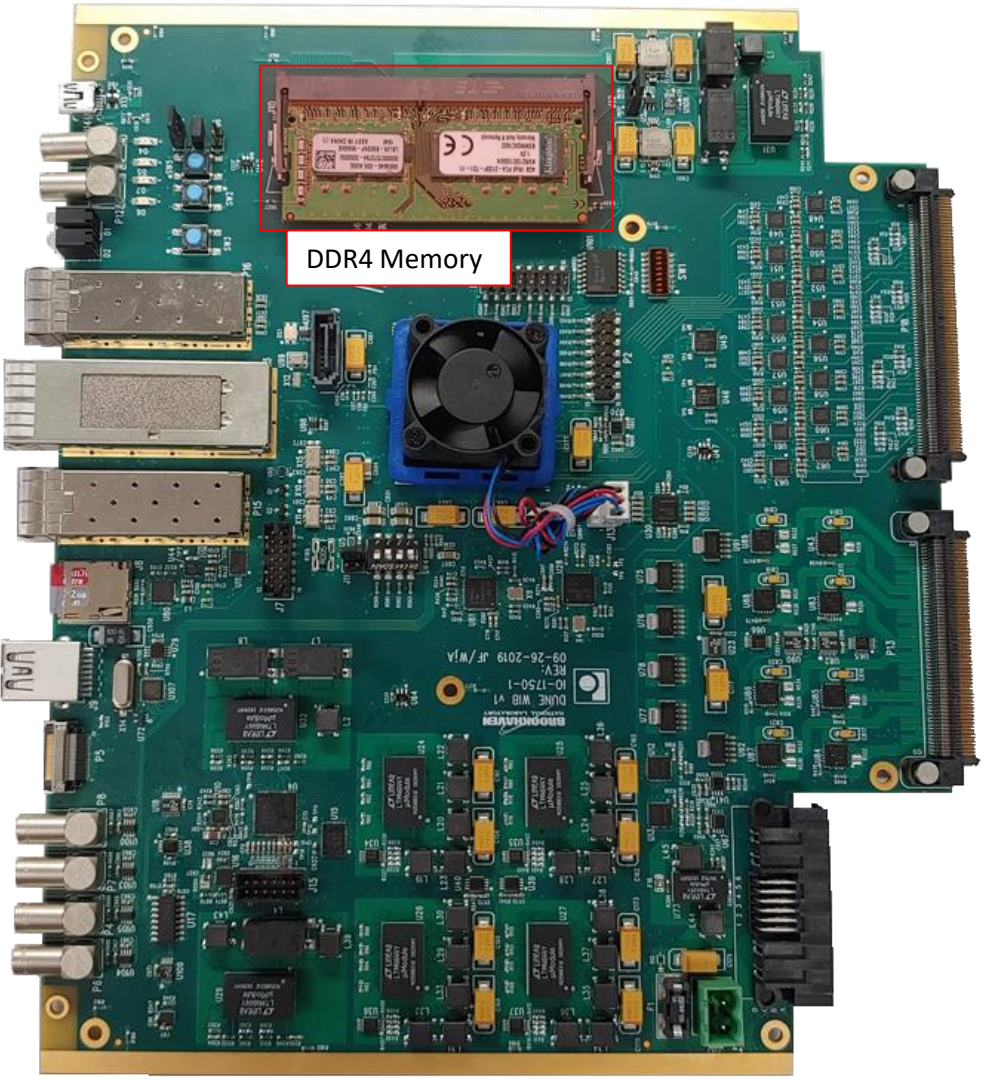
Due to availability and longer lead time at the time of board assembly, the first WIB prototype board has been produced with XCZU9EG-1FFVB1156E (quad core) FPGA

Zynq® UltraScale+™ MPSoC Device Migration Table

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible.

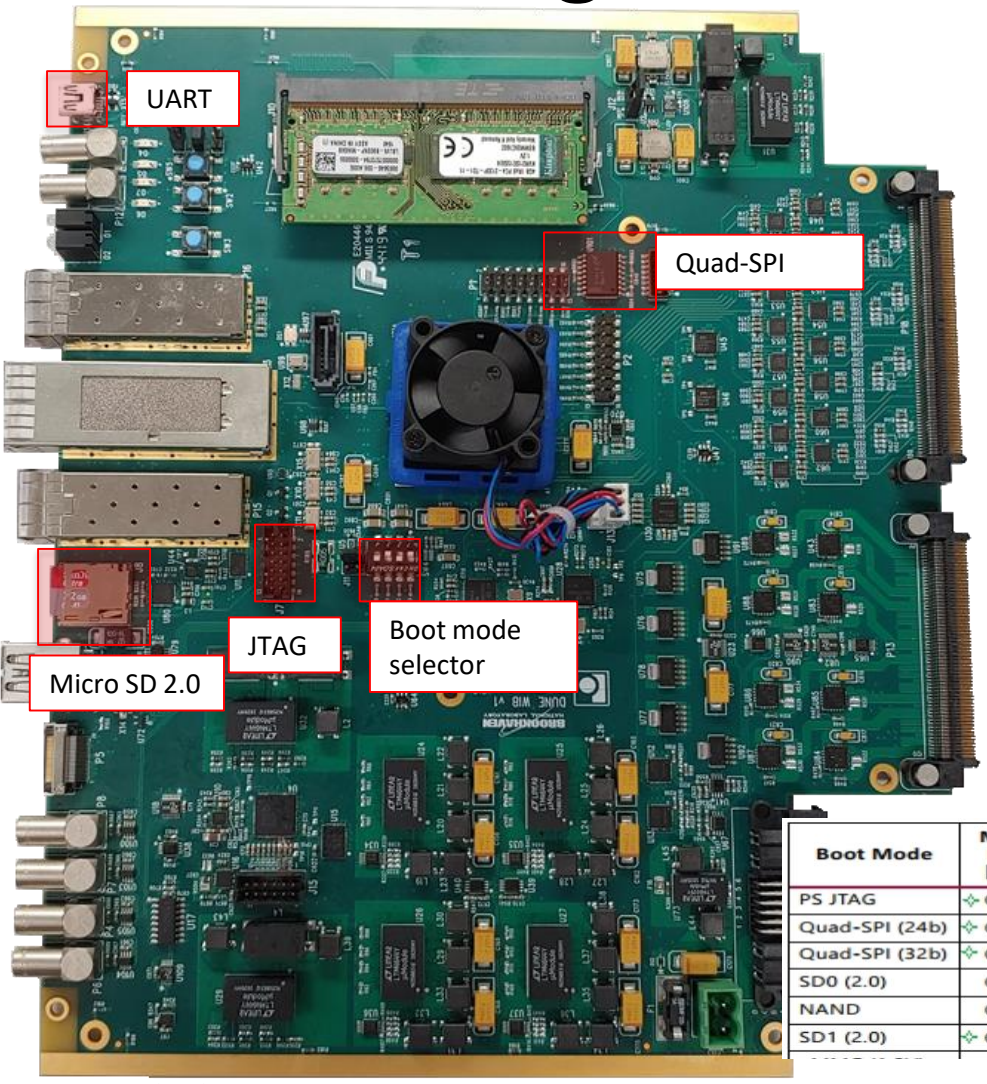
Pkg	mm	Zynq® UltraScale+™																					
		CG Devices							EG Devices												EV Devices		
		ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG	ZU4EV	ZU5EV	ZU7EV
A484	19	●	●						●	●													
A625	21	●	●						●	●													
C784	23	●	●	●	●	●			●	●	●	●								●			
B900	31			●	●		●				●	●		●						●	●	●	
C900	31					●		●					●		●								
B1156	35					●		●					●		●								
C1156	35						●							●		●							
B1517	40															●	●	●					
F1517	40						●							●		●							
C1760	42.5															●	●	●					
D1760	42.5																	●					
E1924	45																	●					

Xilinx Zynq Ultrascale+ DRR4 Memory



- Xilinx Zynq Ultrascale+ FPGA Processor side memory
  - 4 GB DDR4 SODIMM, 260-pin
  - Supports up to DDR4-2666
  - Supports up to 16GB

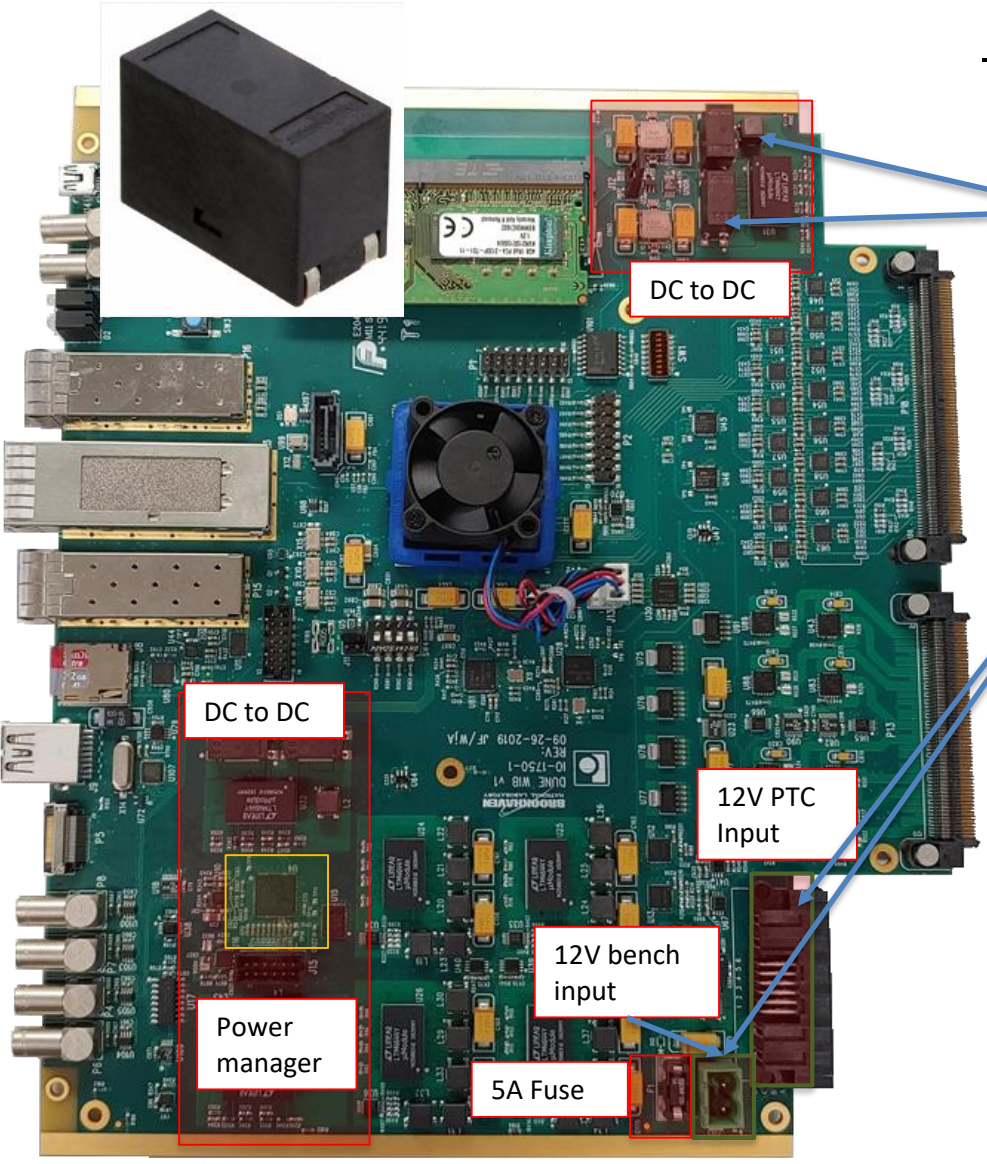
Xilinx Zynq Ultrascale+ Configuration and Debugging



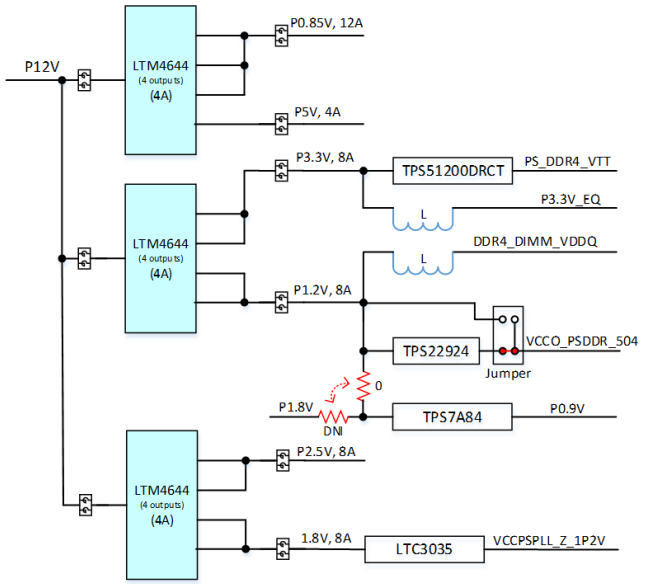
- WIB configuration modes
  - Selectable by dip switch
    - JTAG
    - Dual QUAD-SPI
      - » Provides 1 Gb of non-volatile storage
    - SD card 2.0
- Debugging
  - JTAG
  - UART to USB bridge

Boot Mode	Mode Pins [3:0]	Pin Location	Non-Secure	Secure	Signed	CSU Mode	Description
PS JTAG	0000	JTAG	Yes	No	No	Slave	PSJTAG interface, PS dedicated pins.
Quad-SPI (24b)	0001	MIO[12:0]	Yes	Yes	Yes	Master	24-bit addressing (QSPI24).
Quad-SPI (32b)	0010	MIO[12:0]	Yes	Yes	Yes	Master	32-bit addressing (QSPI32).
SD0 (2.0)	0011	MIO[25:13]	Yes	Yes	Yes	Master	SD 2.0.
NAND	0100	MIO[25:09]	Yes	Yes	Yes	Master	Requires 8-bit data bus width.
SD1 (2.0)	0101	MIO[51:46]	Yes	Yes	Yes	Master	SD 2.0.

WIB Local Power



- WIB Local power
  - Total of 9 power rails 0.85V, 0.9V, 1.2V, 1.8V, 2.5V, 3.3V, 5.0V and PS_DDR4_VTT
  - All inputs and outputs of DC/DC modules are isolated by common mode chokes (CMCs) to minimize the common mode noise
  - Two ways to power the WIB 12V supply
    - Samtec 30A MPTC connector from PTC
    - Molex connecter for benchtop testing



WIB Local Power

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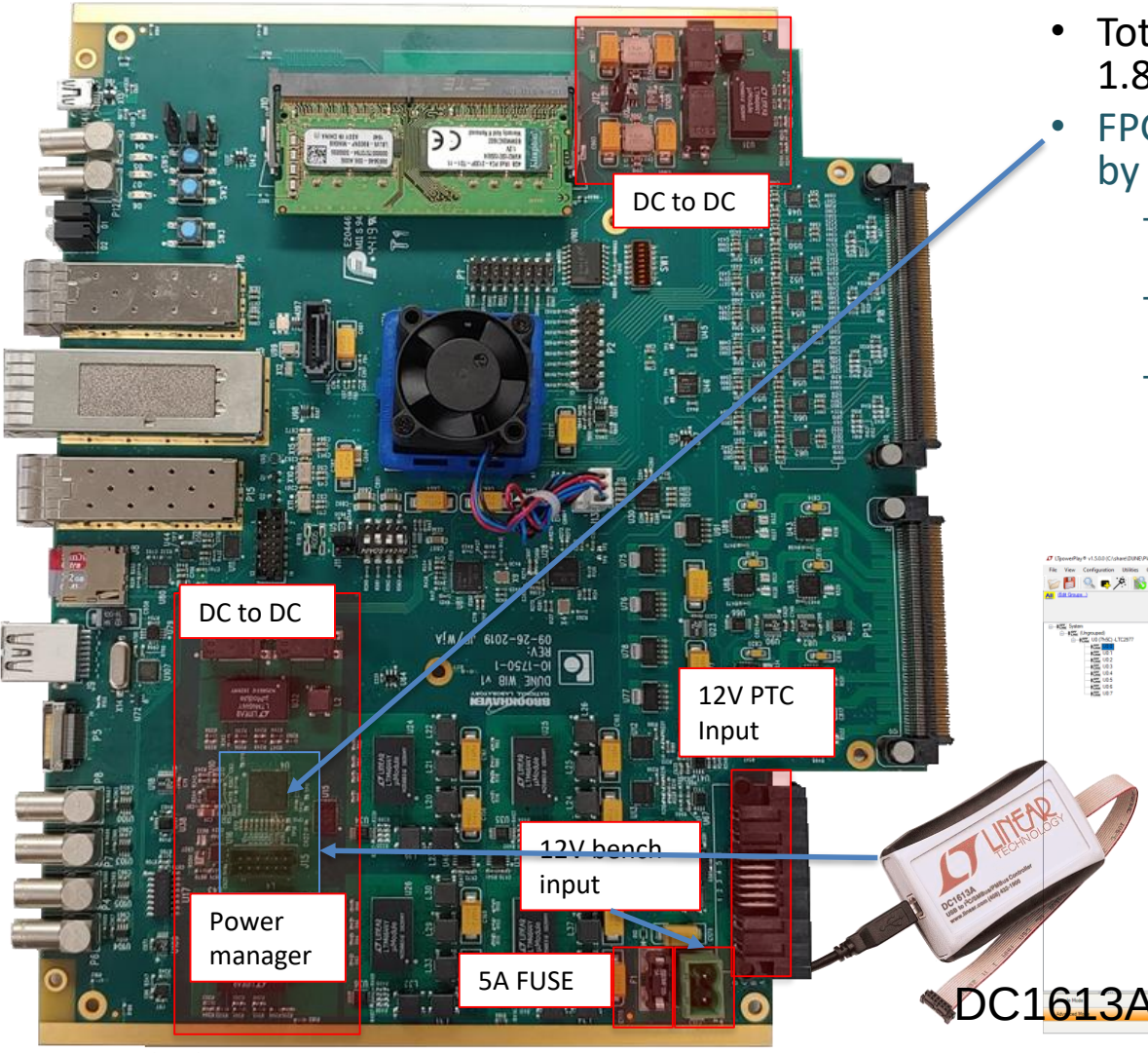
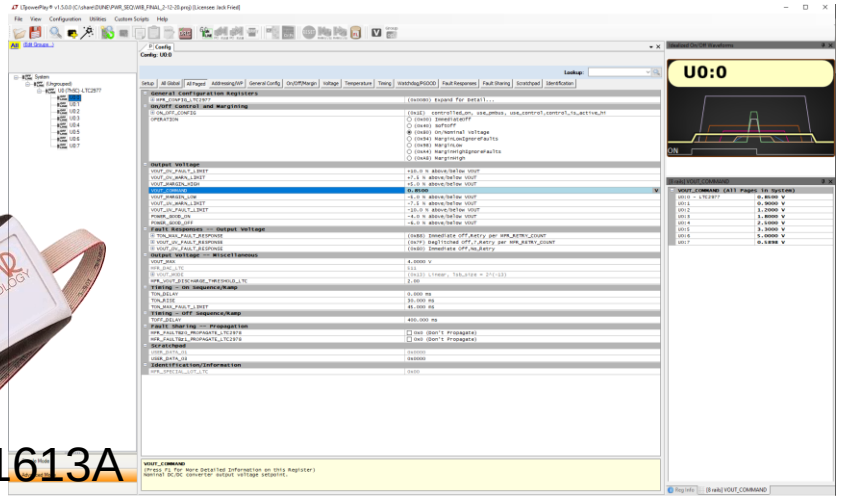
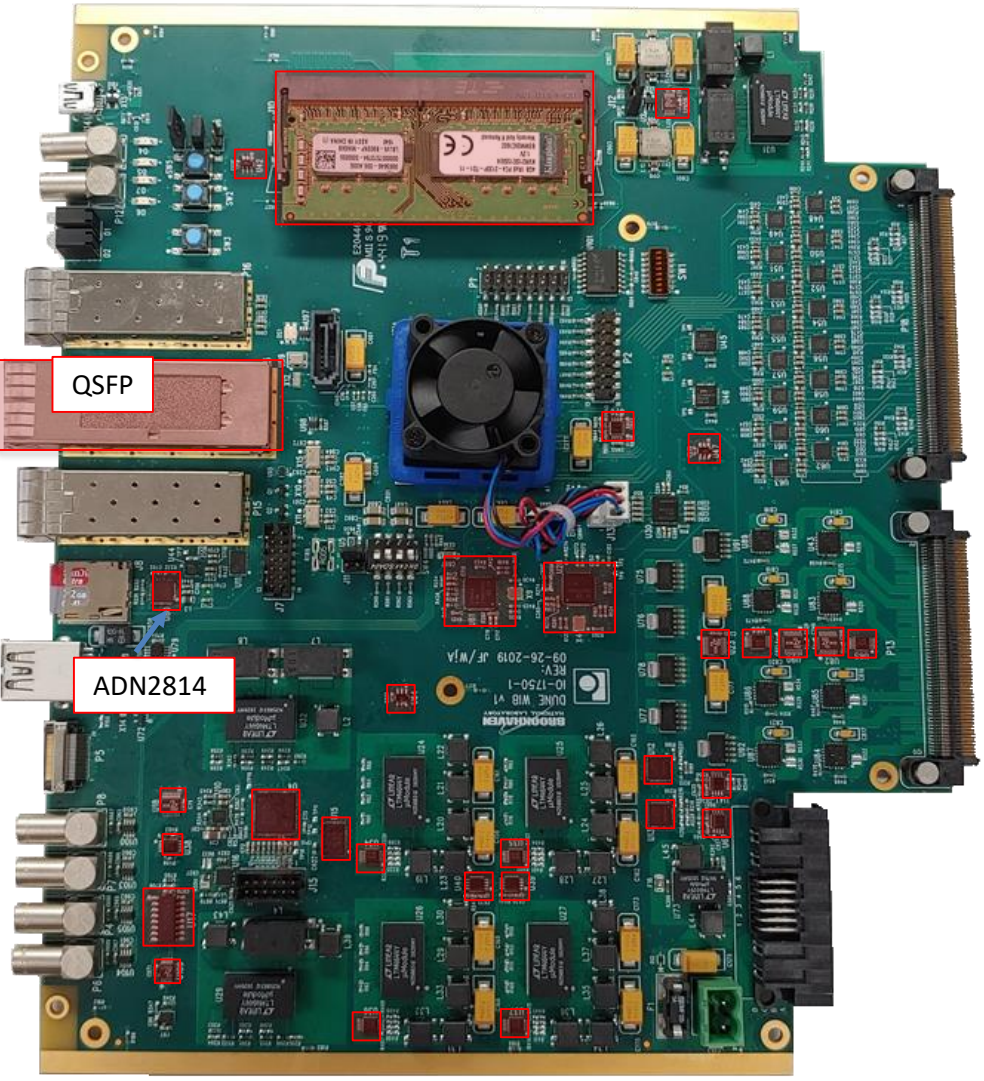
  - Total of 9 power rails 0.85V, 0.9V, 1.2V, 1.8V, 2.5V, 3.3V, 5.0V and PS_DDR4_VTT
  - FPGA Power sequencing and monitoring by LTC2977 power management chip
    - Sequence, Trim, Margin and Supervise Eight Power Supplies
    - Automatic Fault Logging to Internal EEPROM
    - Operate Autonomously without Additional Software



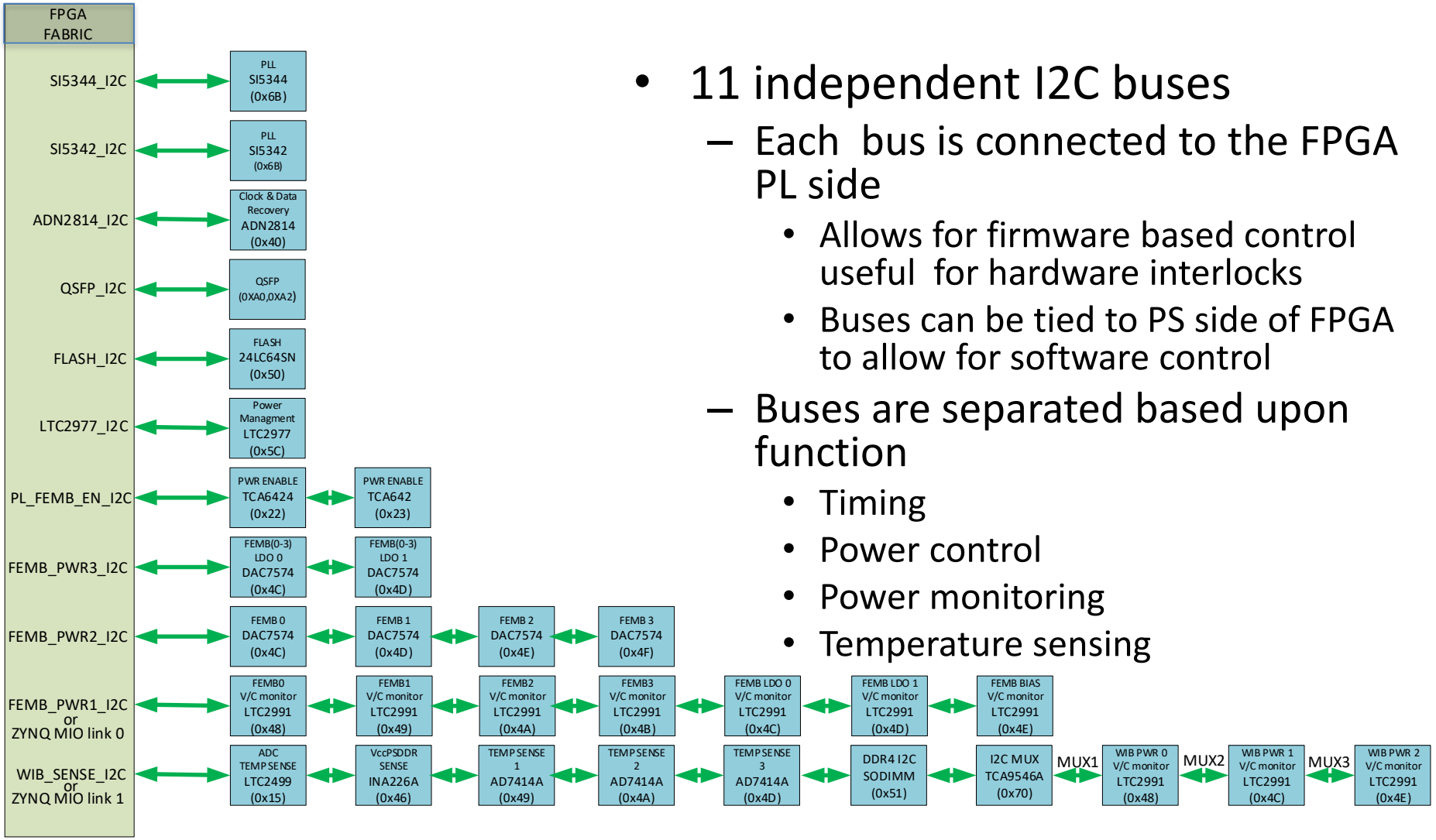


WIB I2C



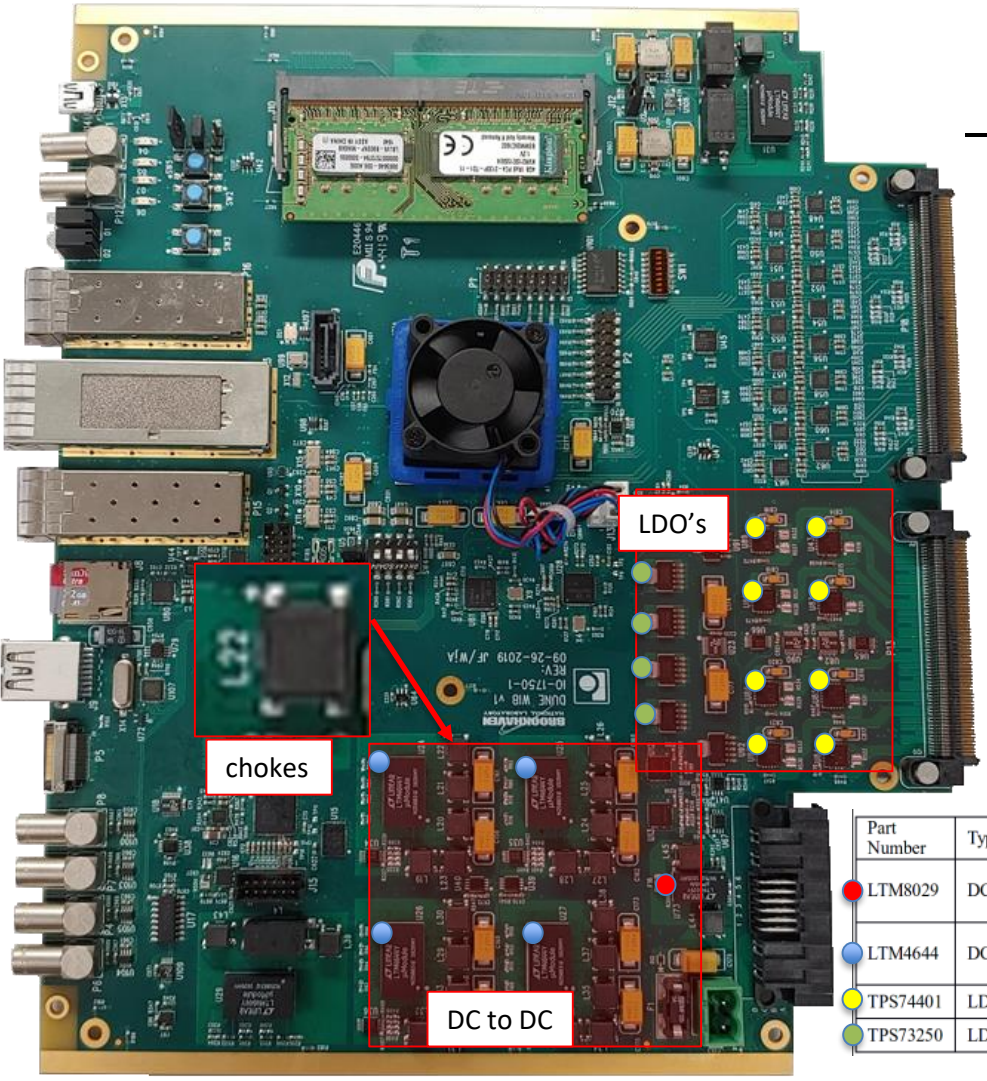
- WIB I2C controls
  - WIB power monitor
    - Voltage & current
  - PLL configuration
  - Clock & data recovery
  - DDR4 interface
  - QSFP interface
  - Flash memory
  - FEMB power monitor
    - Voltage & current
  - FEMB power control
    - Voltage Adjustment
    - Power on & off
  - Temperature Sensors

WIB I2C MAP



- 11 independent I2C buses
  - Each bus is connected to the FPGA PL side
    - Allows for firmware based control useful for hardware interlocks
    - Buses can be tied to PS side of FPGA to allow for software control
  - Buses are separated based upon function
    - Timing
    - Power control
    - Power monitoring
    - Temperature sensing

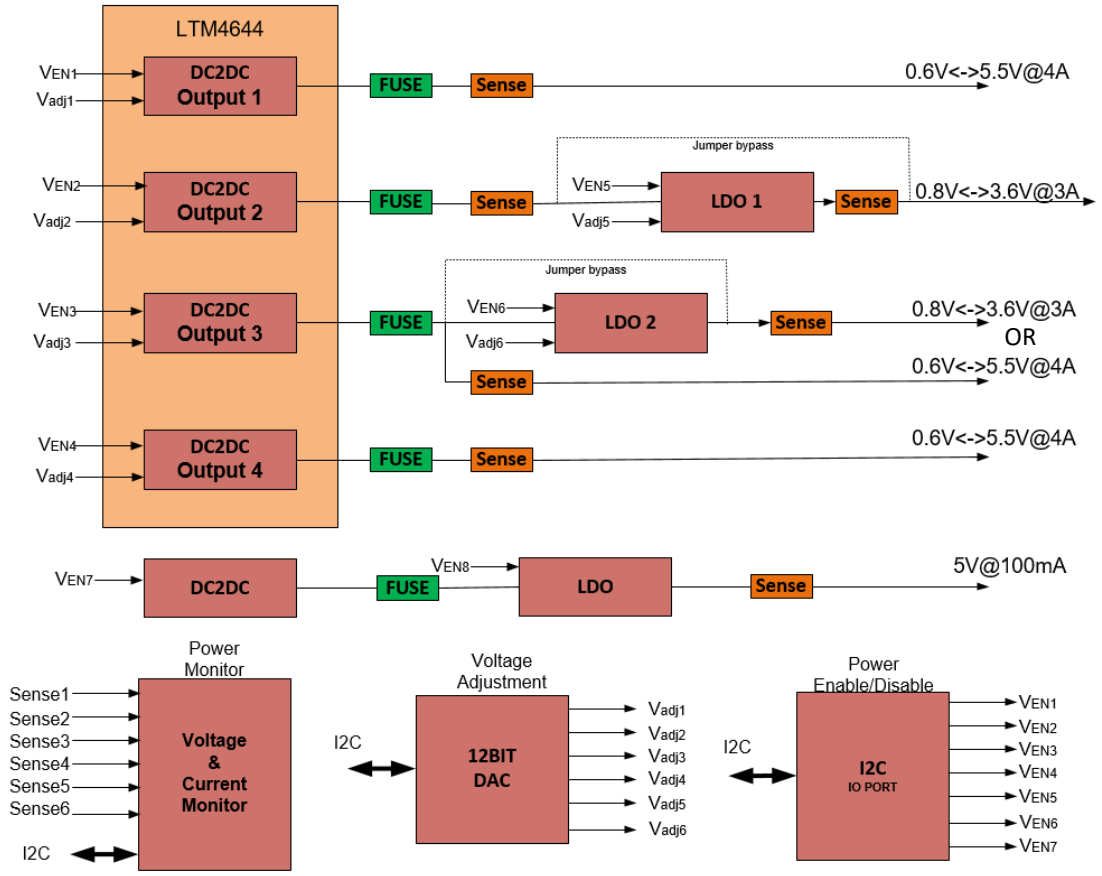
WIB FEMB Power



- Power control and monitoring
  - Multiple configuration options for FEMB power (ProtoDUNE, SBND and Dune Cold Data ASIC)
    - FEMB voltage and current monitoring
    - Remote FEMB Voltage control and adjustment
  - All inputs and outputs of DC/DC modules are isolated by common mode chokes (CMCs) to minimize the common mode noise propagated to the FEMBs

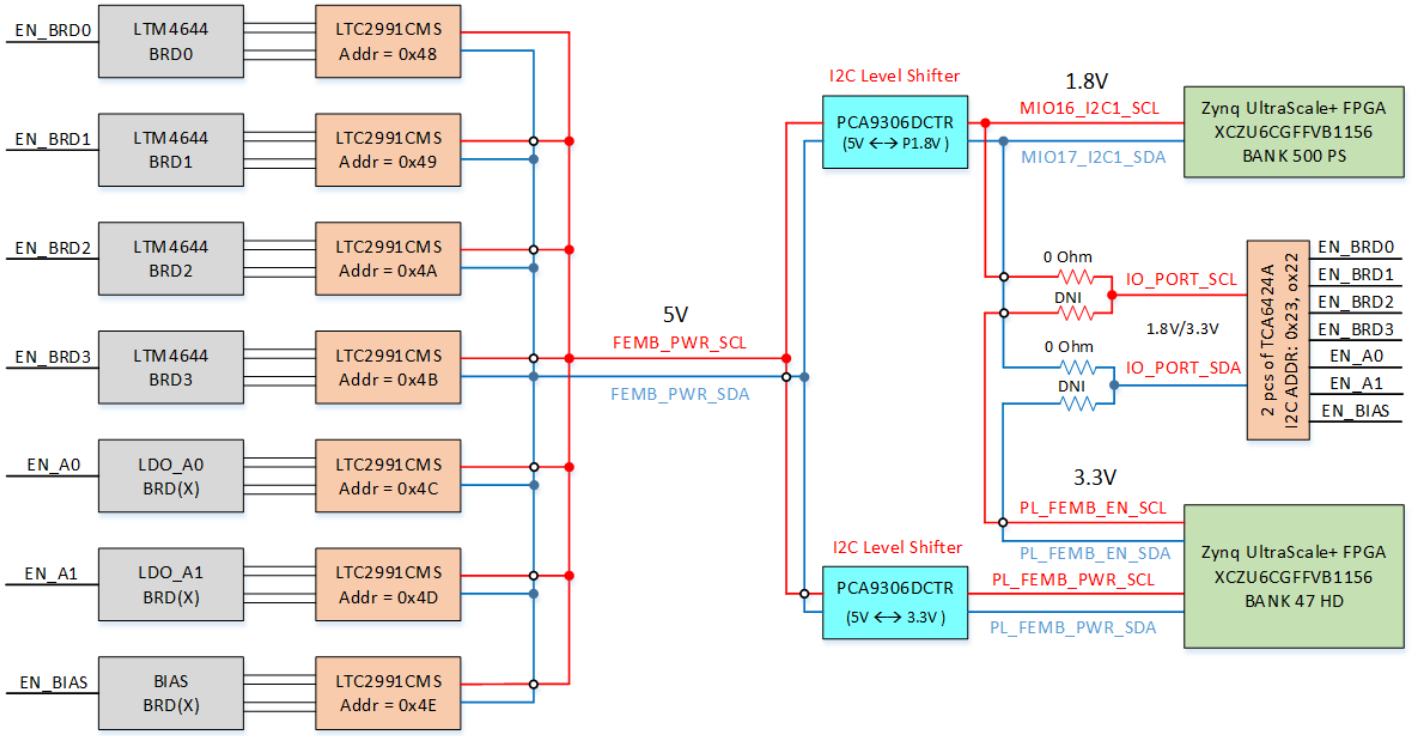
Part Number	Type	Package	Input	Output	Output Number	Output Current (max)	Switching Frequency	Output Noise
LTM8029	DC/DC	35-BBGA	4.5~46V	1.2~18V	1	600mA	Adjustable, 800kHz (158k) in use	RMS Ripple: 10mV @ 600mA (typ)
LTM4644	DC/DC	77-BBGA	4~14V	0.6~5.5V	4	4.0A	Adjustable, 1MHz (typ) in use	RMS Ripple: 5mV @ 0A (typ), load dependent
TPS74401	LDO	20-VQFN	5.5V max	0.8~3.6V	1	3.0A	Not applied	16 x V_{out} (typ) μV_{RMS}
TPS73250	LDO	SOT-23	5.5V max	5.0V	1	250mA	Not applied	30 (typ) μV_{RMS}

FEMB Power Supply Capability



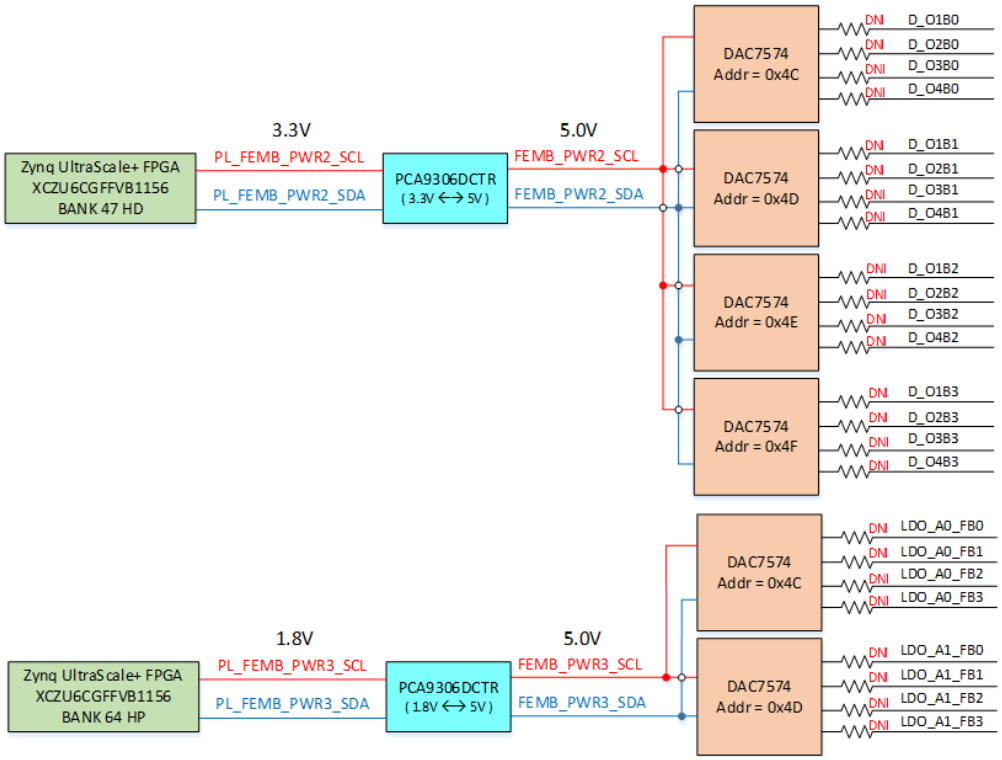
- The 12V input is regulated to deliver up to 6 supplies to each FEMB:
  - 4 power rails of up to 4A each from LTM4644 DC/DC module
  - each LTM4644 channel can be shifted/offset by a “Voltage Adjust” pin (12-bit DAC)
  - DC outputs 2 and 3 are filtered through a low noise regulator (TPS74401) in anticipation of being used as low noise power rails.
  - both filtered and unfiltered source of output 3 are accessible by the FEMB

Current measurement for FEMB power



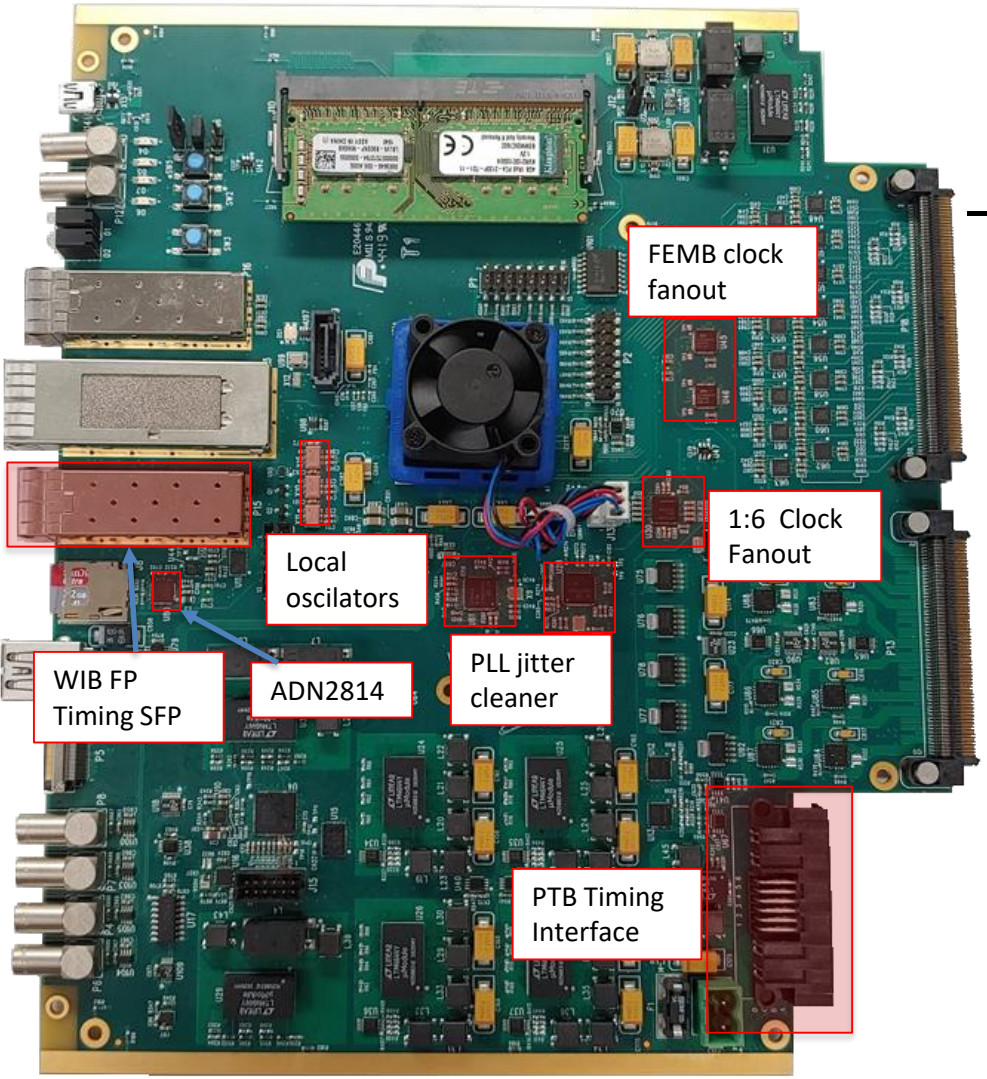
- The WIB uses LTC2991 octal I2C monitors to measure voltages and currents through pick off points. Four inputs of each LTC2991 are used to differentially measure the voltage and current across a single output's sense resistor. The I2C addresses of the monitor chips are fixed by pull up or pull down resistors to VCC or GND on 3 pins of each chip, which gives 8 address possibilities. An I2C level shifter is used to allow bidirectional voltage translations between the FPGA and the 5V required by the LTC2991 chips. The voltage the FPGA uses for I2C changes depending on which power banks are being used. This is chosen by jumper resistors. I2C devices or devices which require enable pins can be communicated with both through the Zynq Processor (accessible through Linux software), or through the FPGA fabric firmware.

Dynamic Adjustment for Outputs of Power Modules



- The actual configuration of power rail outputs can be configured entirely by firmware or runtime software through 12-bit DAC.
- This eliminates the need for hardware rework to adapt the WIB power rails to different FEMB designs.
- Through the DACs, a small amount of programmable current is injected to a feedback (FB) pin of LTM4644/TPS74401 to change the corresponding channel's output voltage.
- This is a new feature of WIB, and disabled by default, but will be extensively tested in the first revision.

WIB Clock Distribution



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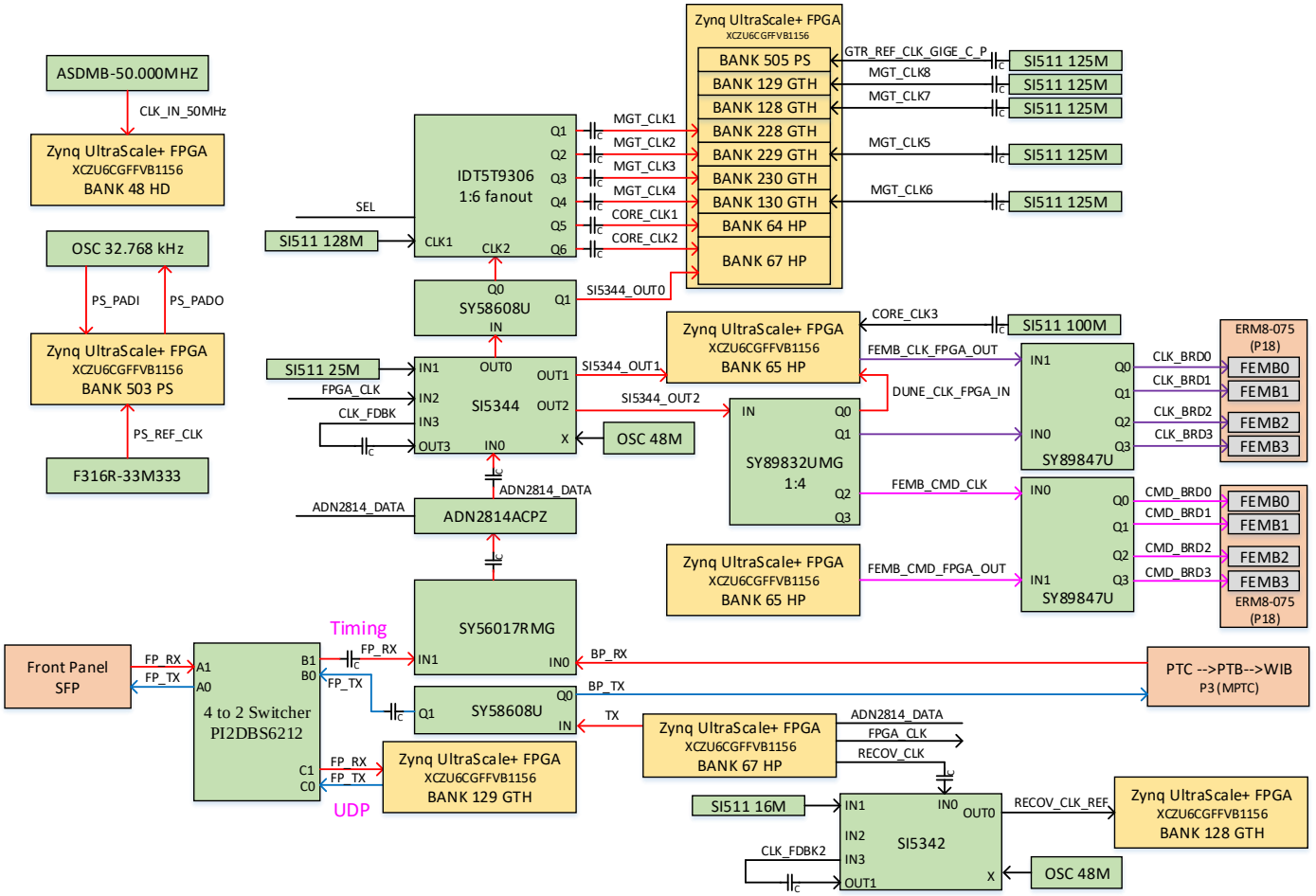
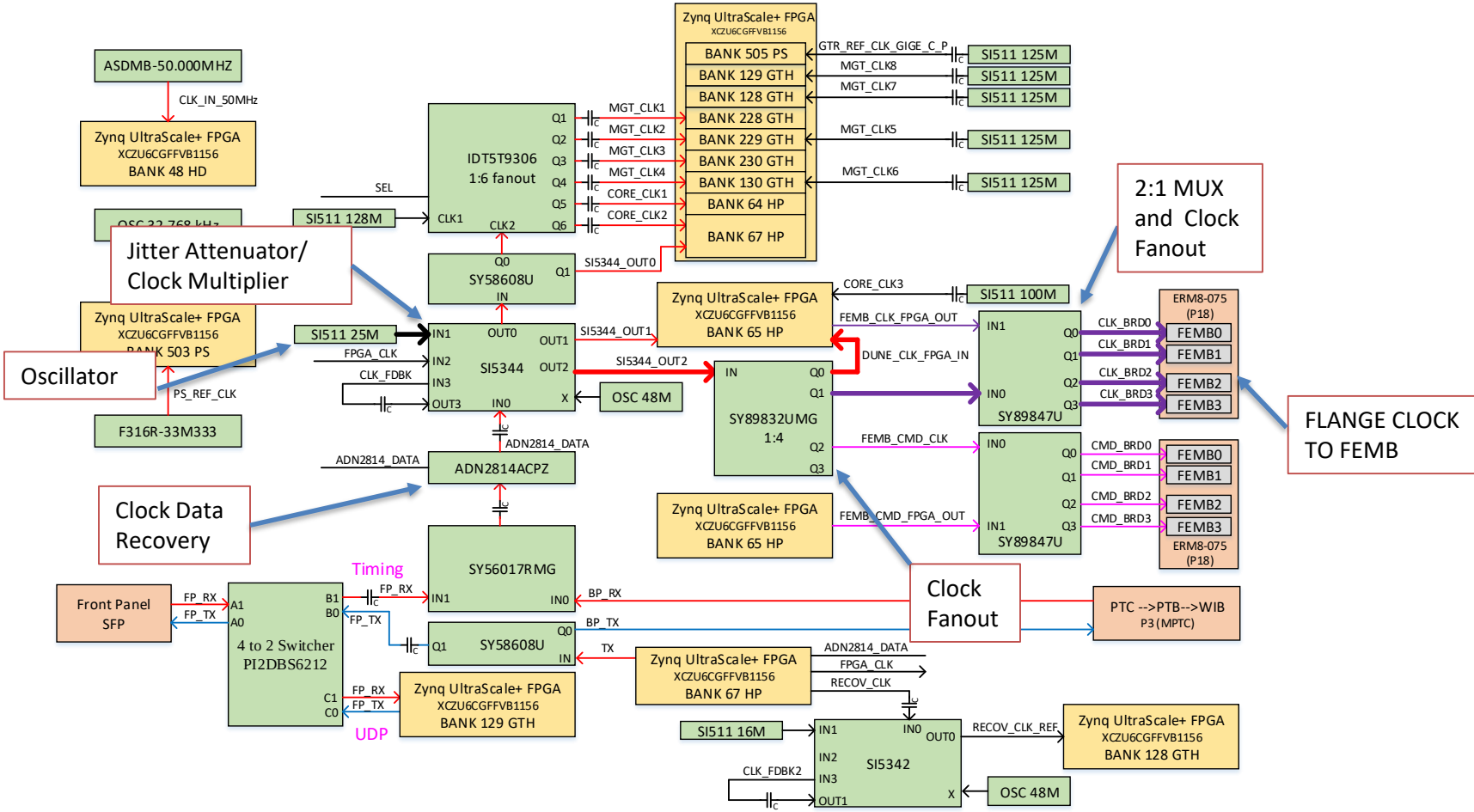
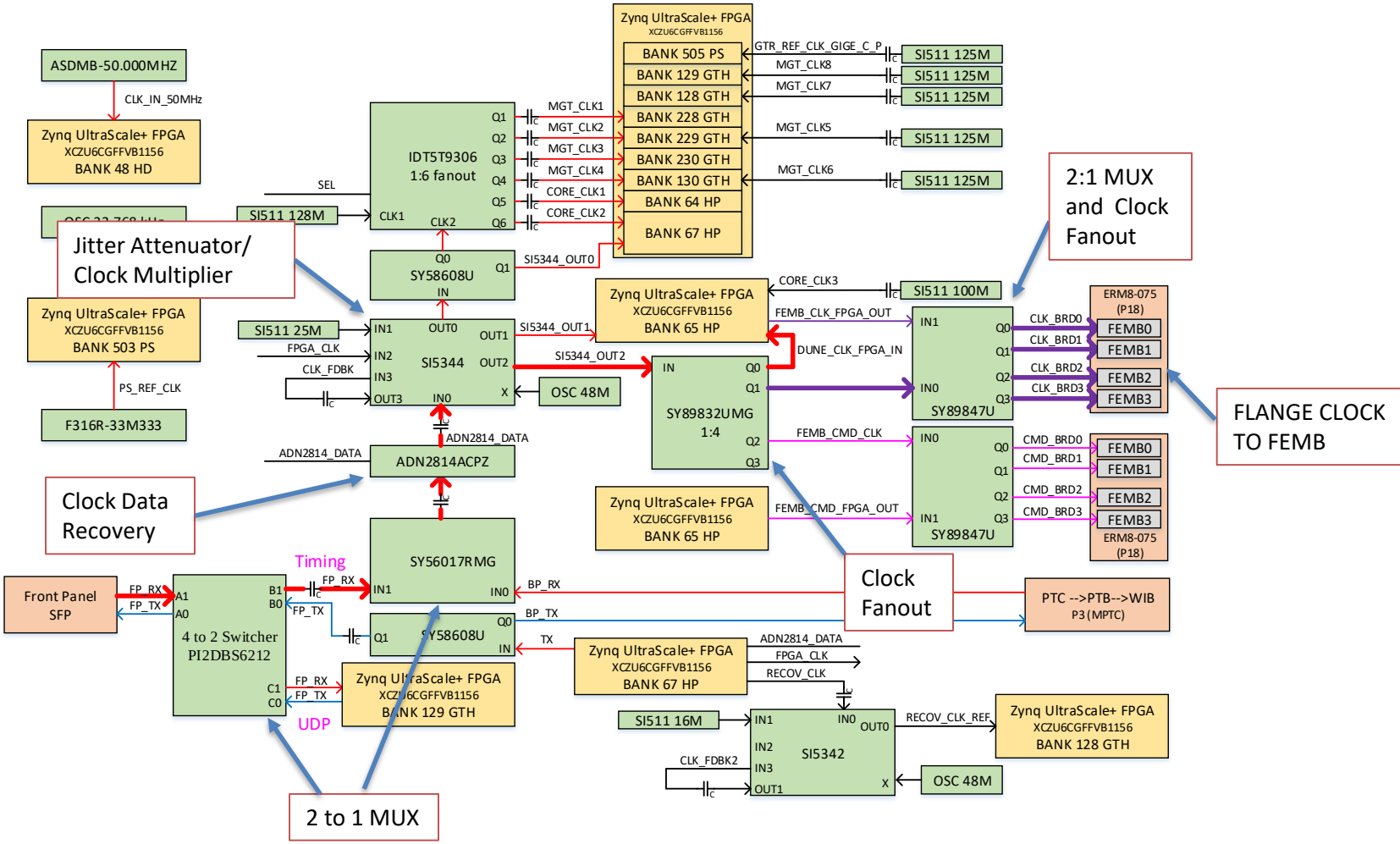
WIB Clock Distribution



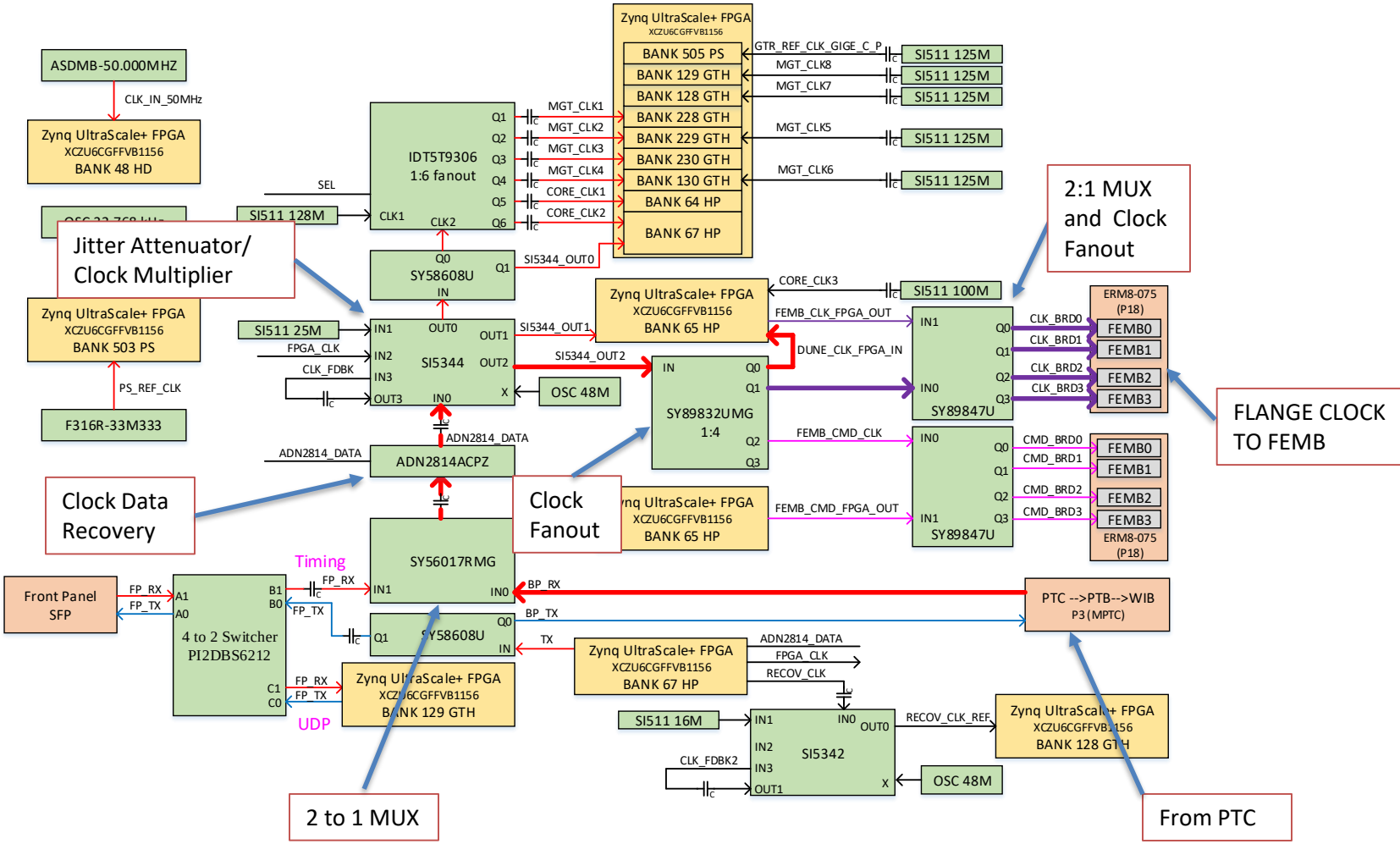
WIB FEMB Clock Distribution Using Local Oscillator



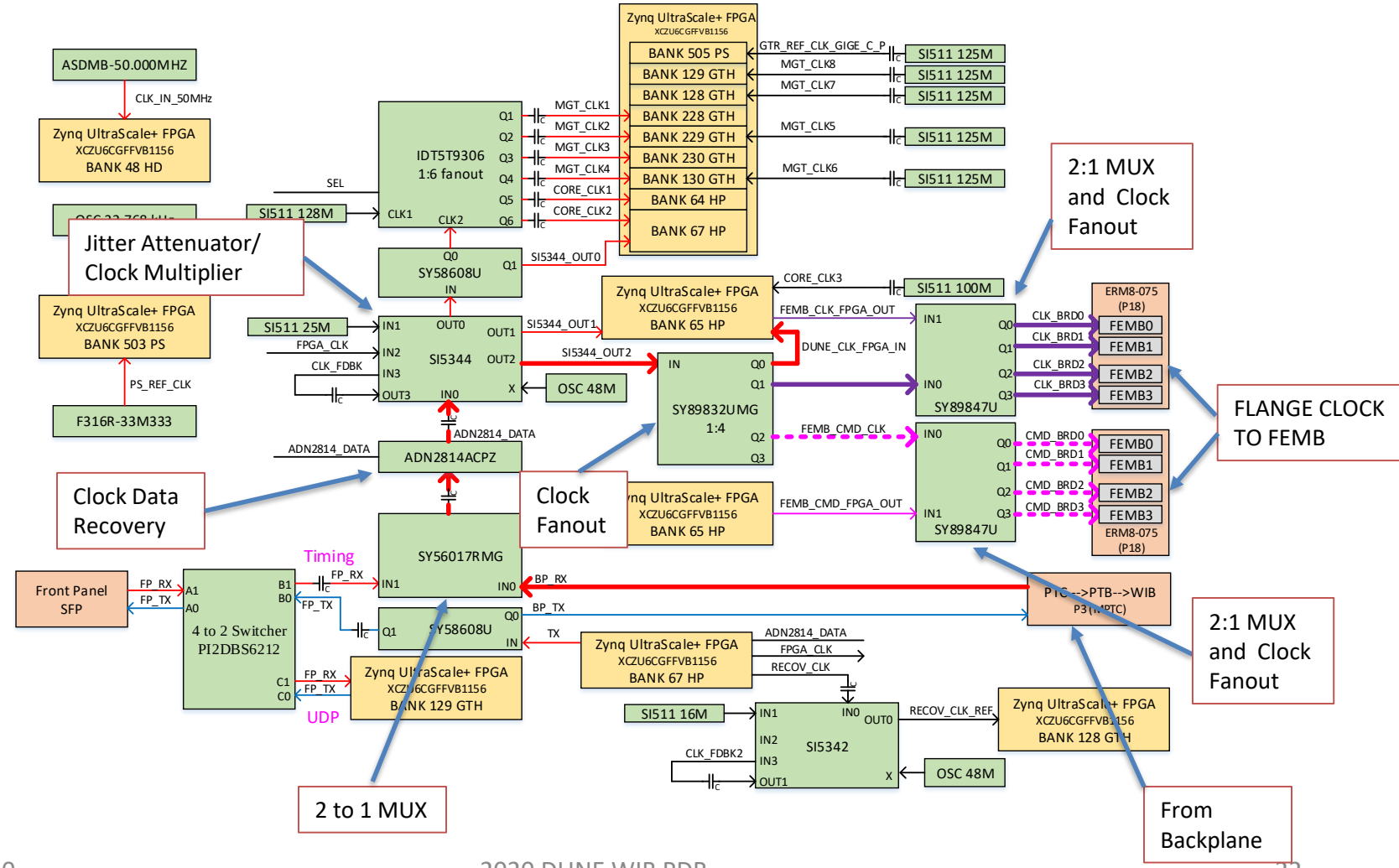
WIB FEMB Clock Distribution Using Front Panel Timing Fiber



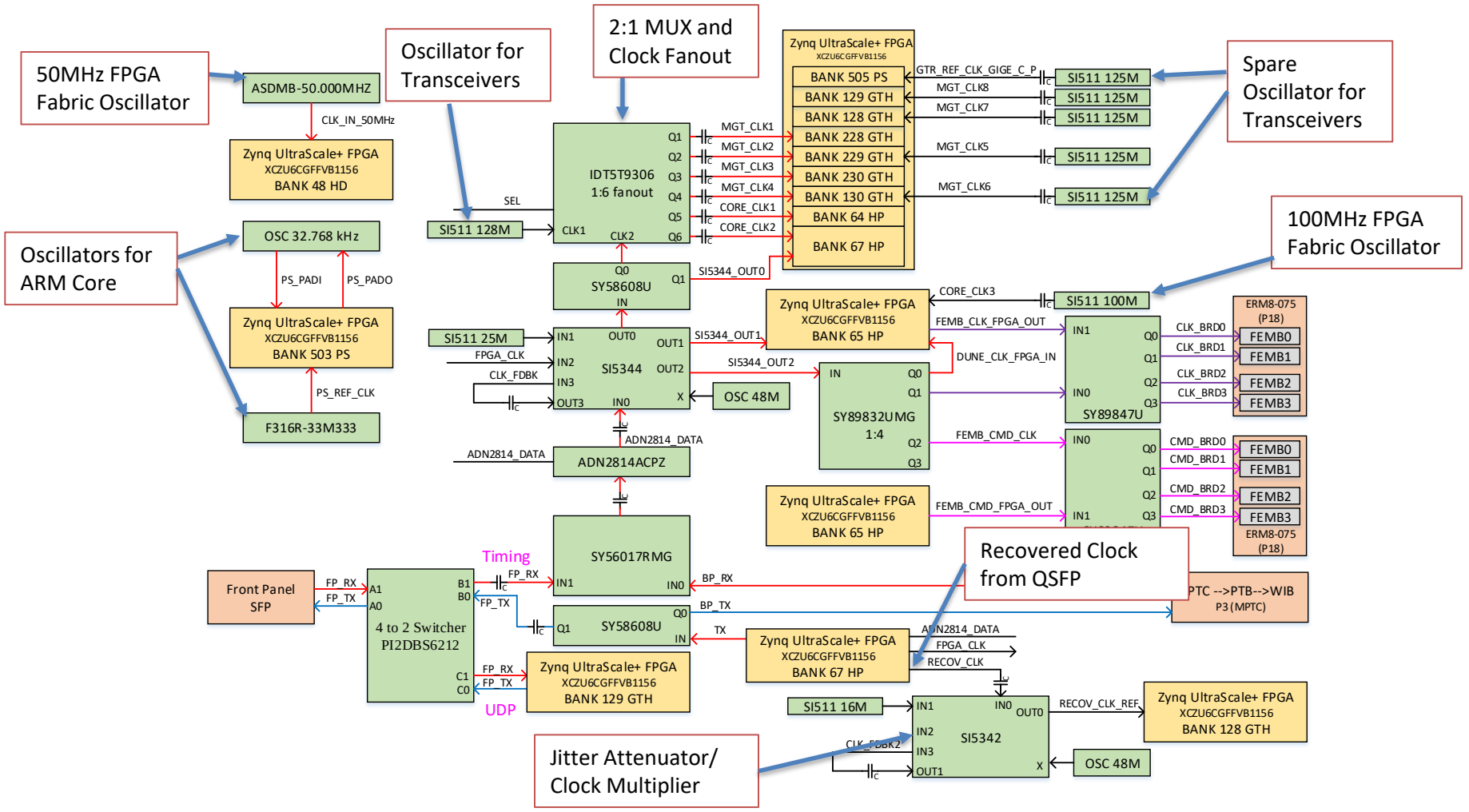
WIB FEMB Clock Distribution Using (PTB) Backplane



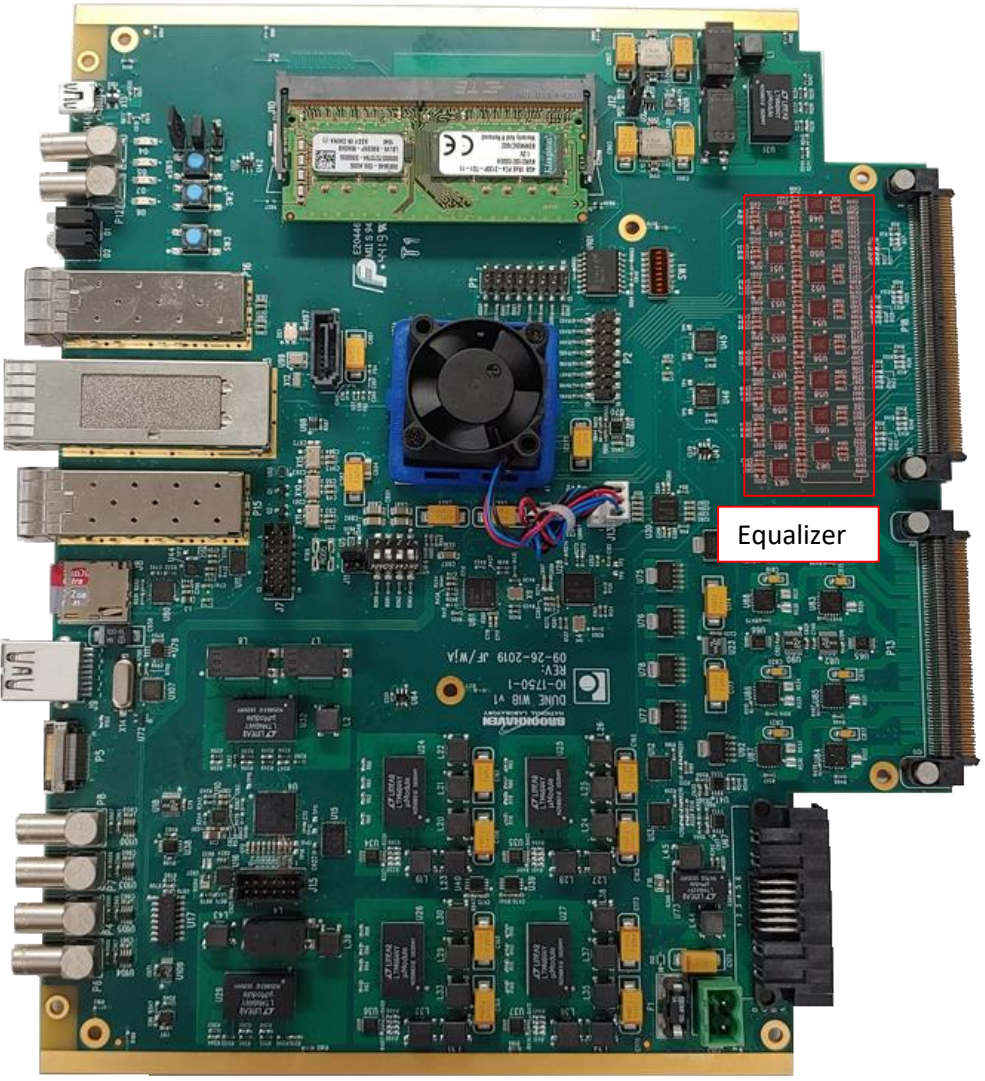
WIB FEMB Clock Distribution
FEMB with Two Clocks



WIB Clock Distribution

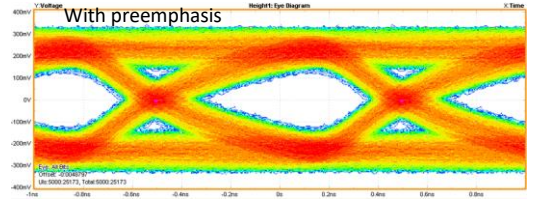


WIB Adaptive Equalizer

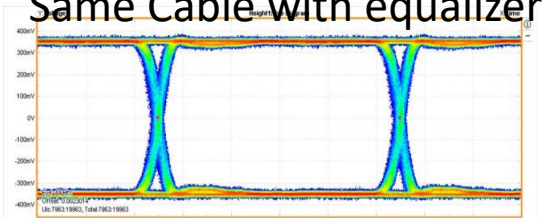


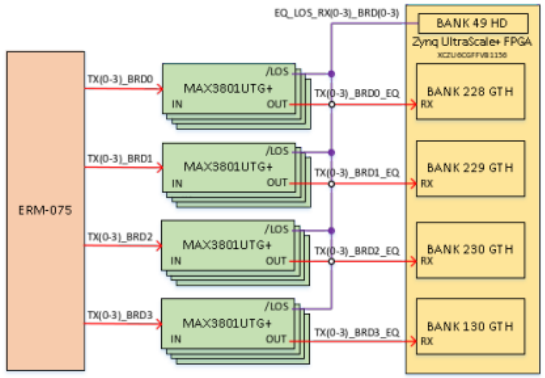
- Adaptive cable equalizer
  - MAX3801
  - Can be bypasses if not required

Samtec 18m 26awg @ RT

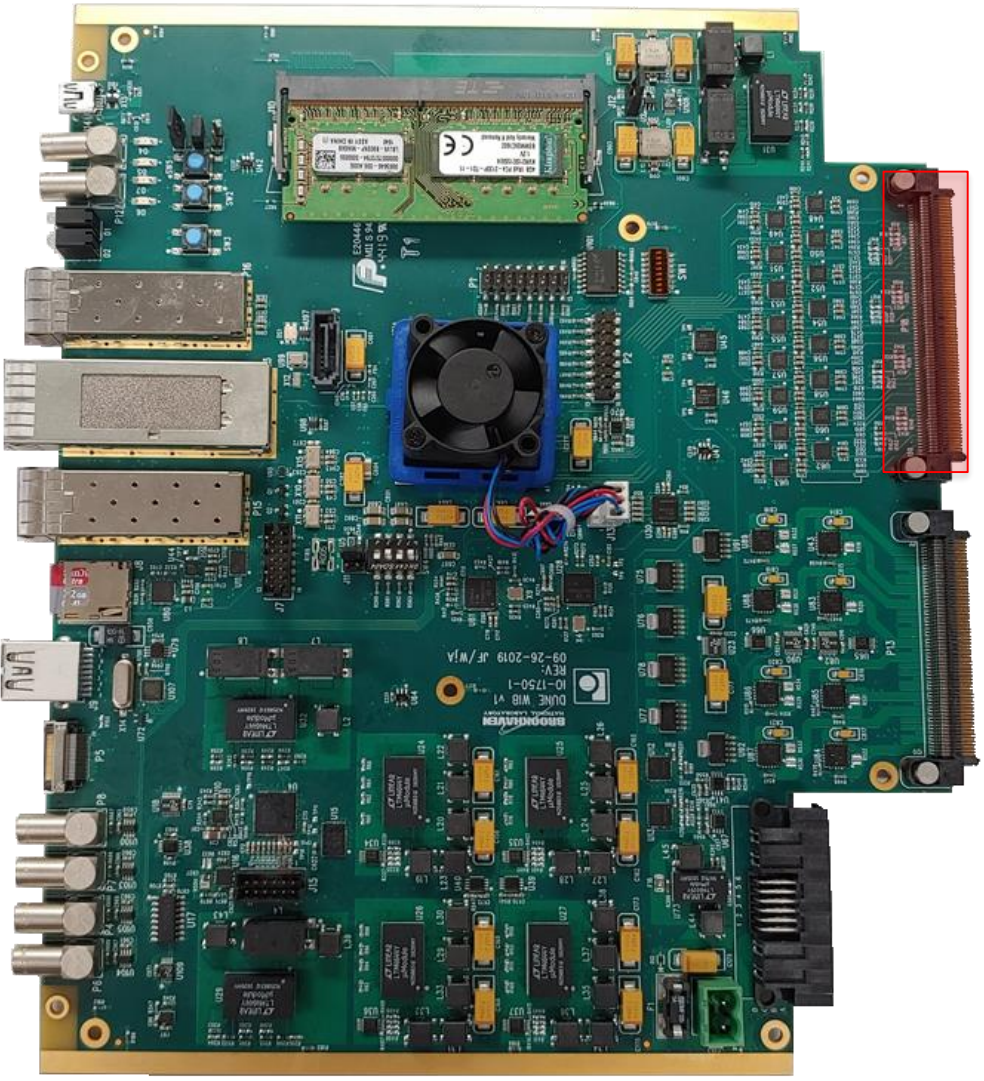


Same Cable with equalizer





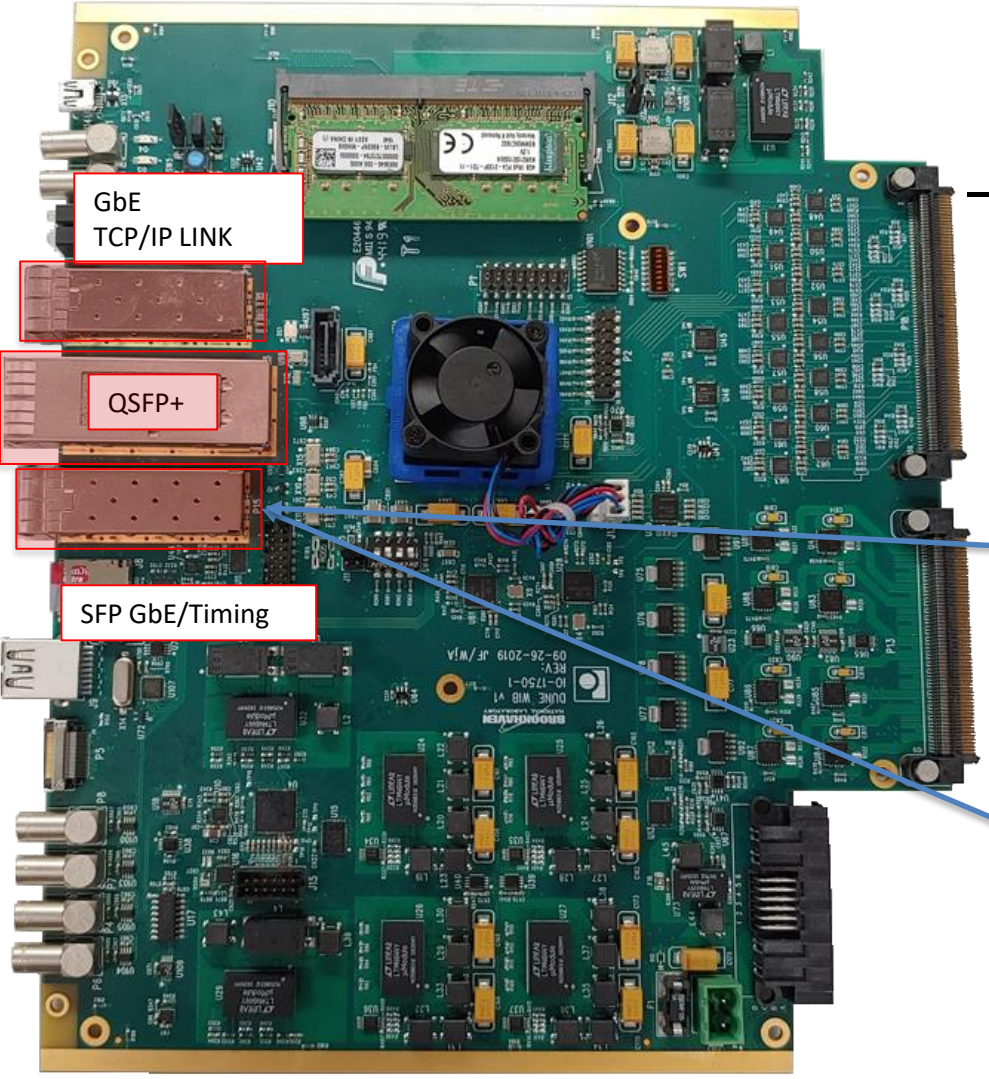
WIB FEMB IO



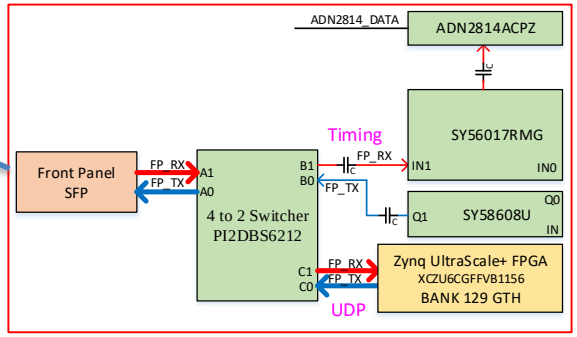
- FEMB IO connections
  - Four data links
    - From ERM8 to Adaptive Equalizer to ZYNQ GTH bank
  - Six pairs of differential IO connected to FPGA HP banks
  - Two timing critical IO LVDS pairs connected to FPGA HP bank or Si5344 PLL jitter cleaner. (LVDS)

Signal name	Type	# of Pairs
4xData Links	Differential	**4**
FEMB FANOUT CLOCK 1	Differential	**1**
FEMB FANOUT CLOCK 2	Differential	**1**
LVDS IO 1	Differential	**1**
LVDS IO 2	Differential	**1**
LVDS IO 3	Differential	**1**
LVDS IO 4	Differential	**1**
LVDS IO 5 / ANALOG MONITOR	Differential	**1**
LVDS IO 6	Differential	**1**

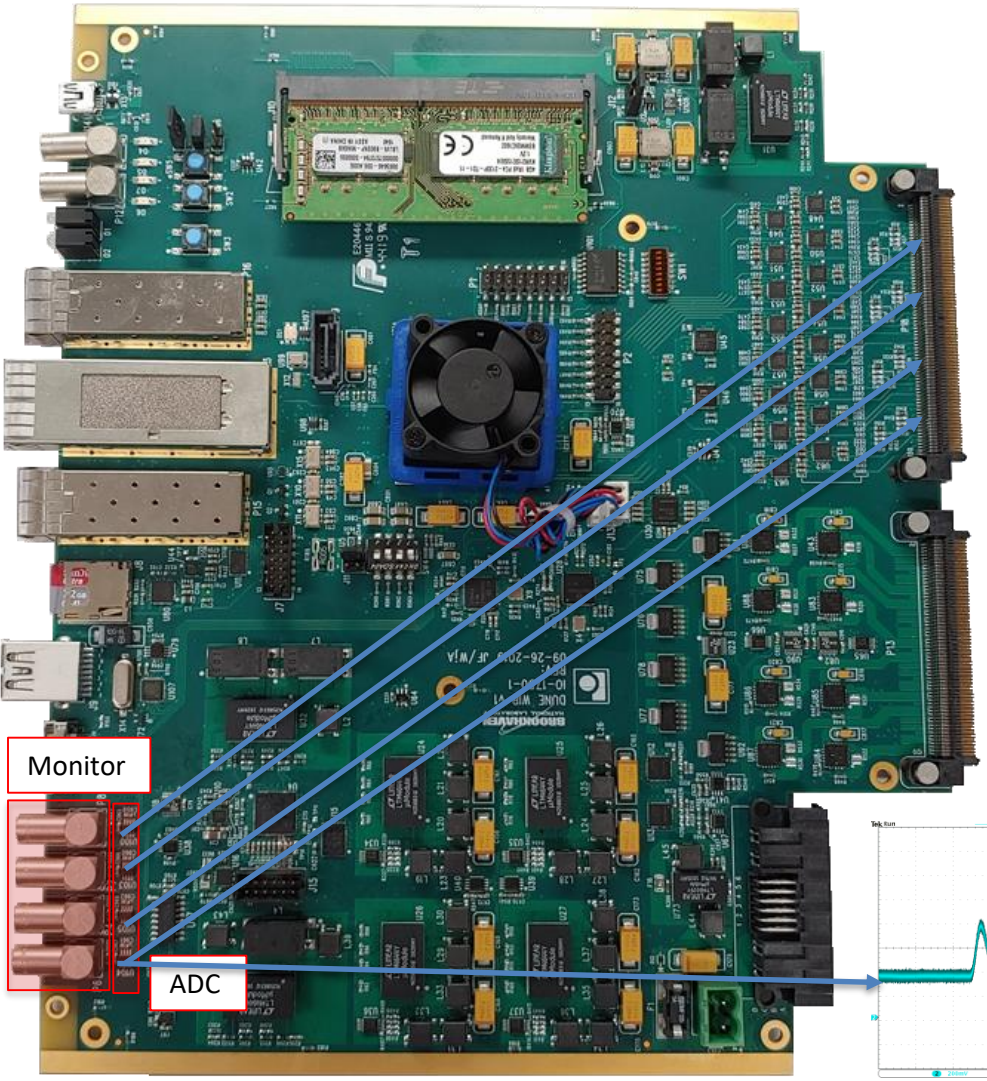
WIB Communication



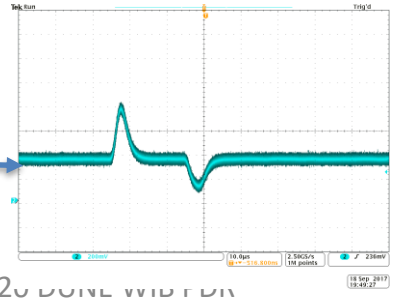
- Communication
  - QSFP+ (could be replaced with two SFP+ to facilitate fiber routing) → FELIX
  - 1Gbps Ethernet Fiber for TCP/IP link → Slow Control / CCM
  - SFP for DUNE timing system or GbE UDP or TCP

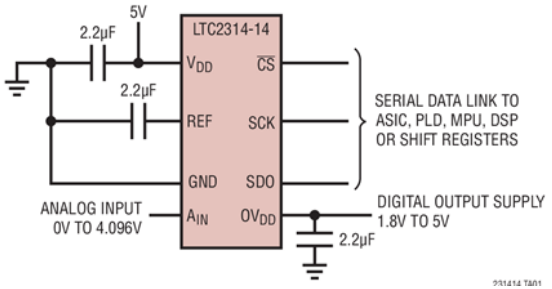


FEMB Analog Monitor

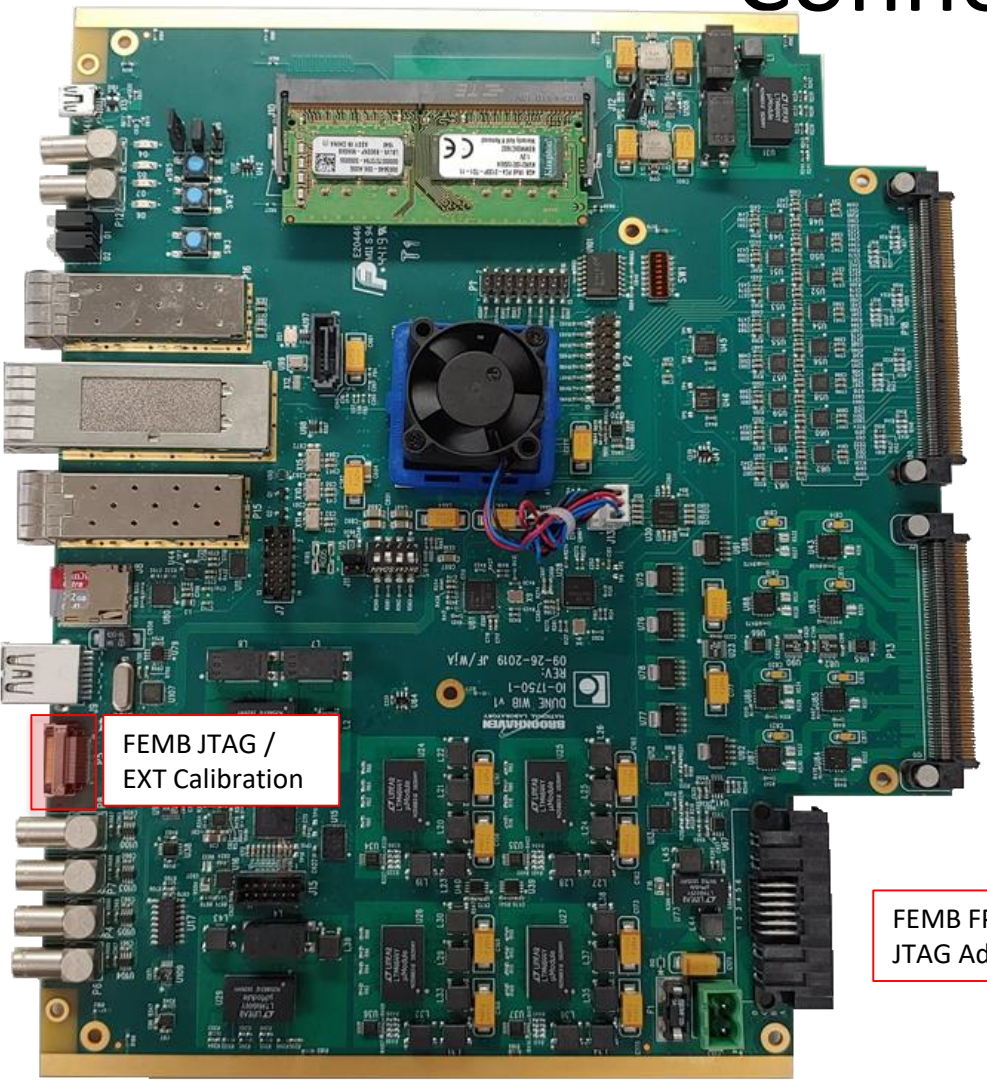


- Analog monitors one for each FEMB
- LTC2314-14 4.5Msps 14bit sampling ADC
  - Used to measure FEMB LArASIC monitor output temperature , channel baseline and bandgap
- Can be used to Inject external test pulse

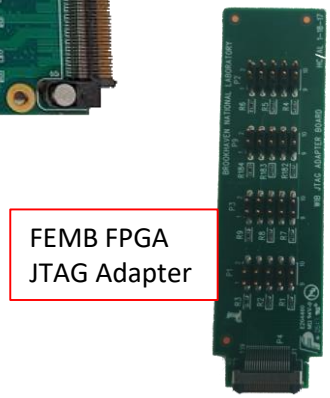


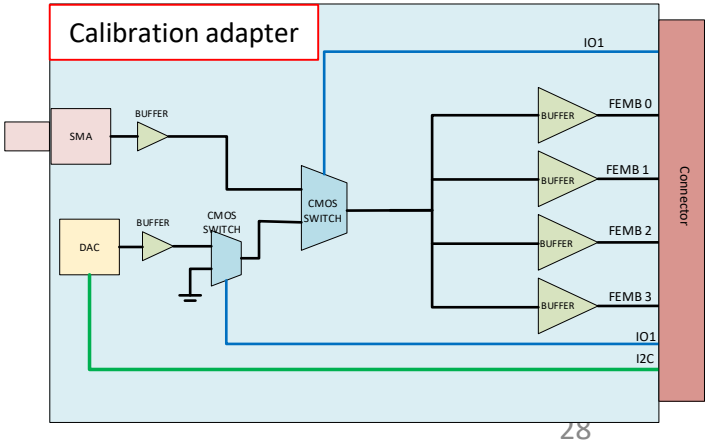


WIB FEMB JTAG/Calibration Connector

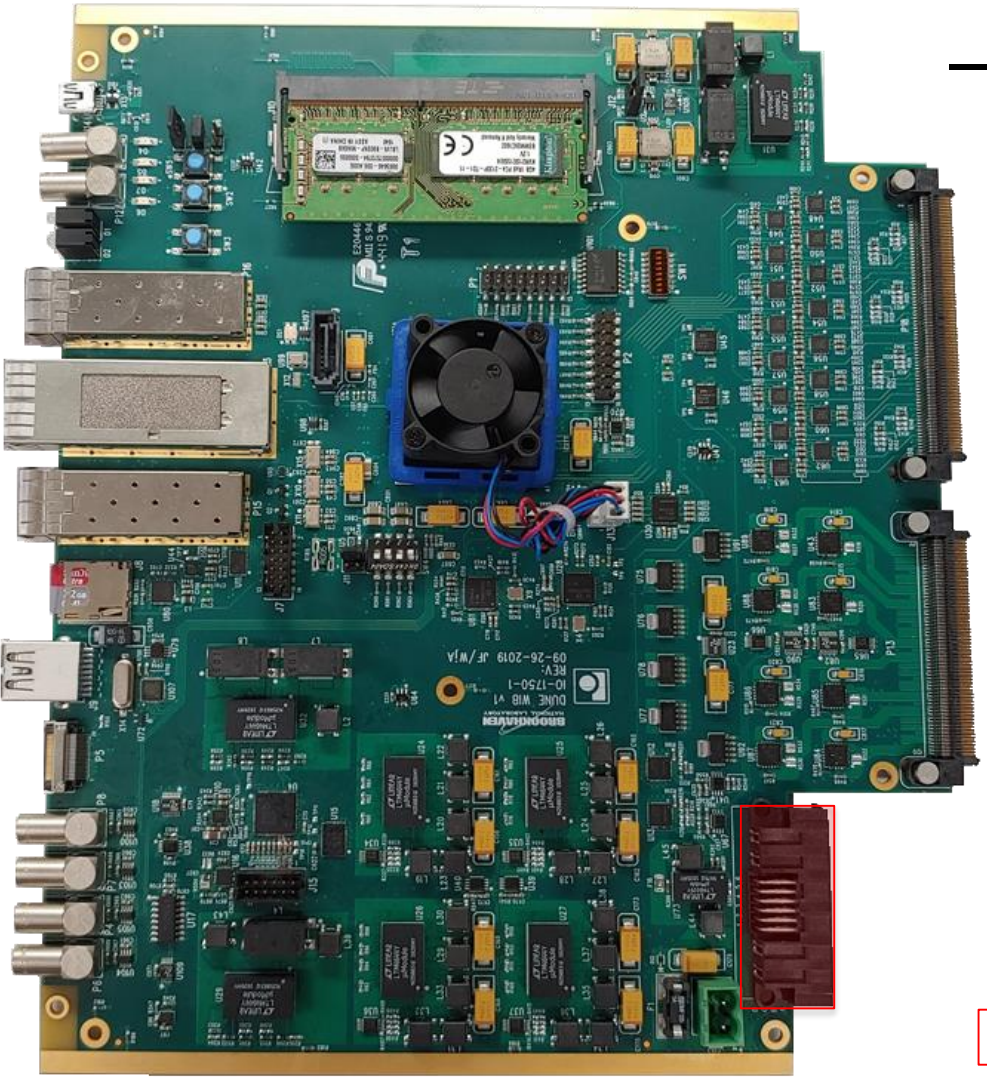


- FEMB FPGA JTAG adapter
  - Used to program FPGA based FEMBs
- Calibration adapter
  - Inject external calibration pulse to FEMBs using DAC or external input
- Connector signals
  - Four FEMB JTAG signals
  - FEMB calibration connections to flange one for each FEMB
  - One I2C link
  - Two digital IO signal
  - Power 2.5V and 3.3V

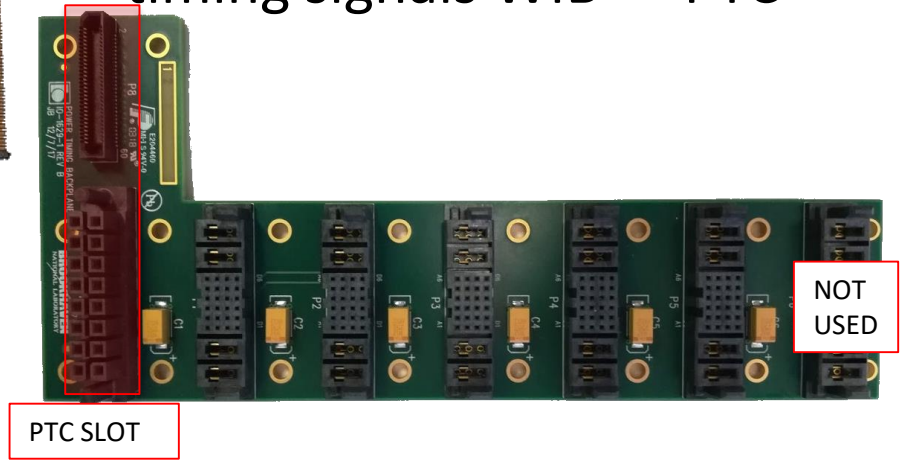




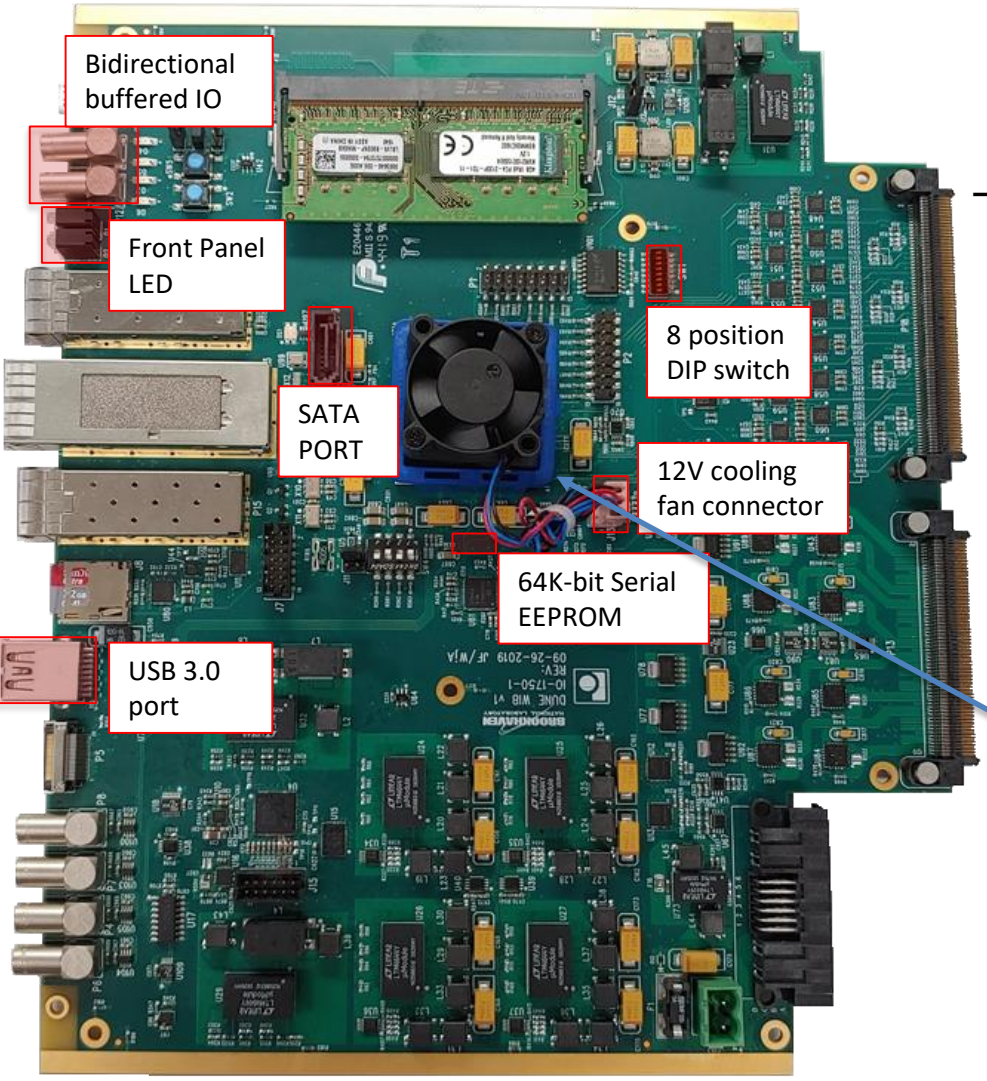
WIB <-> PTB <-> PTC Communication



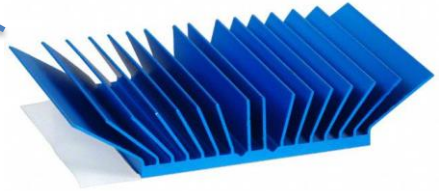
- WIB PTB IO
  - Four bit slot address
  - 6 DIFF or 12 SE bussed signals
    - Used for crate addressing and WIB PTC communication.
  - Two point to point LVDS timing signals WIB<->PTC



WIB Miscellaneous Features

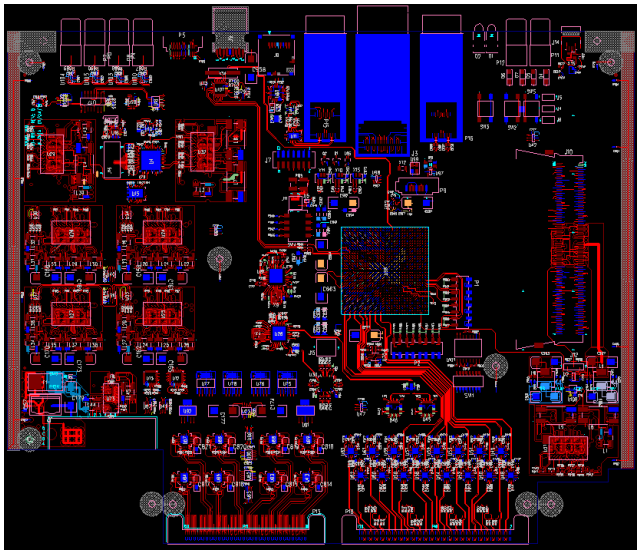


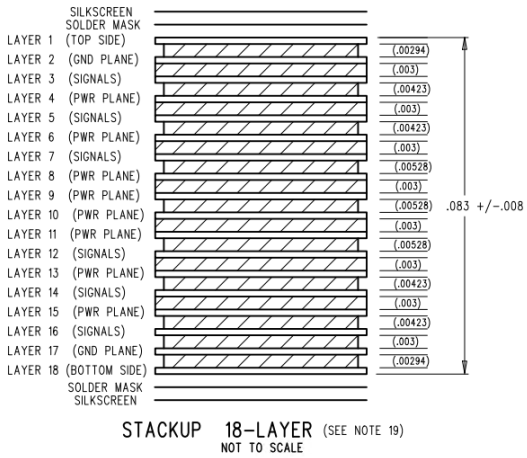
- WIB Miscellaneous Features
  - 8 position DIP switch
  - 4 Front panel LEDs
    - Because we need blinking lights
  - Two buffered bidirectional IO
    - 3.3V output
    - 5V input tolerant
  - SATA 3.1 6GHz line rates
  - USB 2.0/3.0
  - 64K-bit serial EEPROM
  - Cooling fan connector **NOT required**
    - Passive cooling using heatsink is sufficient for bench testing
    - WIEC has active cooling



WIB PCB Layout

- 18 Layer PCB
  - 8 signal layers
  - 8 power layers
  - 2 ground layers
- ½ oz copper for outer and internal signal layers
- 1 oz copper for plane layers
- Overall board thickness 0.083 +/- .008
- Multiple impedance requirements for differential and single ended signals especially for the DDR4





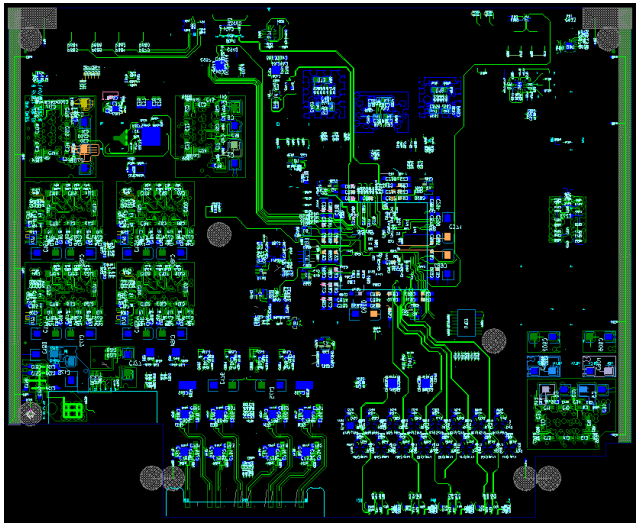
STACKUP 18-LAYER (SEE NOTE 19)
NOT TO SCALE

MATERIAL STACKUP AND TRACE WIDTHS MAY BE MODIFIED. FINAL IMPEDANCE VALUES MUST BE ACHIEVED FOR THE FOLLOWING:

LAYERS 1 AND 18:
- 66ohm +/-10% DIFFERENTIAL FOR 7.6 MIL TRACE PAIRS.
- 86ohm +/-10% DIFFERENTIAL PAIRS (NOT USED).
- 100ohm +/-10% DIFFERENTIAL FOR 3.4 MIL TRACE PAIRS.
- 39ohm +/-10% SINGLE-ENDED FOR 7.5 MIL TRACES.
- 50ohm +/-10% SINGLE-ENDED TRACES (NOT USED).

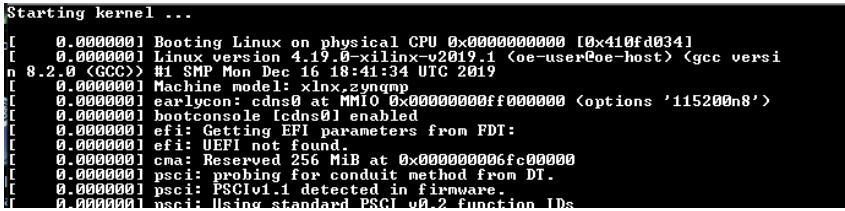
LAYERS 3, 5, 14, 16:
- 66ohm +/-10% DIFFERENTIAL FOR 6.3 MIL TRACE PAIRS.
- 86ohm +/-10% DIFFERENTIAL FOR 3.6 MIL TRACE PAIRS.
- 100ohm +/-10% DIFFERENTIAL FOR 3 MIL TRACE PAIRS.
- 39ohm +/-10% SINGLE-ENDED FOR 5 MIL TRACES.
- 50ohm +/-10% SINGLE-ENDED FOR 3.1 MIL TRACES.

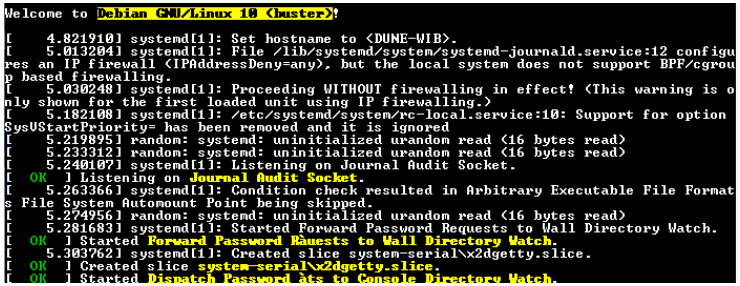
LAYERS 7, 12:
- 66ohm +/-10% DIFFERENTIAL FOR 6.6 MIL TRACE PAIRS.
- 86ohm +/-10% DIFFERENTIAL FOR 3.7 MIL TRACE PAIRS.
- 100ohm +/-10% DIFFERENTIAL FOR 3.1 MIL TRACE PAIRS.
- 39ohm +/-10% SINGLE-ENDED FOR 5.4 MIL TRACES.
- 50ohm +/-10% SINGLE-ENDED FOR 3.35 MIL TRACES.

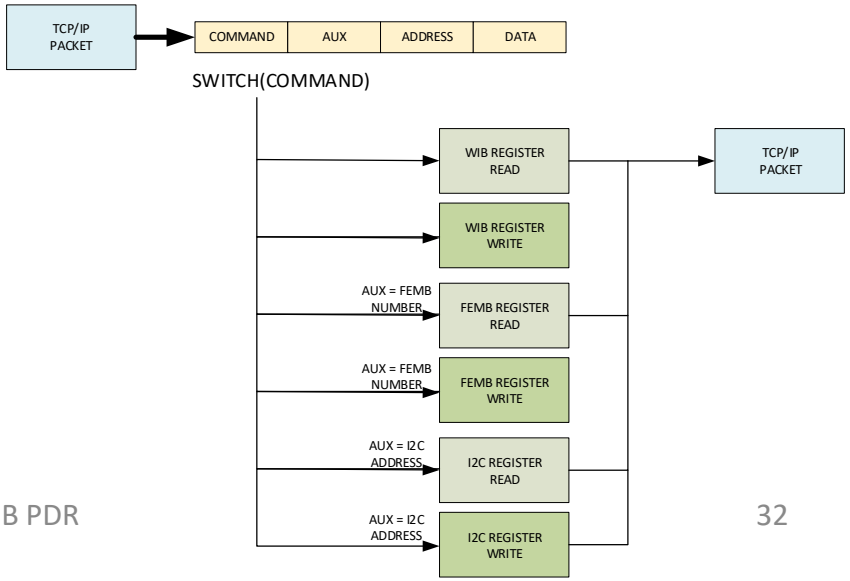


WIB Zynq Ultrascale+ Testing

- Linux Kernel
  - Linux version 4.19.0-xilinx-v2019.1
  - Located on SD CARD
- Linux File System
  - Debian GNU/Linux 10 (buster)
  - Located on SD CARD
- Simple C++ WIB server application
  - TCP/IP interface
  - Labview/Python client
  - Functions (so far)
    - WIB register peek / poke
    - FEMB register peek / poke
    - I2C control
  - Simple interface allows for quick testing of WIB functions

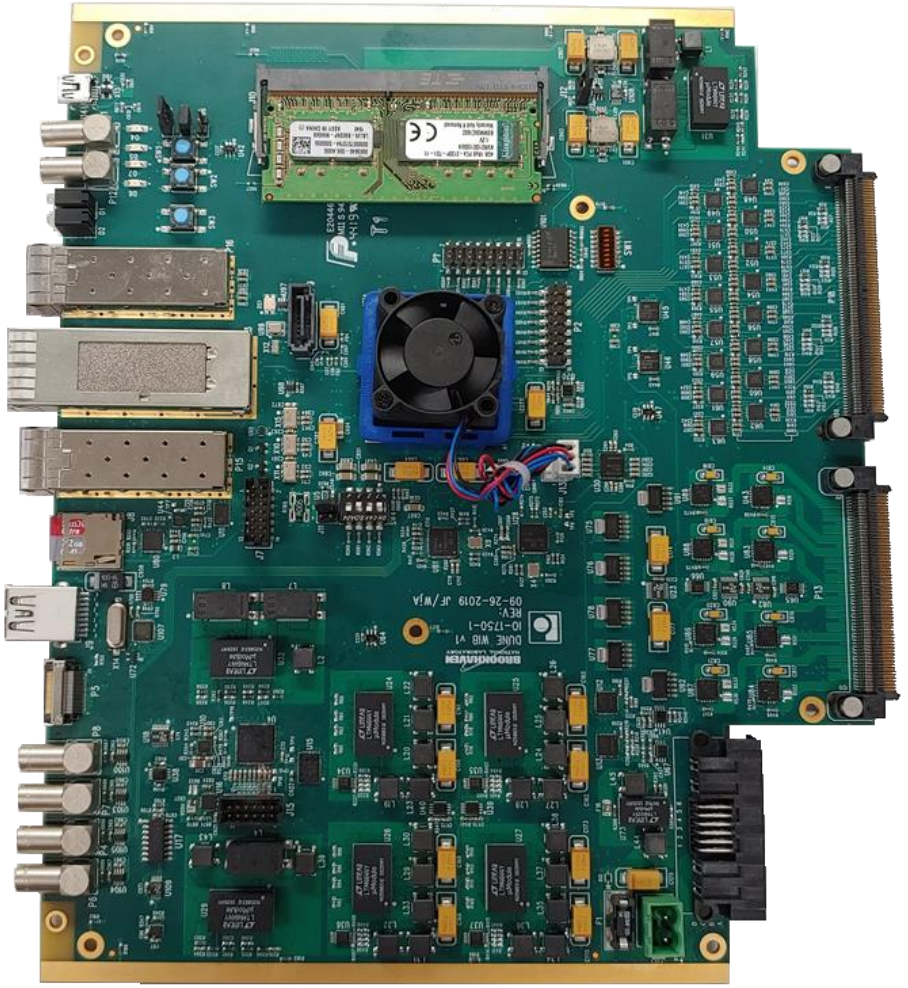






WIB Zynq Ultrascale+ Status

- WIB SocFPGA power management
  - Sequencing control --PASS/DONE
  - Fault management --PASS/DONE
  - Voltage output auto trim --PASS/DONE
- Zynq SocFPGA PL & PS configuration
  - JTAG --PASS/DONE
  - SD CARD --PASS/DONE
  - QSPI --PASS/DONE
- DDR4
  - Functional Testing & validation --PASS/DONE
- ZYNQ PS GIG-E sgmii interface
  - Functional Testing --PASS/DONE
- WIB FEMB communication
  - FEMB clock and data IO -- PASS/DONE
    - Functionality test
- WIB QSFP 10Gb DAQ link
  - Functional Testing & validation test -- PASS/DONE
- WIB FEMB power management
  - Functional Testing --in progress
- WIB timing system
  - SI5344 PLL -- PASS/DONE
  - SI5342 PLL -- PASS/DONE
  - Front panel auxiliary SFP port --not started
  - Bristol timing system AD2814 --not started
- WIB FEMB monitors
  - FEMB monitor ADC's --not started

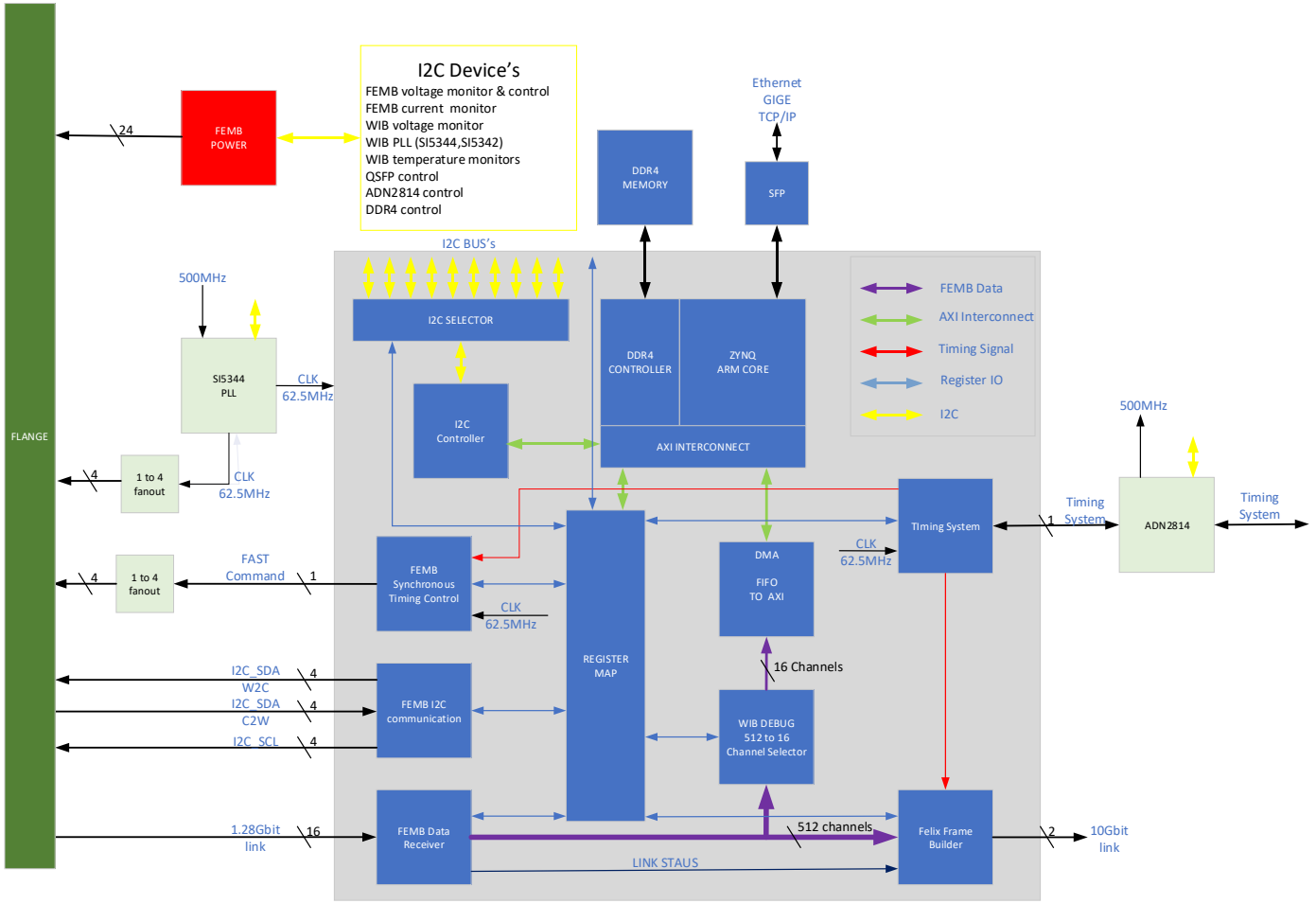


Summary

- Four Xilinx Zynq style WIBs populated and tested with ZU9EG
  - One WIB sent to UPENN for testing and development
- Link to Schematic
  - https://docs.dunescience.org/cgi-bin/private/RetrieveFile?docid=17849&filename=DUNE_WIB.pdf&version=2
- Link to BOM
  - https://docs.dunescience.org/cgi-bin/private/RetrieveFile?docid=17849&filename=IO-1650-1_BOM_01032019.xlsx&version=2
- Link to Gerber's
  - https://docs.dunescience.org/cgi-bin/private/RetrieveFile?docid=17849&filename=IO-1750-1_artwork.pdf&version=2

BACKUP

BNL Xilinx ZYNQ WIB Firmware



Zynq® UltraScale+™ MPSoCs: CG Devices

		Device Name[1]	ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG
Processing System (PS)	Application Processor Unit	Processor Core	**Dual-core** ARM® Cortex™-A53 MPCore™ up to 1.3GHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB						
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore up to 533MHz						
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core						
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC						
		Static Memory Interfaces	NAND, 2x Quad-SPI						
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet						
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO						
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains						
		Security	RSA, AES, and SHA						
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor						
PS to PL Interface			12 x 32/64/128b AXI Ports						
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600
		CLB Flip-Flops (K)	94	141	176	234	429	461	548
		CLB LUTs (K)	47	71	88	117	215	230	274
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520
		PCI Express® Gen 3x16	-	-	2	2	-	2	-
		150G Interlaken	-	-	-	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-
		AMS - System Monitor	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-
	Speed Grades	Extended[2]	-1 -2 -2L						
		Industrial	-1 -1L -2						

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

Zynq® UltraScale+™ MPSoCs: EG Devices

		Device Name[1]	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** ARM® Cortex™-A53 MPCore™ up to 1.5GHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB										
	Real-Time Processor Unit	Processor Core	**Dual-core** ARM Cortex-R5 MPCore™ up to 600MHz										
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core										
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 667MHz										
		Memory	L2 Cache 64KB										
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC										
		Static Memory Interfaces	NAND, 2x Quad-SPI										
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet										
		General Connectivity	2xUSB 2.0, 2x SD/SDIO, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO										
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains										
		Security	RSA, AES, and SHA										
		AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor										
PS to PL Interface			12 x 32/64/128b AXI Ports										
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256	469	504	600	653	747	926	1,143
		CLB Flip-Flops (K)	94	141	176	234	429	461	548	597	682	847	1,045
		CLB LUTs (K)	47	71	88	117	215	230	274	299	341	423	523
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5	6.9	6.2	8.8	9.1	11.3	8.0	9.8
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1	25.1	11.0	32.1	21.1	26.2	28.0	34.6
		UltraRAM (Mb)	-	-	13.5	18.0	-	27.0	-	22.5	31.5	28.7	36.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4	4	8	4	8	4	11	11
	Integrated IP	DSP Slices	240	360	728	1,248	1,973	1,728	2,520	2,928	3,528	1,590	1,968
		PCI Express® Gen 3x16	-	-	2	2	-	2	-	4	-	4	5
		150G Interlaken	-	-	-	-	-	-	-	1	-	2	4
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-	-	-	-	2	-	2	4
		AMS - System Monitor	1	1	1	1	1	1	1	1	1	1	1
	Transceivers	GTH 16.3Gb/s Transceivers	-	-	16	16	24	24	24	32	24	44	44
		GTY 32.75Gb/s Transceivers	-	-	-	-	-	-	-	16	-	28	28
	Speed Grades	Extended[2]	-1 -2 -2L			-1 -2 -2L -3				-1 -2 -2L -3			
		Industrial						-1 -1L -2					

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.