WIB Firmware/Software Development Plans

H. CHEN ON BEHALF OF WI ELECTRONICS TEAM

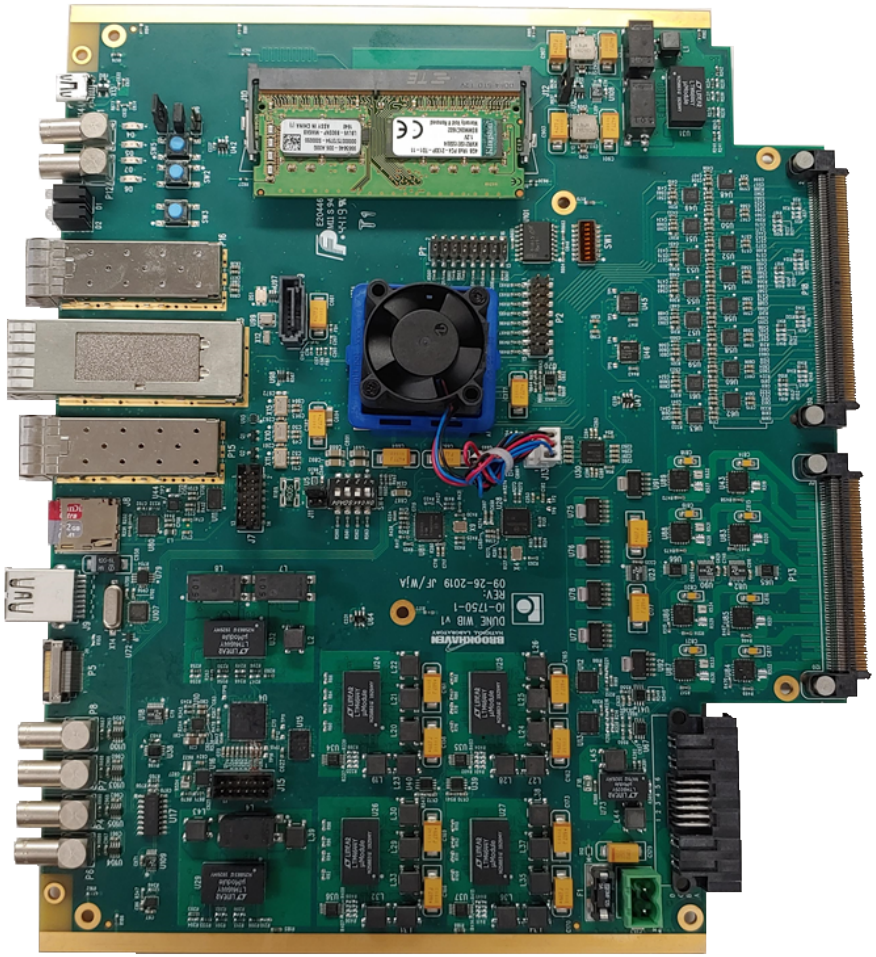
BROOKHAVEN NATIONAL LABORATORY

MARCH 10TH, 2020

Outline

- Introduction
- WIB FW/SW Development for APA7/ProtoDUNE II
- WIB FW/SW Development for DUNE Far Detector
- Summary

Introduction

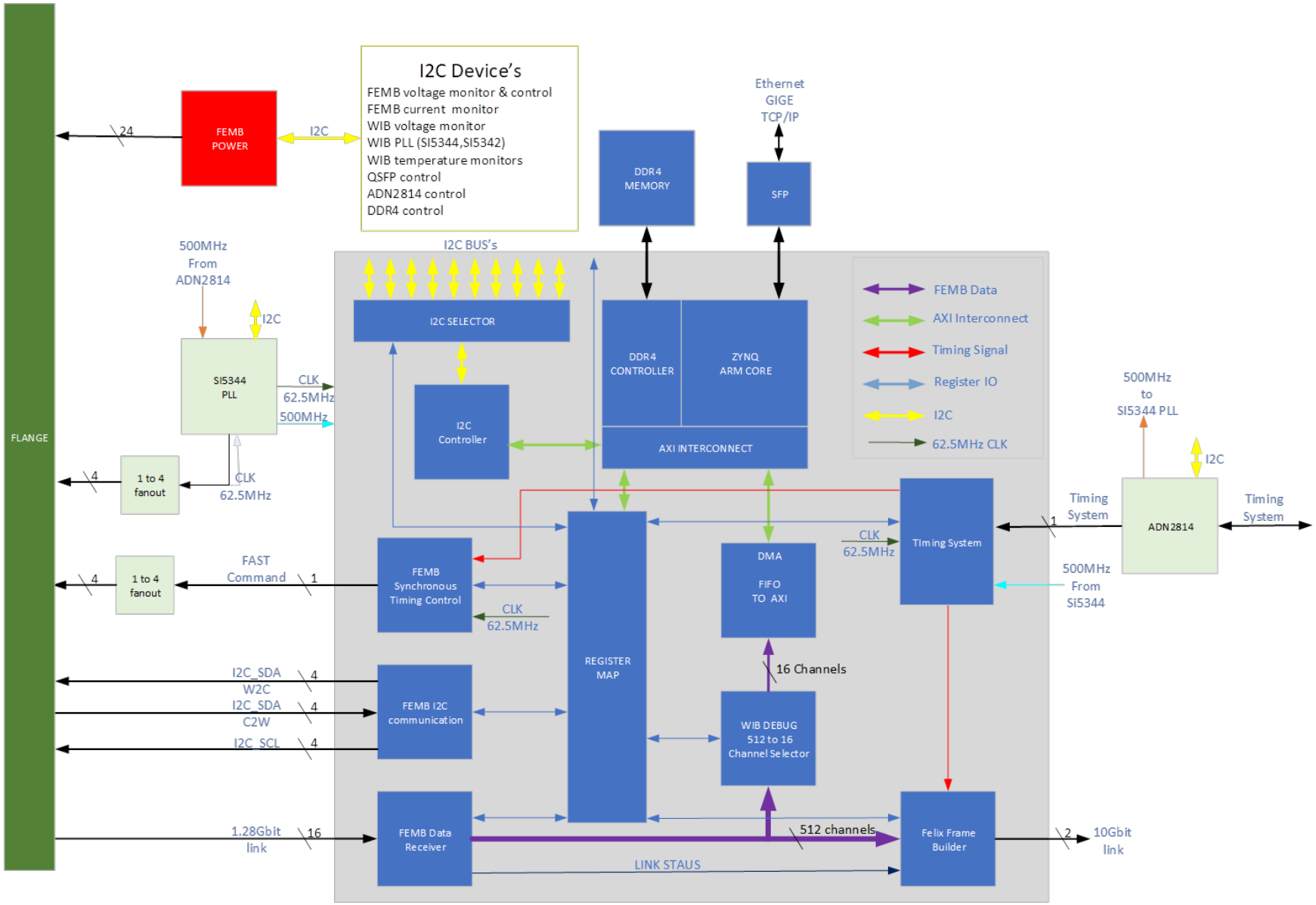


- Successful ProtoDUNE-SP operation in 2018-2020 provides valuable experience for WIB development
- An intermediate WIB prototype is developed for APA7/ProtoDUNE II
  - Migration from Intel/ALTERA Arria V to Xilinx Zynq+ FPGA for more resources and lower cost
  - ARM processor embedded in Zynq+ FPGA provides flexibilities in FW/SW development
  - ***Significant cost impact***: $1,360.6 vs. $799.77
    - With latest quote of $343.30 from CERN, ~25% of FPGA cost on ProtoDUNE WIB
- WIB for DUNE far detector is collecting requirements for development of specifications
  - See Volodya's talk on HW requirements
  - See Josh's talk on FW/SW requirements

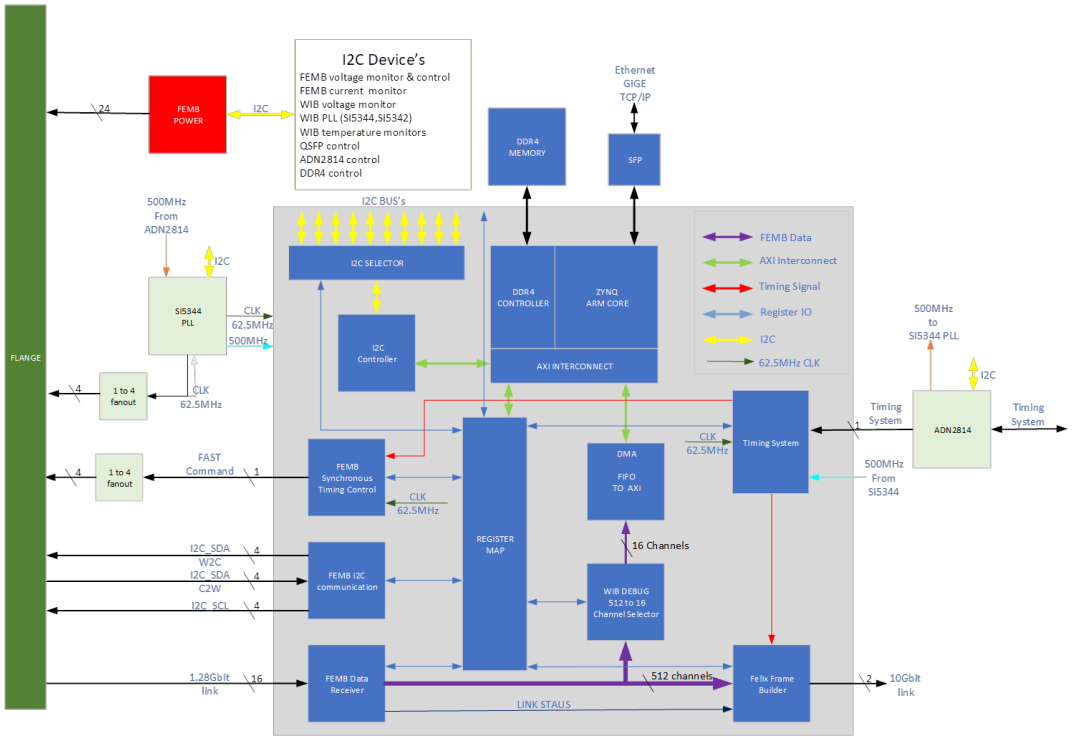
WIB FW/SW Development for APA7/ProtoDUNE II

- Firmware development will take place at BNL and Penn
  - BNL firmware development will focus on the hardware functionality test and interfaces with CE/DAQ
  - Penn firmware development will focus on the integration in the readout system with DAQ through FULL mode links to FELIX
- Software development will take place at Penn and other collaboration institutes
  - Penn software development will focus on Linux OS on Zynq+ FPGA
  - Collaboration institutes will development necessary software package, e.g. WIBTools, for integration with DAQ system
- Small firmware and software development teams with light coordination, similar to ProtoDUNE development
  - ProtoDUNE FW development at BNL/BU
  - ProtoDUNE SW development at BNL/MSU/LSU

WIB FW for APA7/ProtoDUNE II (1)



WIB FW for APA7/ProtoDUNE II (2)



- FEMB Interface
  - Timing control
  - I2C communication
  - Data receiver
- Timing System Interface
  - ADN2814 for CDR
- DAQ System Interface
  - 9.6 Gb/s FELIX FULL mode frame builder
- Slow Control & Monitoring
  - I2C controller
  - V/I/T control and monitoring
  - Other on board components
- Diagnostic
  - DDR4 memory
  - GbE for remote debug

WIB FW for APA7/ProtoDUNE II (3)

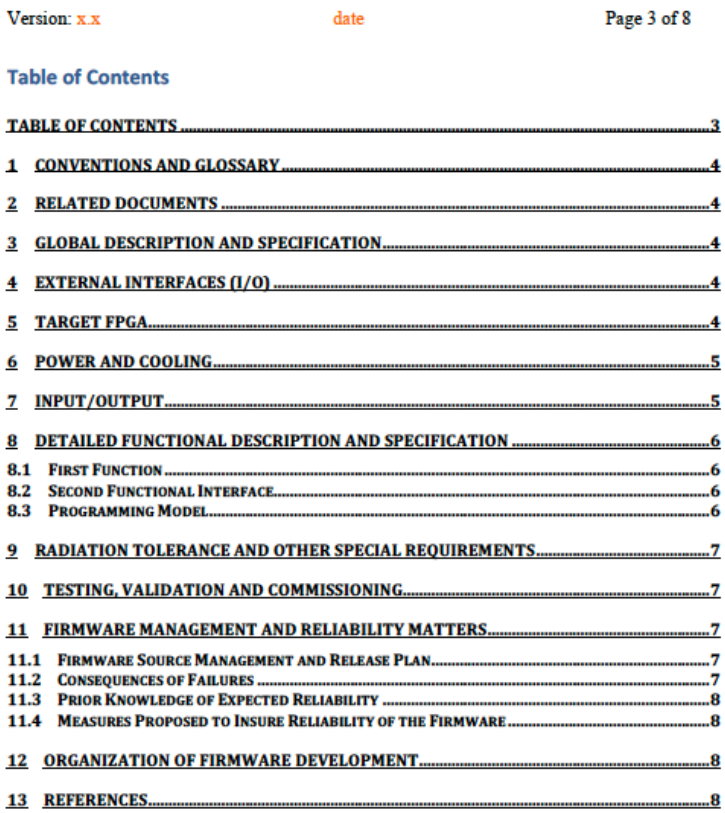
- Memory Mapped I/O
  - REG_IO_PL
    - FPGA fabric registers, primary register control
  - AXI_GPIO
    - Register IO independent of fabric register space
    - Used for fabric reset
  - AXI_DMA
    - DMA controller
  - AXI_I2C
    - I2C controller

Cell	Slave Interface	Base Name	Offset Addre... ^1	Range	High Address
zynq_ultra_ps_e_0					
Data (40 address bits : 0x00A0000000 [256M] ,0x0400000000 [4G] ,0x1000000000 [224G] ,0x00B0000000 [256M] ,0x0500000000 [4G					
axi_gpio_0	S_AXI	Reg	0x00_A000_0000	4K	0x00_A000_0FFF
axi_iic_0	S_AXI	Reg	0x00_A000_1000	4K	0x00_A000_1FFF
REG_IO_PL_0	S00_AXI	S00_AXI_reg	0x00_A000_2000	4K	0x00_A000_2FFF
axi_dma_0	S_AXI_LITE	Reg	0x00_A000_3000	4K	0x00_A000_3FFF
axi_dma_0					

WIB FW/SW Development for DUNE FD

- Firmware development will take place at collaboration institutes
  - Leading institute will coordinate firmware development with focus on the integration in the readout system with DAQ through FULL mode links to FELIX
  - BNL will participate in the coordinated firmware development, firmware for hardware functionality test and interfaces with CE/DAQ will be available
- Software development will take place at collaboration institutes
  - Leading institute for software development will work closely with firmware coordination and DAQ system
  - Including Linux OS on Zynq+ FPGA, and software package, e.g. WIBTools, for integration with DAQ system
- ***Formal firmware coordination is crucial*** for development, maintenance and operation of DUNE FD
  - Software development will be closely coordinated with DAQ system

WIB FW Specifications Document (1)



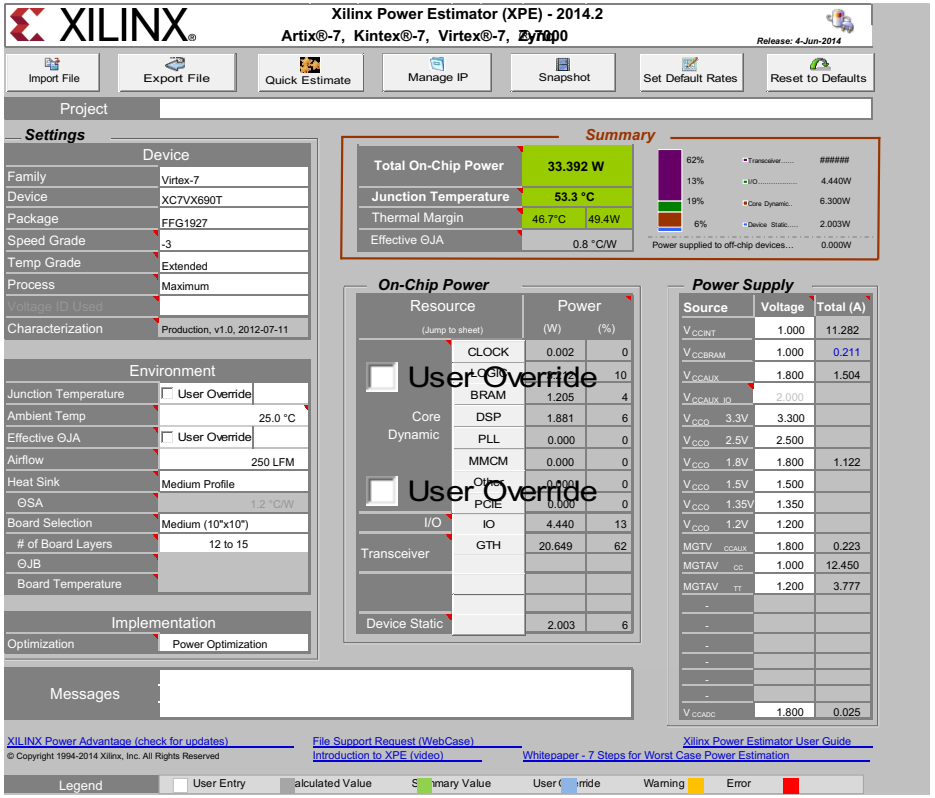
Version: x.x date Page 3 of 8

Table of Contents

Specification for name

- Firmware specifications document will be led by firmware coordinator and prepared by firmware development team
  - Plan to follow ATLAS firmware specifications document template
- Firmware specifications document is ***a living document***
  - Will be evolving along the project advancement

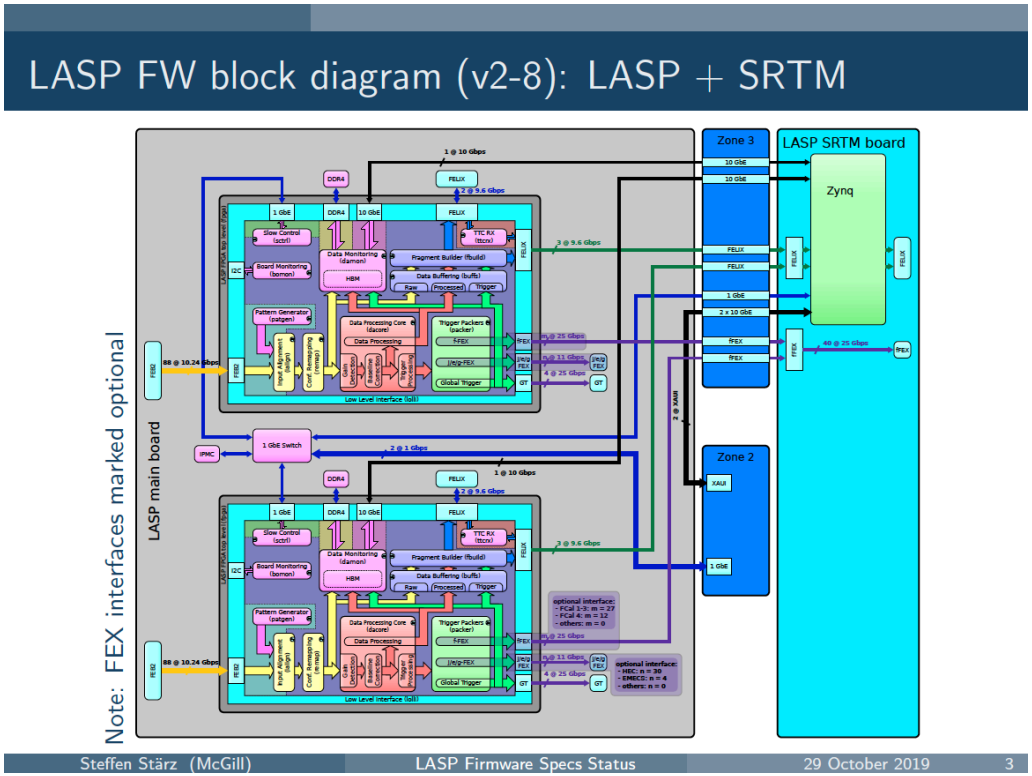
WIB FW Specifications Document (2)



Xilinx FPGA XPE Tool

- External Interface/Input Output
  - Include interfaces on board and to other system
  - Link speed, protocol and data format should be specified
  - I/O definition will evolve into a constraint file for the firmware build, may only be available by PDR
- Target FPGA/Power and Cooling
  - Require ***early interaction*** between firmware and hardware design teams
  - Power and cooling scheme in hardware design will set the ***power budget*** for firmware design
  - FPGA vendor provided tool can be used to assess the available ***FPGA resources*** → avoid the surprise down the road

WIB FW Specifications Document (3)



ATLAS LAr LASP Firmware Block

- Detailed Functional Description and Specification/Organization
  - ***Firmware block diagram***
  - Critical interfaces and parameters, e.g. latency, to be specified
  - Institutes involved and responsibilities
- Testing, Validation and Commissioning
  - Not required prior to the first specifications review
  - ***Crucial*** for FDR/PRR to prepare for firmware testing plan
  - Include ***continuous integration***, system integration test to validate firmware and assess the readiness for commissioning and operation
- Firmware Management and Reliability Matters
  - Source code management and release plan, e.g. ***git repository***
  - SEU mitigation for boards exposed to radiation → doesn't apply to WIB

Summary

- Successful ProtoDUNE-SP operation in 2018-2020 provides valuable experience for WIB development
- An intermediate WIB prototype is developed for APA7/ProtoDUNE II
  - ***More versatile FPGA with significant cost reduction***
  - FW/SW development is planned with light coordination
- WIB for DUNE far detector is collecting requirements for development of specifications
  - ***Formal firmware coordination is crucial*** for development, maintenance and operation of DUNE FD
  - Will develop ***firmware specifications document*** following ATLAS firmware template
  - Plan to have hardware and firmware reviewed simultaneously in the future reviews

Backup Slides

Warm Interface Electronics (2)

- DUNE far detector will need 750 WIBs, FPGA is the main cost driver
- Market survey has been carried out in past months
  - Current Intel FPGA cost on ProtoDUNE-SP WIB is $1,360.6 each
  - Xilinx Zynq+ offers a cost effective alternative, $799.77 each, with additional features, e.g. ARM, TCP/IP etc.

	WIB	WIB	WIB	WIB	WIB	WIB	WIB
Manufactures	Intel/Altera	Intel/Altera	Intel/Altera	Xilinx	Xilinx	Xilinx	Xilinx
Series	Arria V	Arria 10 GX	Arria 10 GX	Kintex UltraScale	Kintex UltrScale+	Kintex UltrScale+	Zynq UltraScale+
FPGA	5AGTFD3H3F35I 5N	10AX032H4F34E 3SG	10AX048H4F34E 3SG	XCKU040-1FFVA1156I	XCKU9P-1FFVE900E	XCKU11P-1FFVA1156E	XCZU6CG-1FFVB1156E
LEs (K)	362	320	480	530	600	653	469
M10K/M20K Memory Blocks	17.26 (M10K)	17.82 (M20K)	28.62 (M20K)	-	-	-	-
MLAB Memory (Mb)	2	2.7	4.2	-	-	-	-
Max. Distributed RAM (Mb)	-	-	-	7	8.8	9.1	6.9
Total Block RAM(Mb)	-	-	-	21	32.1	21.1	25.1
UltraRAM(Mb)	-	-	-	-	0	22.5	-
DSP	1045	985	1368	1920	2520	2928	1973
GPIO(3.3V/HR/HD +	544 + 0	48 + 336	48 + 444	104 + 416	96 + 208	48 + 416	120 + 208 + 214
XCVR	24 (10 Gb/s)	24(17.4 Gb/s)	24(17.4 Gb/s)	20 (12.5 Gb/s)	28 (12.5 Gb/s)	20 (12.5 Gb/s) + 8 (25 Gb/s)	24 (12.5 Gb/s)
Size (mmxmm)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (F1152)	35 x35 (A1156)	31x31 (E900)	35 x35 (A1156)	35 x35 (B1156)
Price($)	1360.6 for 744-1000 pcs quote	$1016.00 for 100-1000 pcs	$1550.00 for 100-1000 pcs	$1010.14 for 51-300 pcs quote and $769.45 for 301-1000 pcs	$1000.04 for 51-300 pcs quote and $760.84 for 301-1000 pcs	$1410.97 for 1-499 pcs and $1074.57 for 500-1000 pcs	$1050.88 for 36-249 pcs quote and $799.77 for 250-1000 pcs